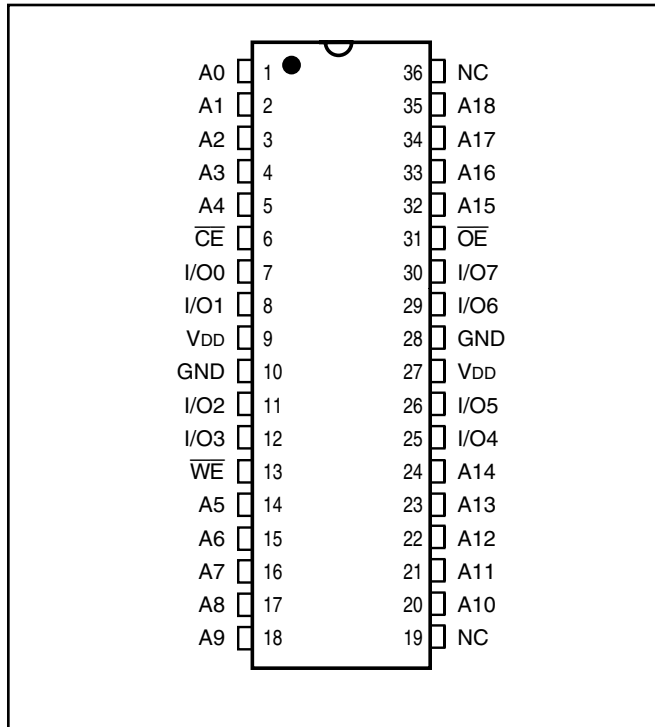
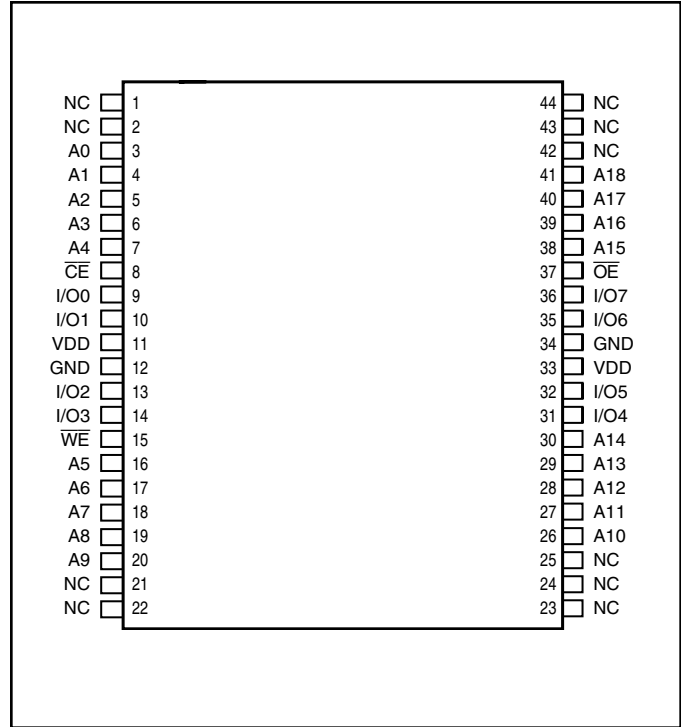


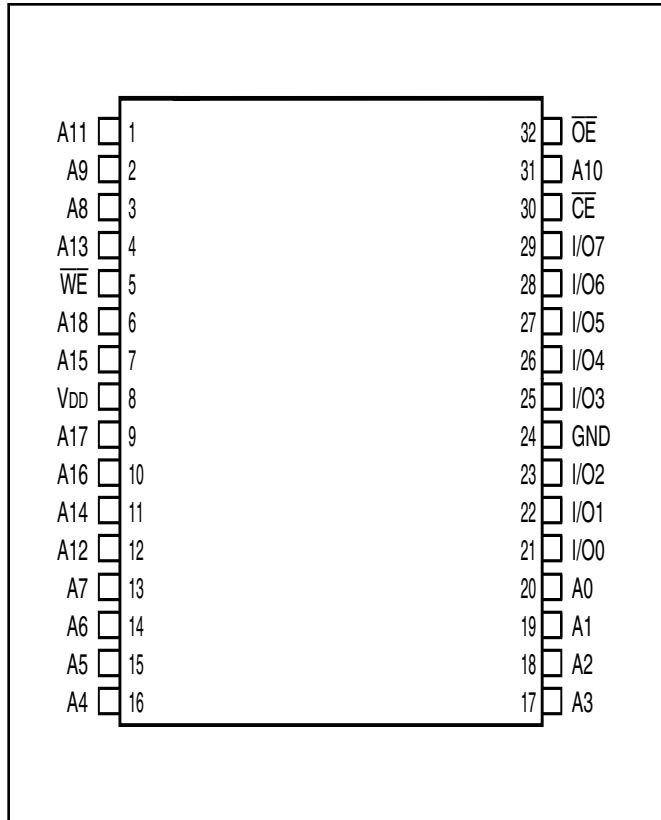
**HIGH SPEED (IS61/64C5128AL) PIN CONFIGURATION**
**36-Pin SOJ (400-mil)**

**44-Pin TSOP (Type II)**

**PIN DESCRIPTIONS**

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
VDD	Power
GND	Ground
NC	No Connection

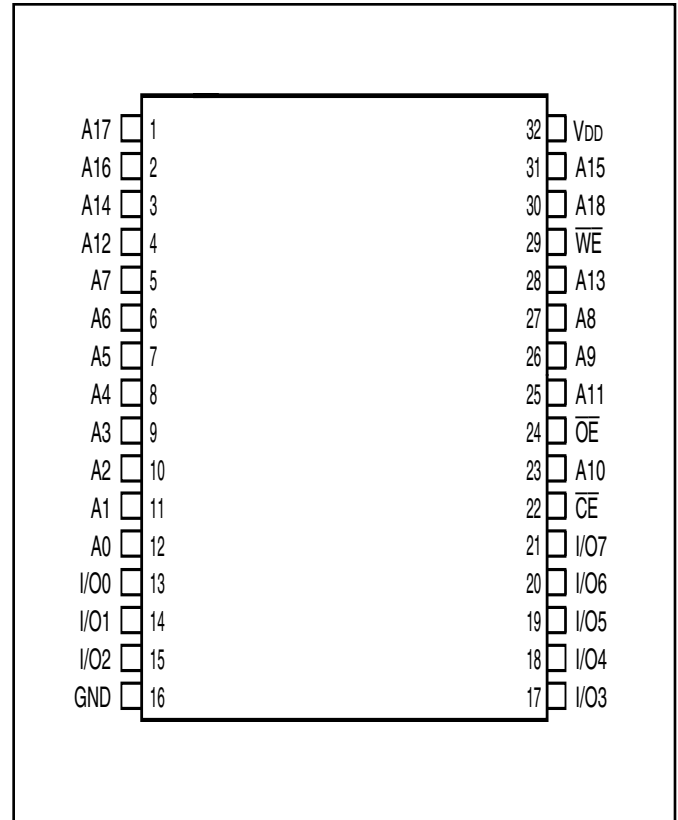
# IS61C5128AL/AS IS64C5128AL/AS

## LOW POWER (IS61/64C5128AS) PIN CONFIGURATION

### 32-pin sTSSOP (TYPE I)



### 32-pin SOP 32-pin TSOP (TYPE II)



## PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

**TRUTH TABLE**

Mode	I/O PIN				
	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O0-I/O7	V <sub>DD</sub> Current
Not Selected	X	H	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 5.0V.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	—	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>DD</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V	
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> Outputs Disabled	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA

**Note:** 1. V<sub>IL</sub> = -3.0V for pulse width less than 10 ns.

**OPERATING RANGE: HIGH SPEED OPTION (IS61/64C5128AL)**

Range	Ambient Temperature	V <sub>DD</sub>	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	10
Industrial	-40°C to +85°C	5V ± 10%	10
Automotive	-40°C to +125°C	5V ± 10%	12

**OPERATING RANGE: LOW POWER OPTION (IS61/64C5128AS)**

Range	Ambient Temperature	V <sub>DD</sub>	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	25
Industrial	-40°C to +85°C	5V ± 10%	25
Automotive	-40°C to +125°C	5V ± 10%	25

**HIGH SPEED OPTION (IS61/64C5128AL)**
**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	Test Conditions		-10 ns		-12 ns		Unit
				Min.	Max.	Min.	Max.	
I <sub>CC1</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = V <sub>DD MAX.</sub> , $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	45	—	45	mA
			Ind.	—	50	—	50	
			Auto.	—	55	—	55	
I <sub>CC2</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = V <sub>DD MAX.</sub> , $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	50	—	45	mA
			Ind.	—	55	—	50	
			Auto.	—	70	—	60	
			typ. <sup>(2)</sup>	30		25		
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = V <sub>DD MAX.</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE} \geq V_{IH}$ , f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	30	—	30	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = V <sub>DD MAX.</sub> , $\overline{CE} \leq V_{DD} - 0.2V$ , V <sub>IN</sub> $\geq V_{DD} - 0.2V$ , or V <sub>IN</sub> $\leq 0.2V$ , f = 0	Com.	—	8	—	8	mA
			Ind.	—	12	—	12	
			Auto.	—	20	—	20	
			typ. <sup>(2)</sup>	2				

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25% and not 100% tested.

**LOW POWER OPTION (IS61/64C5128AS)**
**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	Test Conditions		-25 ns		Unit
				Min.	Max.	
I <sub>CC</sub>	Average operating Current	$\overline{CE} = V_{IL}$ , V <sub>DD</sub> = Max. I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	10	mA
			Ind.	—	15	
			Auto.	—	20	
I <sub>CC1</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	25	mA
			Ind.	—	30	
			Auto.	—	40	
			typ. <sup>(2)</sup>	15		
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE} \geq V_{IH}$ , f = 0	Com.	—	1	mA
			Ind.	—	1.5	
			Auto.	—	2	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CE} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> $\geq V_{DD} - 0.2V$ , or V <sub>IN</sub> $\leq V_{SS} + 0.2V$ , f = 0	Com.	—	0.8	mA
			Ind.	—	0.9	
			Auto.	—	2	
			typ.	0.2		

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25% and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	-10		-12		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	10	—	12	—	25	—	ns
$t_{AA}$	Address Access Time	—	10	—	12	—	25	ns
$t_{OHA}$	Output Hold Time	3	—	3	—	3	—	ns
$t_{ACE}$	$\overline{CE}$ Access Time	—	10	—	12	—	25	ns
$t_{DOE}$	$\overline{OE}$ Access Time	—	5	—	6	—	15	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	5	0	6	0	8	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	2	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	5	0	6	0	8	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	2	—	2	—	2	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

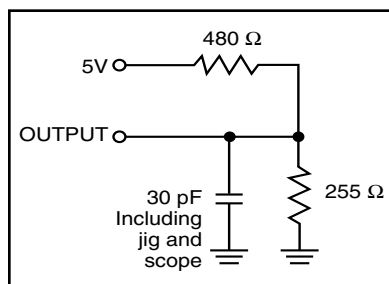
**AC TEST LOADS**


Figure 1

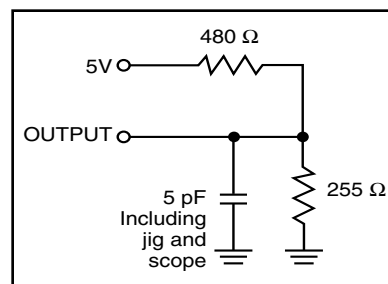
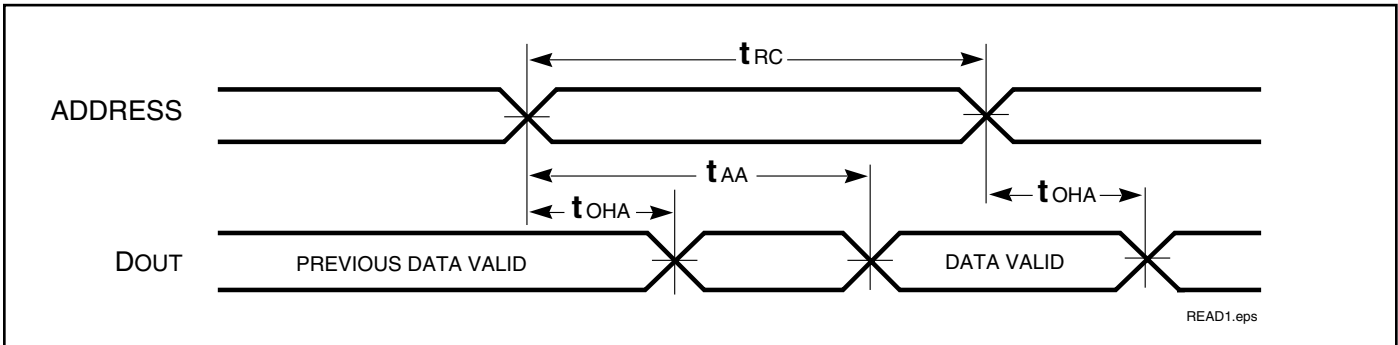
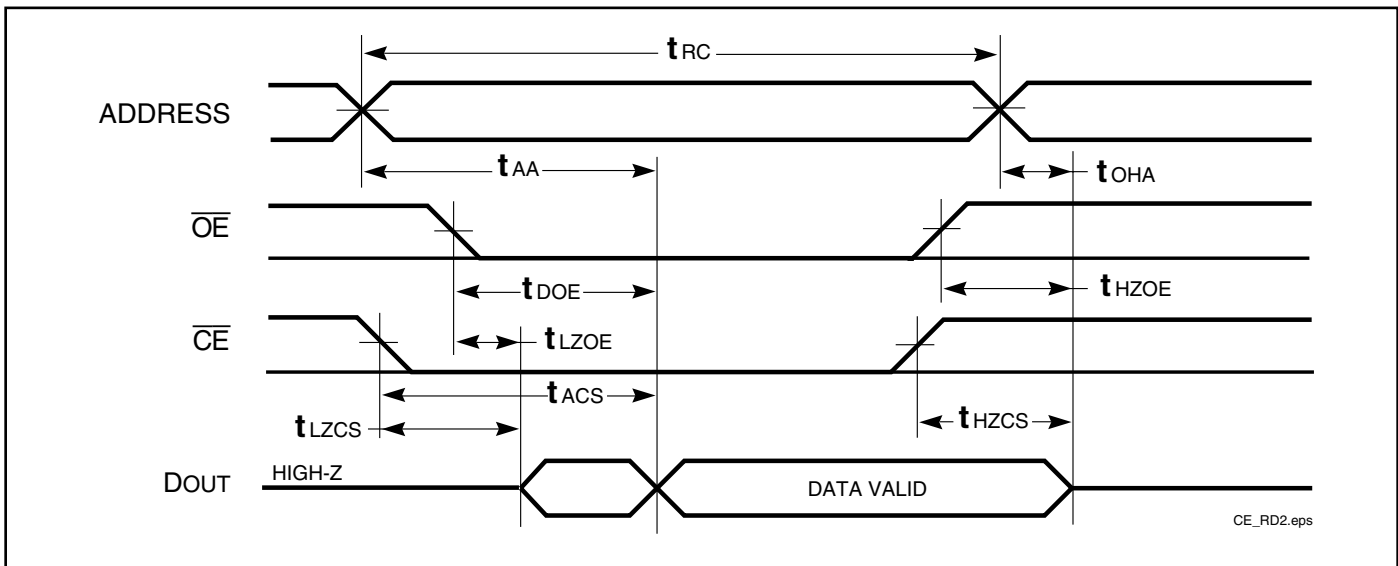


Figure 2

**AC WAVEFORMS**  
**READ CYCLE NO. 1<sup>(1,2)</sup>**



**READ CYCLE NO. 2<sup>(1,3)</sup>**



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

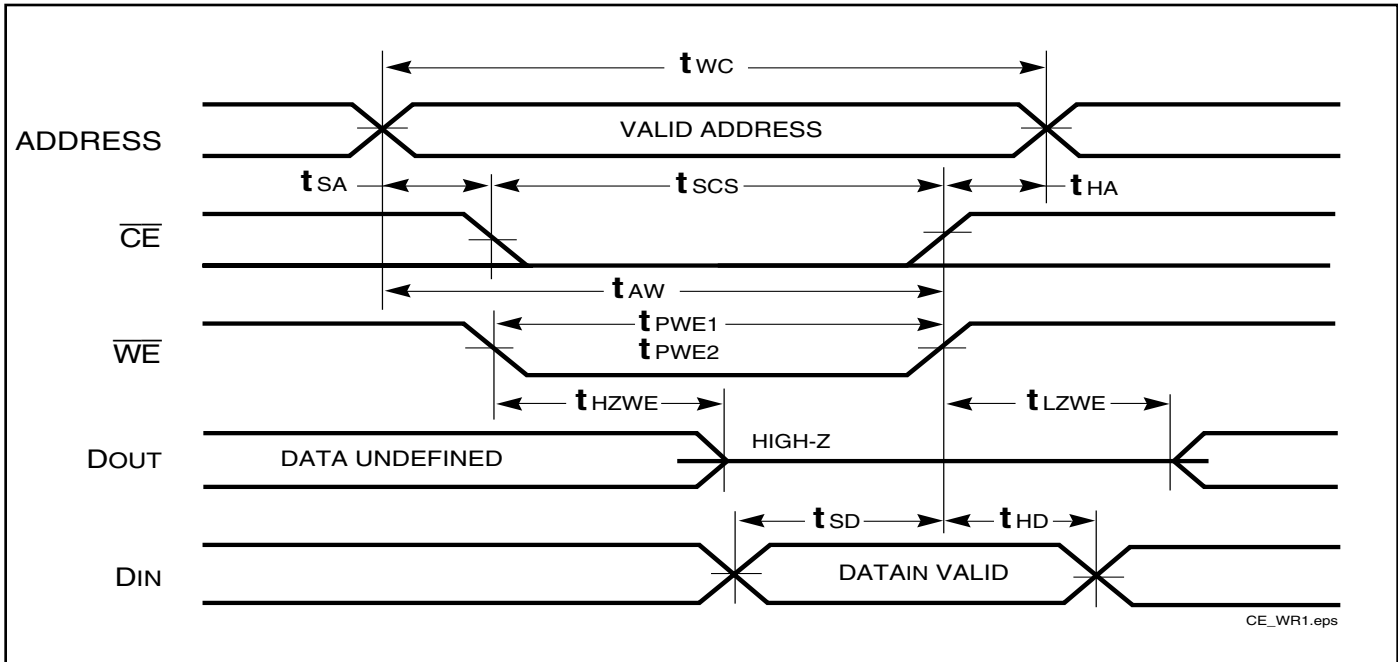
**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup> (Over Operating Range)**

Symbol	Parameter	-10		-12		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time	10	—	12	—	25	—	ns
t <sub>sce</sub>	$\overline{CE}$ to Write End	7	—	9	—	18	—	ns
t <sub>aw</sub>	Address Setup Time to Write End	7	—	9	—	18	—	ns
t <sub>ha</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>sa</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>pwe1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ =High)	7	—	9	—	15	—	ns
t <sub>pwe2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ =Low)	7	—	9	—	15	—	ns
t <sub>sd</sub>	Data Setup to Write End	6	—	6	—	15	—	ns
t <sub>hd</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>hzwe</sub> <sup>(2)</sup>	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	15	ns
t <sub>lzwe</sub> <sup>(2)</sup>	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

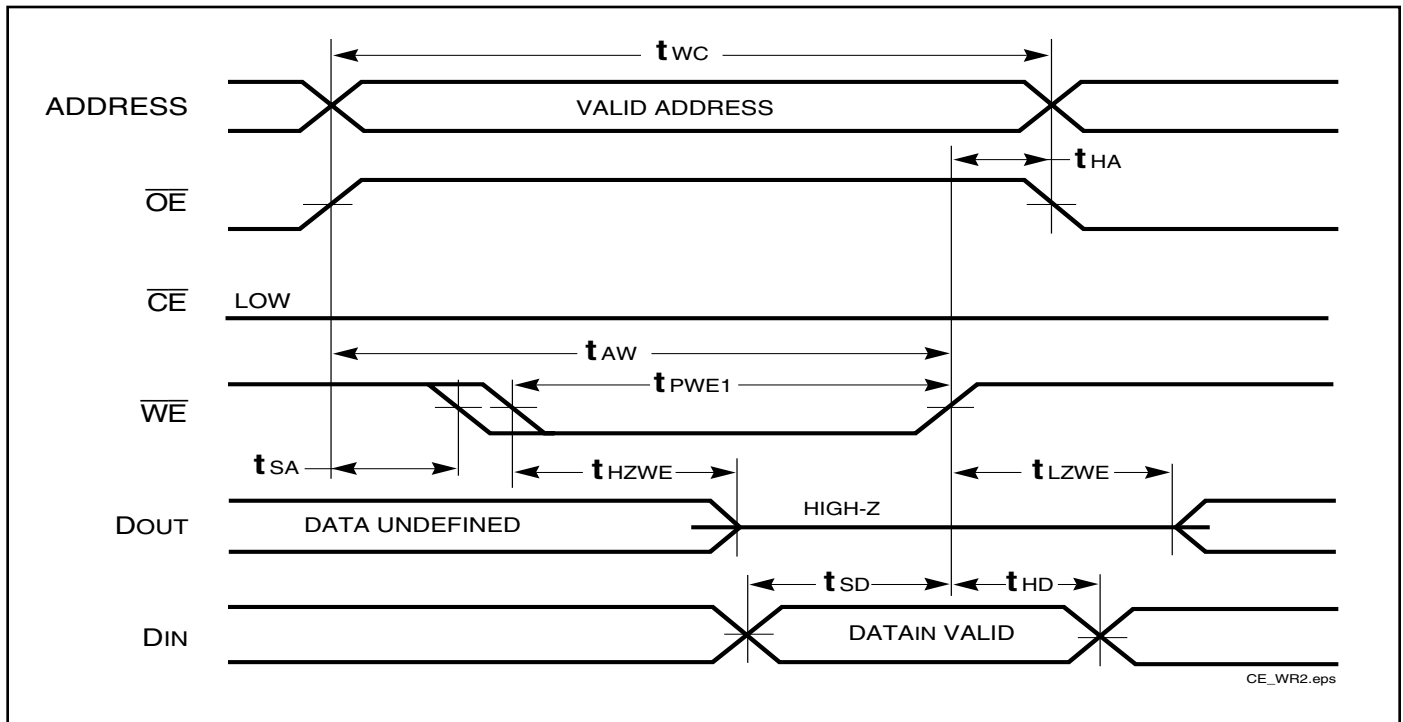


**AC WAVEFORMS**
**WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**

**Notes:**

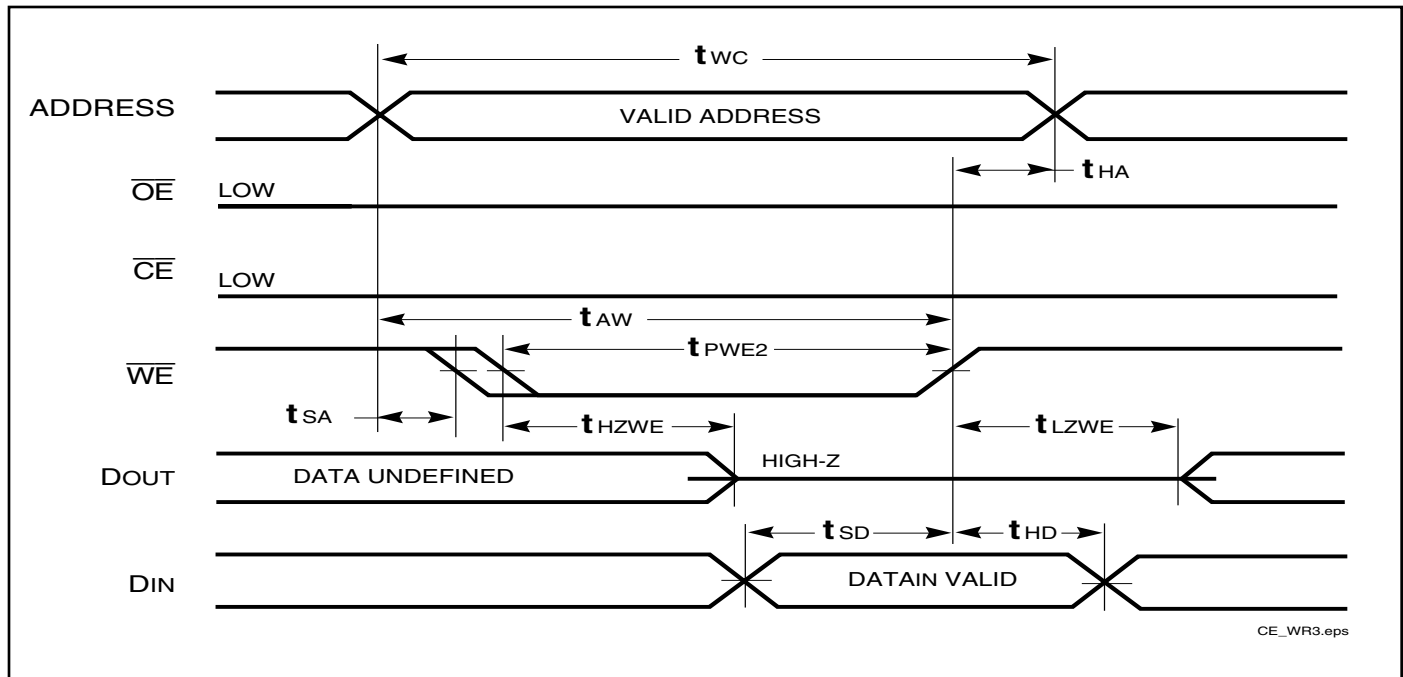
1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

# IS61C5128AL/AS IS64C5128AL/AS

## WRITE CYCLE NO. 2 ( $\overline{OE}$ is HIGH During Write Cycle) <sup>(1,2)</sup>



## WRITE CYCLE NO. 3 ( $\overline{OE}$ is LOW During Write Cycle) <sup>(1)</sup>



**Notes:**

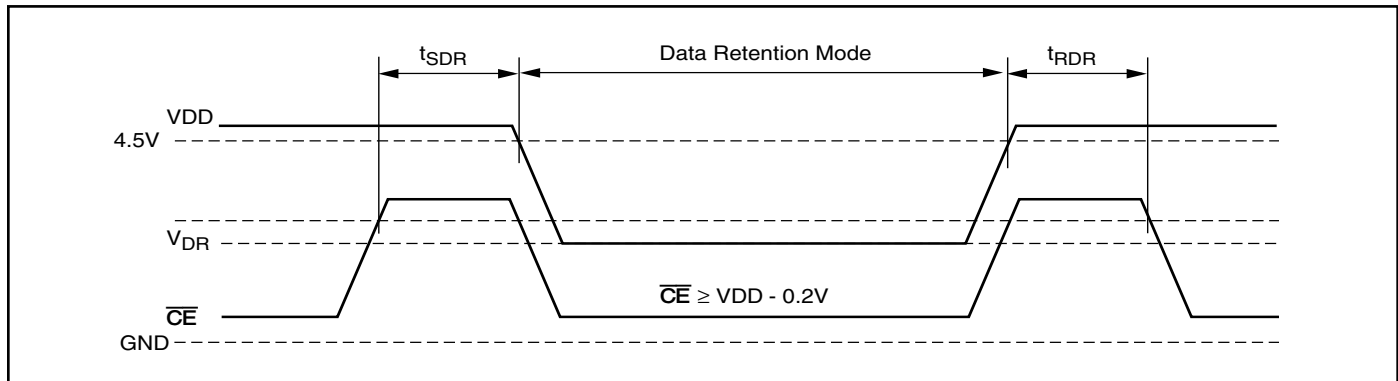
1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

**DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61/64C5128AL)**

Symbol	Parameter	Test Condition	Min.	Max.	Unit	
$V_{DR}$	$V_{DD}$ for Data Retention	See Data Retention Waveform	2.9	5.5	V	
$I_{DR}$	Data Retention Current	$V_{DD} = 2.9V, \overline{CE} \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V, \text{ or } V_{IN} \leq V_{SS} + 0.2V$	Com.	—	8	mA
			Ind.	—	10	
			Auto. typ. <sup>(1)</sup>	—	15	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform	0	—	ns	
$t_{RDR}$	Recovery Time	See Data Retention Waveform	$t_{RC}$	—	ns	

**Note:**

1. Typical Values are measured at  $V_{DD} = 5V, T_A = 25^\circ C$  and not 100% tested.

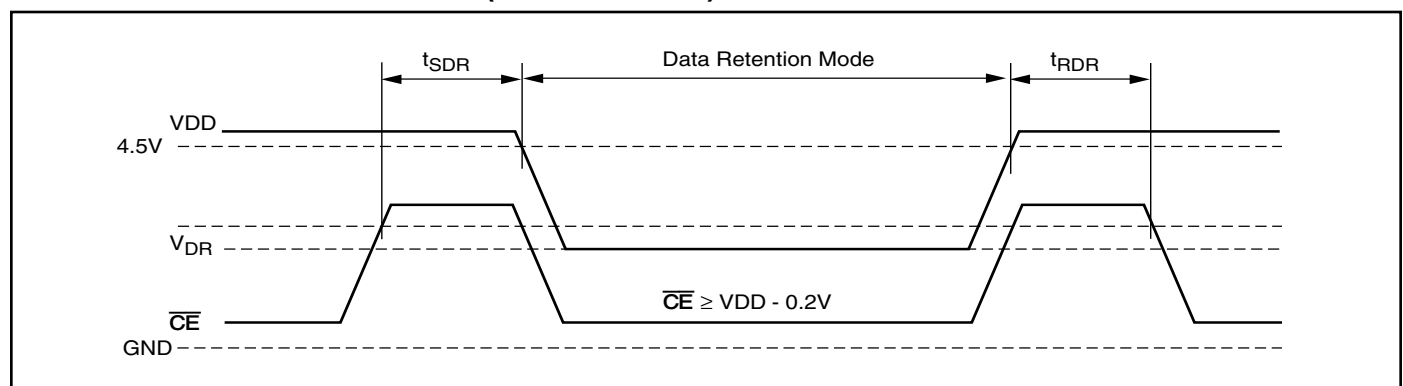
**DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)**


**DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61/64C5128AS)**

Symbol	Parameter	Test Condition	Min.	Max.	Unit	
$V_{DR}$	$V_{DD}$ for Data Retention	See Data Retention Waveform	2.9	5.5	V	
$I_{DR}$	Data Retention Current	$V_{DD} = 2.9V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.8	mA
		$V_{IN} \geq V_{DD} - 0.2V, \text{ or } V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	0.9	
			Auto. typ. <sup>(1)</sup>	—	2	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform	0	—	ns	
$t_{RDR}$	Recovery Time	See Data Retention Waveform	$t_{RC}$	—	ns	

**Note:**

1. Typical Values are measured at  $V_{DD} = 5V, T_A = 25^\circ C$  and not 100% tested.

**DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)**




## IS61C5128AL/AS IS64C5128AL/AS

### HIGH SPEED (IS61/64C5128AL)

#### ORDERING INFORMATION

##### Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61C5128AL-10KLI	400-mil Plastic SOJ, Lead-free
	IS61C5128AL-10TLI	44-pin TSOP-II, Lead-free

##### Automotive Range: -40°C to +125°C

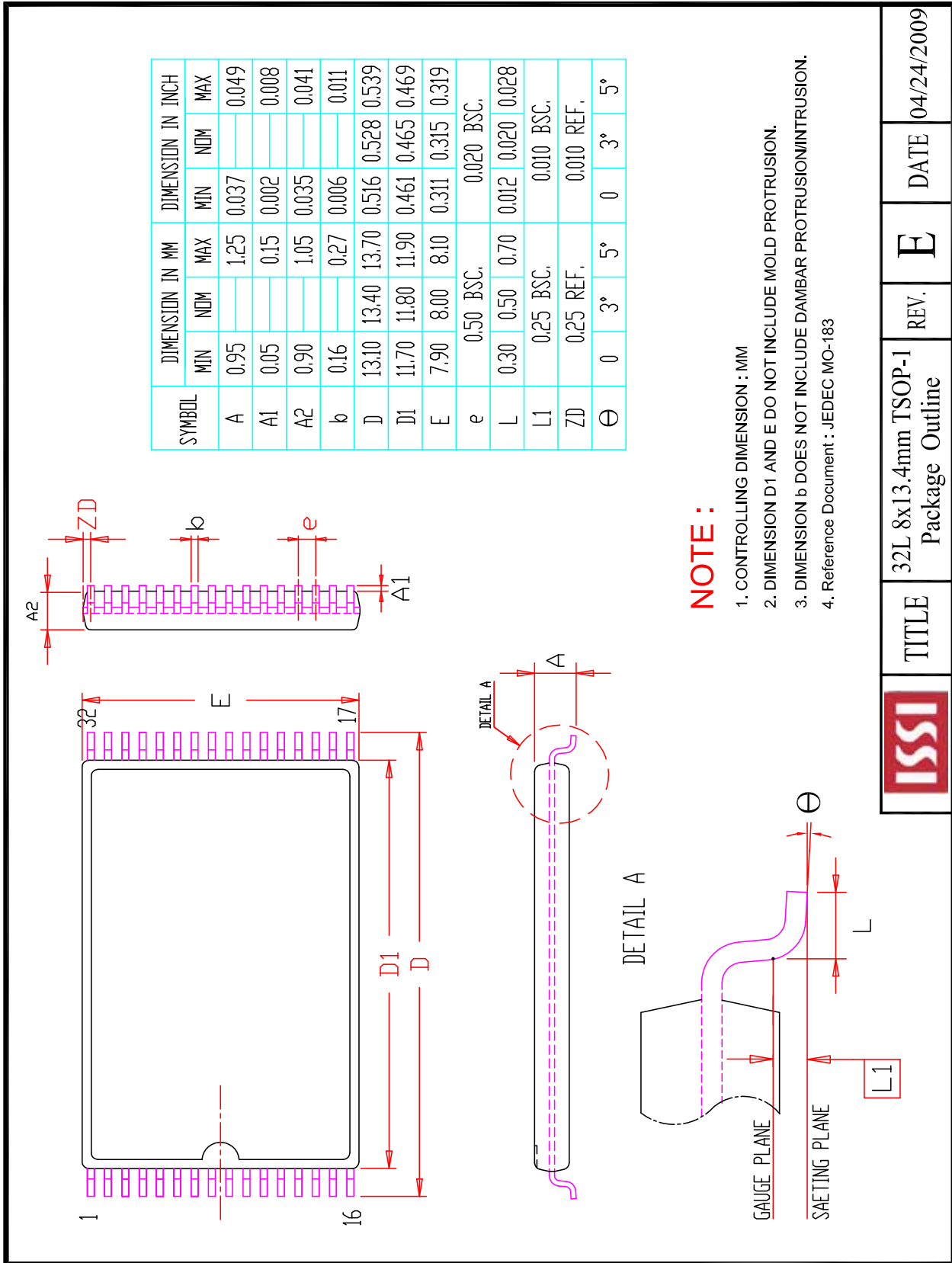
Speed (ns)	Order Part No.	Package
12	IS64C5128AL-12KLA3	400-mil Plastic SOJ, Lead-free
	IS64C5128AL-12CTLA3	44-pin TSOP-II, Lead-free, Copper Leadframe

### LOW POWER (IS61/64C5128AS)

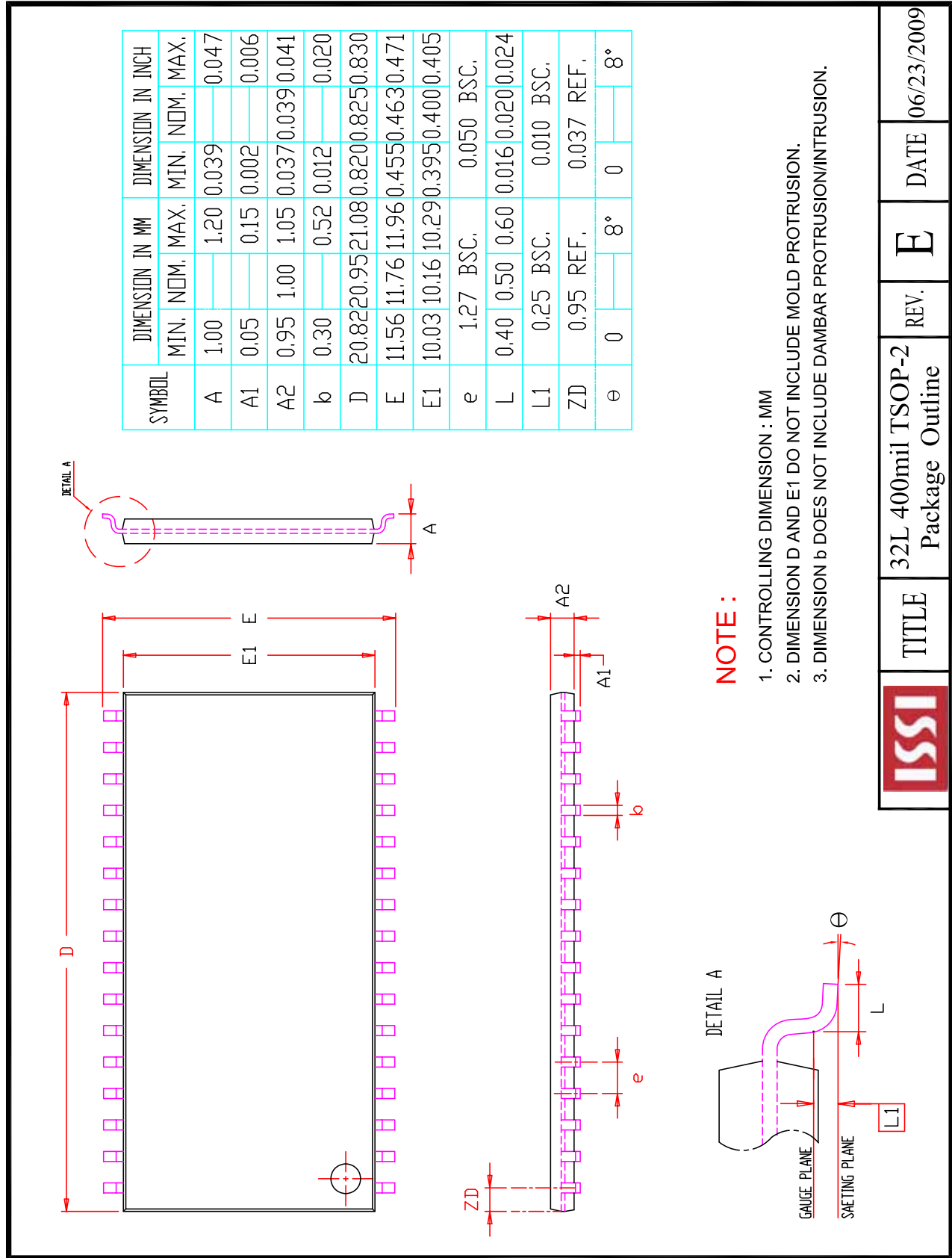
#### ORDERING INFORMATION

##### Industrial Range: -40°C to +85°C

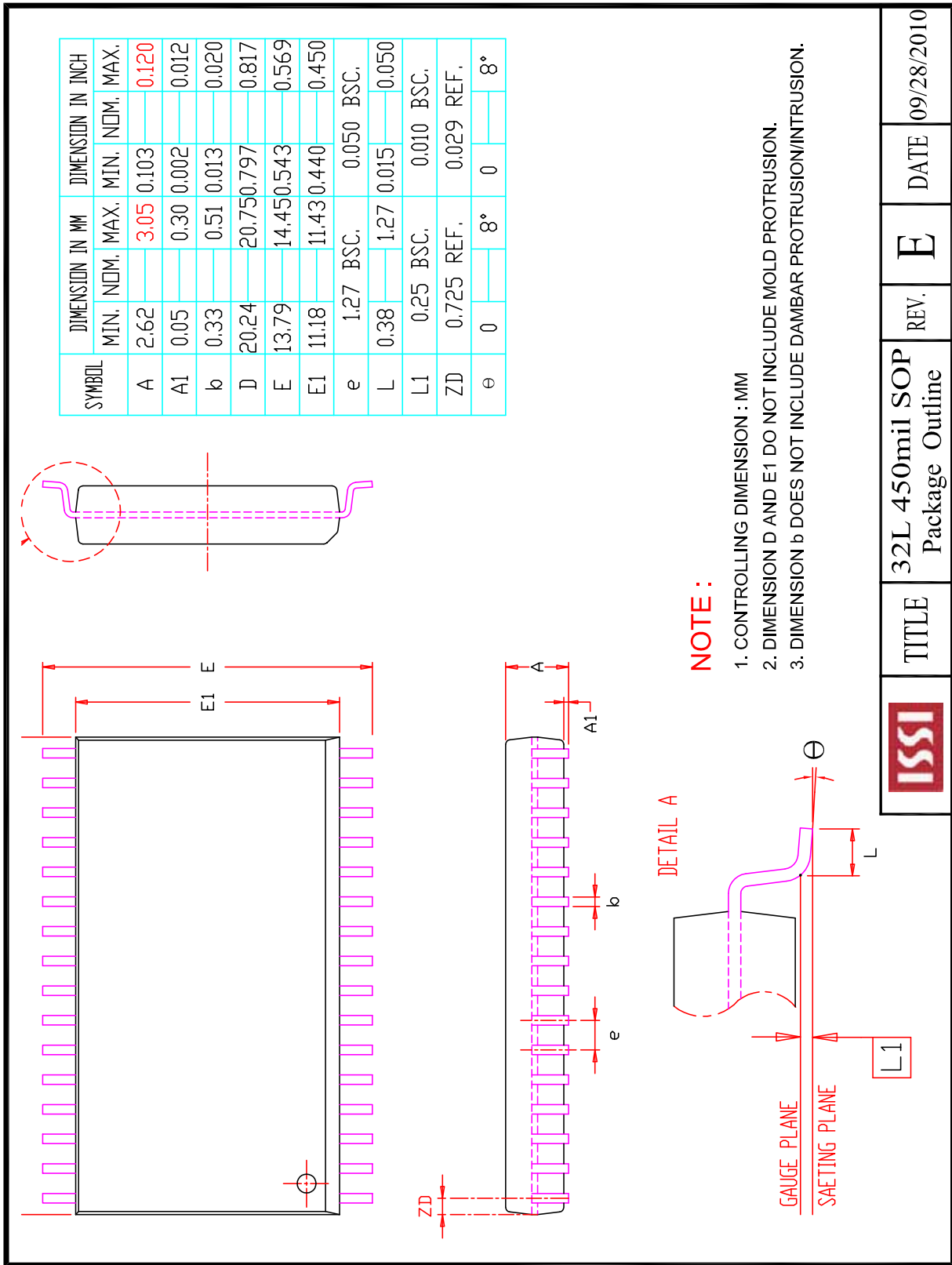
Speed (ns)	Order Part No.	Package
25	IS61C5128AS-25QLI	450-mil Plastic SOP, Lead-free
	IS61C5128AS-25HLI	32-pin STSOP-I, Lead-free
	IS61C5128AS-25TLI	32-pin TSOP-II, Lead-free



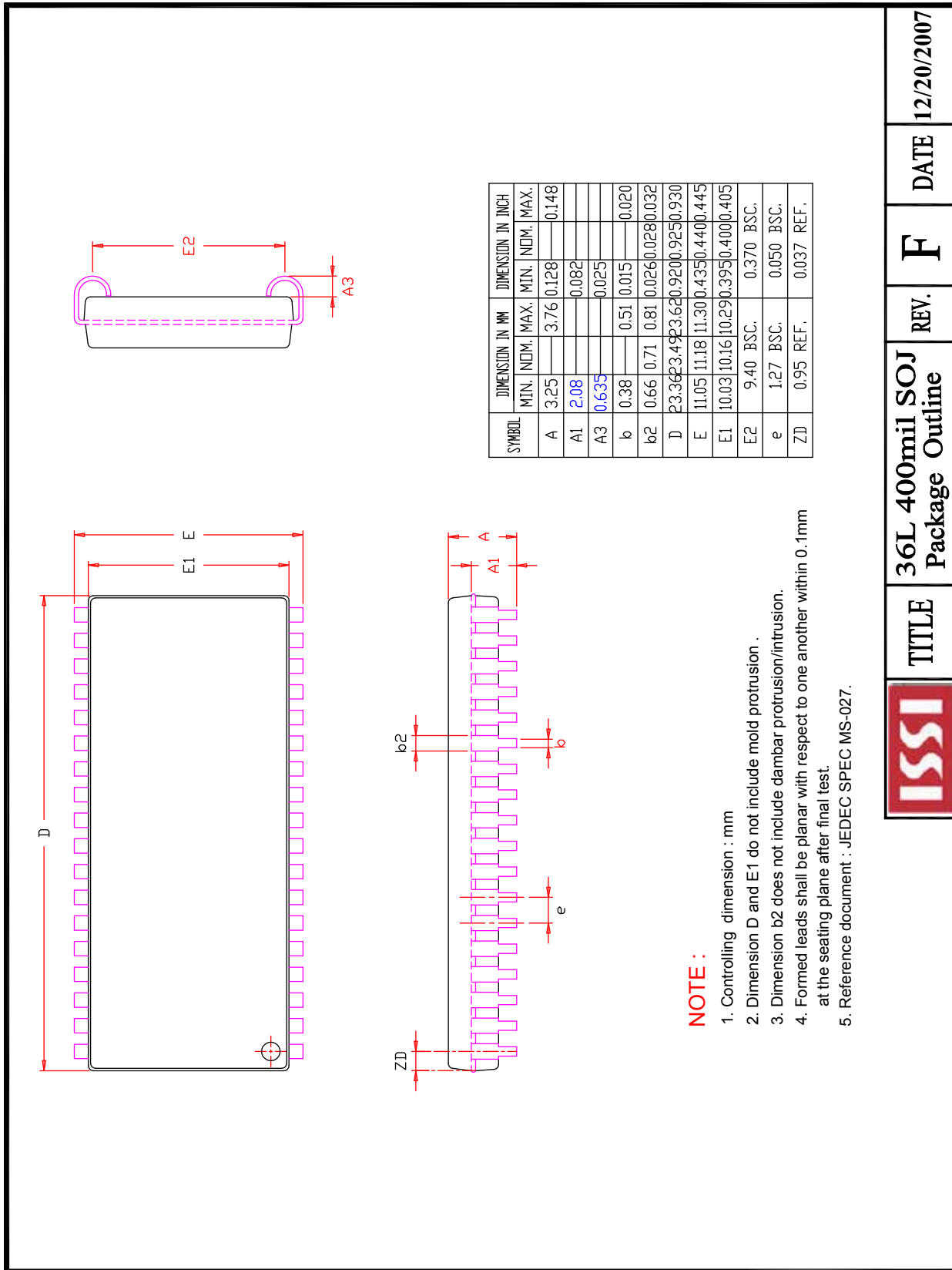
	TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	E	DATE	04/24/2009
--	-------	-------------------------------------	------	---	------	------------



	TITLE	32L 400mil TSOP-2 Package Outline	REV.	E	DATE	06/23/2009
--	-------	--------------------------------------	------	---	------	------------







**TITLE**

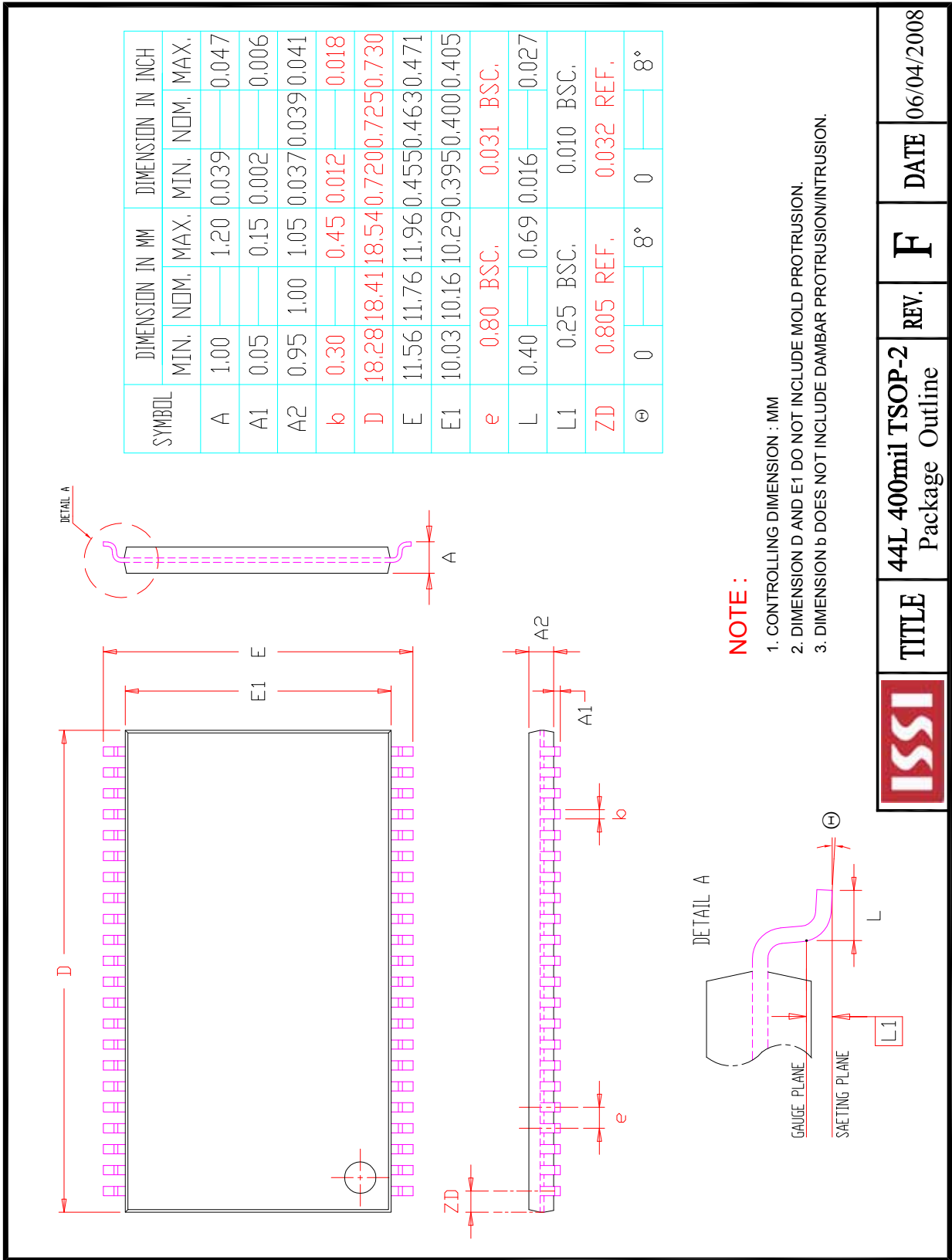
**36L 400mil SOJ  
Package Outline**

**REV.**

**F**

**DATE**

**12/20/2007**



	<b>TITLE</b>	<b>REV.</b>	<b>DATE</b>
	44L 400mil TSOP-2 Package Outline	F	06/04/2008

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ISSI:](#)

[IS61C5128AL-10KLI](#) [IS61C5128AL-10KLI-TR](#) [IS61C5128AS-25QLI](#) [IS61C5128AS-25QLI-TR](#) [IS61C5128AS-25TLI](#)  
[IS61C5128AS-25TLI-TR](#) [IS61C5128AL-10TLI](#) [IS61C5128AL-10TLI-TR](#) [IS61C5128AS-25HLI](#) [IS61C5128AS-25HLI-TR](#)