Control plane applications tend to be more sequential in nature and thus lose scaling efficiency with increasing number of threads or cores. Both P2 devices, with their low power, efficient dual-issue out-of-order e500 core, Power Architecture technology and high 1.2 GHz frequency, offer a level of single-threaded performance that is suitable for control plane applications.

The networking linecard requires an optimal combination of good performance to manage a large amount of control plane traffic balanced against low power and cost. With convenient I/O, flexible core configurations and an onboard security block, the P2010 and P2020 processors are well-suited for this application, which involves controlling ASICs, managing exceptions and routing table maintenance.

The P2010 and P2020 processors are also well-suited for LTE and WiMAX channel card applications. With dual-core performance in single-core power budgets, the P2 devices facilitate the "flattening" of the wireless network hierarchy. The dual Serial RapidIO interfaces allow direct connection to the DSPs (such as the MSC8156 DSP) that implement layer 1 processing as well as redundant backplane connections.

Technical Specifications

- Dual (P2020) or single (P2010) high-performance Power Architecture e500 cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 800 MHz to 1.2 GHz clock frequency
- 512 KB L2 cache with ECC. Also configurable as SRAM and stashing memory.
- Three 10/100/1000 Mb/s enhanced three-speed Ethernet controllers
  - TCP/IP acceleration and classification capabilities
  - IEEE 1588 support
  - Lossless flow control
  - R/G/MII, R/TBI, SGMII
  - FIFO interfaces
- High-speed interfaces supporting various multiplexing options
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Three PCI Express interfaces
  - Two Serial RapidIO interfaces
  - Two SGMII interfaces
- High-Speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface
  - ULPI interface to PHY
- Enhanced secure digital host controller (SD/MMC)
- Serial peripheral interface
- Integrated security engine (SEC 3.1) (optional)
  - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Kasumi, Snow 3G and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (IPsec, SSL, SRTP, WiMAX)
  - XOR acceleration
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller compliant with OpenPIC standard
- Two four-channel DMA controllers
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller
- 16 general-purpose I/O signals
- Package: 689-pin wirebond power-BGA (TEPBGA2)

Software and Tools Support

- Enea®: Real-time operating system support
- Green Hills®: Complete portfolio of software and hardware development tools, trace tools and real-time operating systems
- Mentor Graphics®: Commercial-grade Linux® solution
- P2020 development system, P2020 reference design board and P2020 COM Express development board

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Document Number: QP20XXFS REV 5 cc

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