

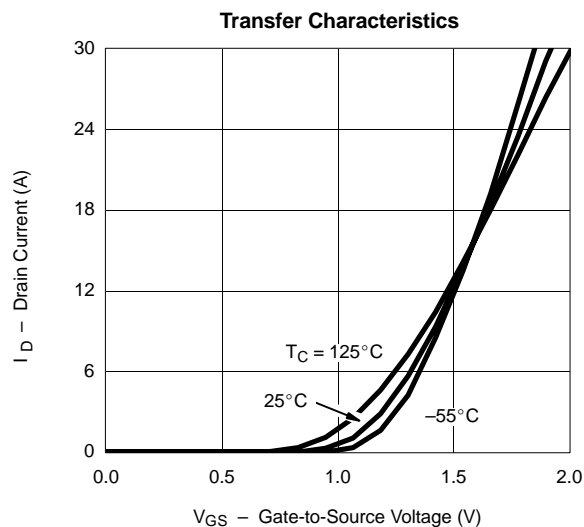
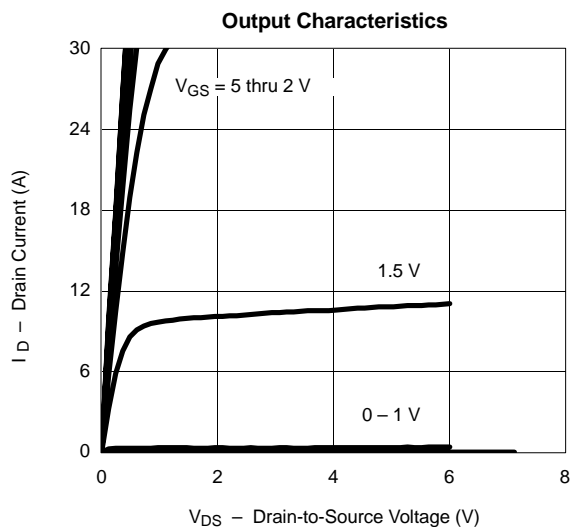
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -7.4 \text{ A}$		0.014	0.017	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -6.3 \text{ A}$		0.018	0.023	Ω
		$V_{GS} = -1.8 \text{ V}, I_D = -5.5 \text{ A}$		0.024	0.032	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -7.4 \text{ A}$		28		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.3 \text{ A}, V_{GS} = 0 \text{ V}$		-0.64	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}, V_{GS} = -5 \text{ V}, I_D = -7.4 \text{ A}$		30.5	50	nC
Gate-Source Charge	Q_{gs}		5.3			
Gate-Drain Charge	Q_{gd}		3.8			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 15 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$		30	50	ns
Rise Time	t_r		30			
Turn-Off Delay Time	$t_{d(off)}$		110			
Fall Time	t_f		65			
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.3 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		45	80	

Notes

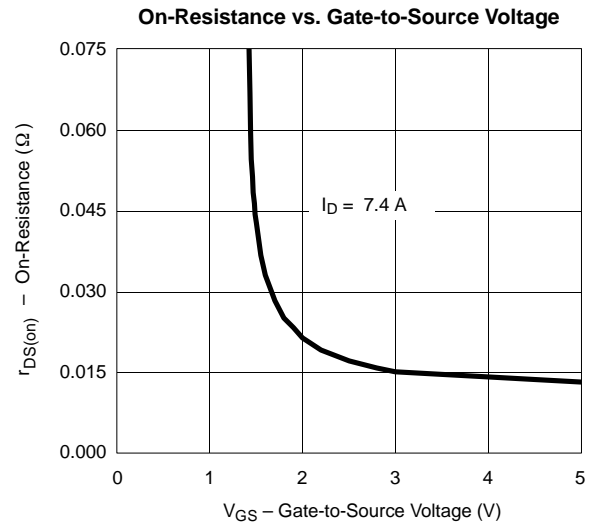
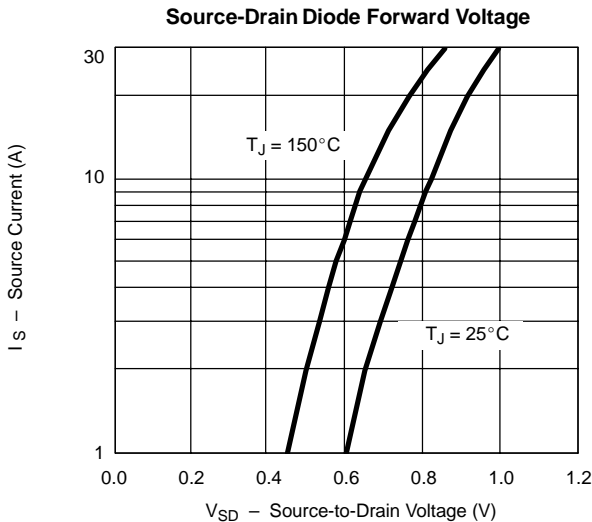
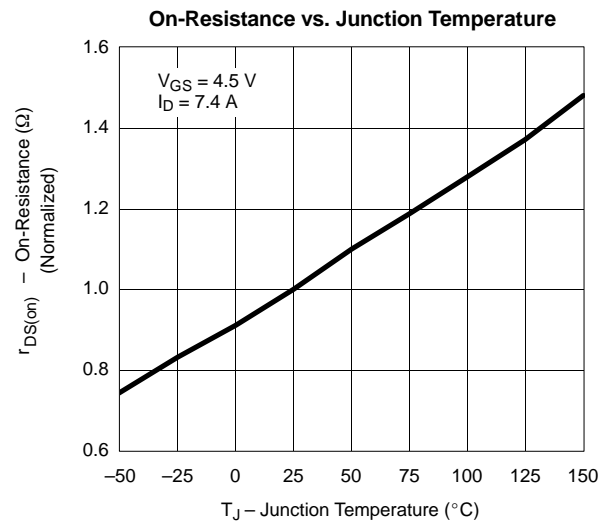
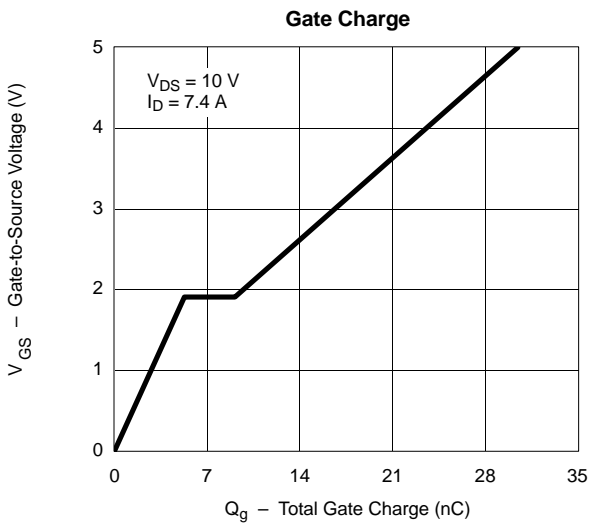
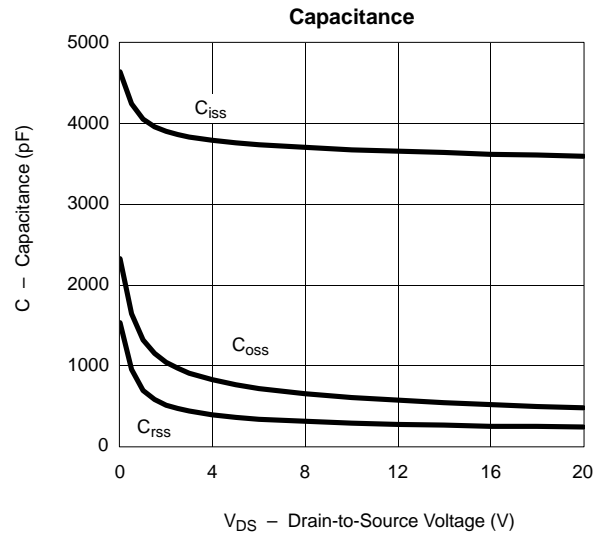
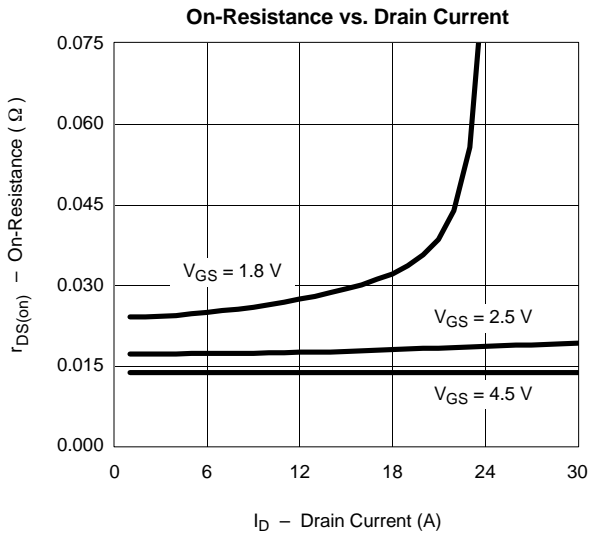
- a Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

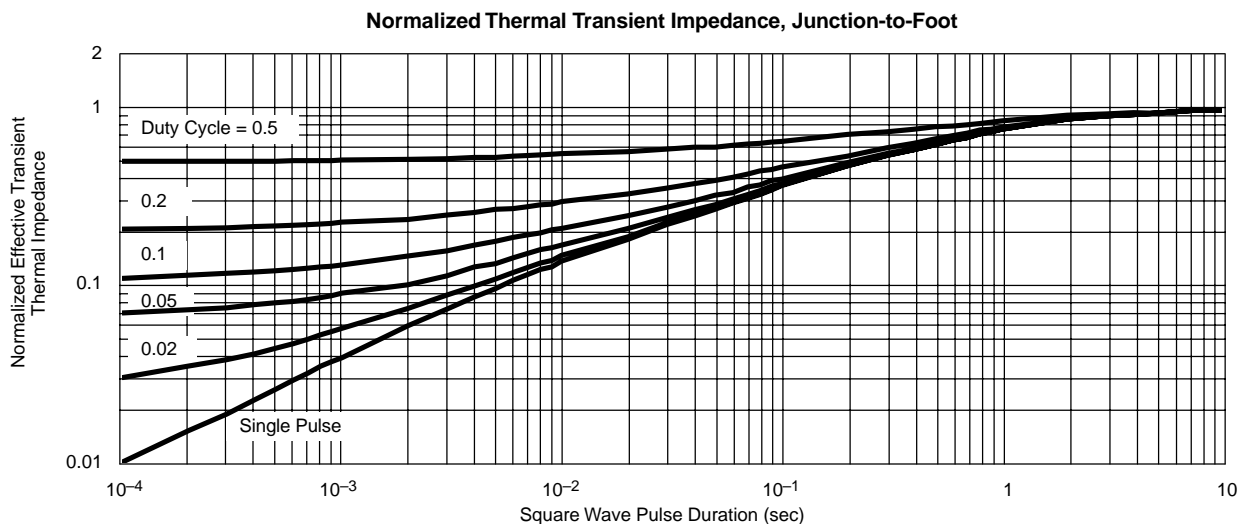
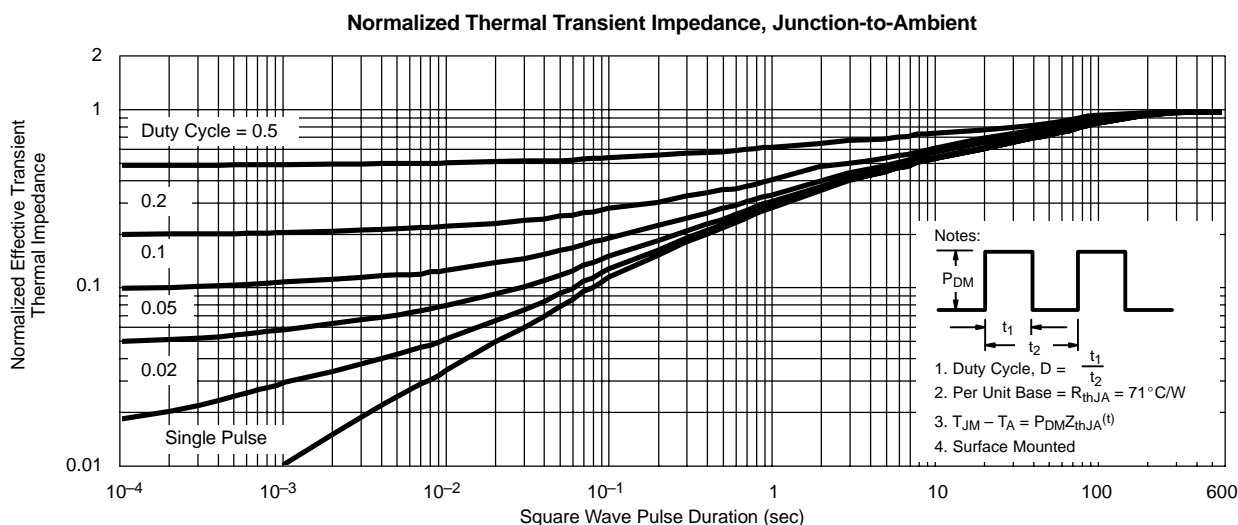
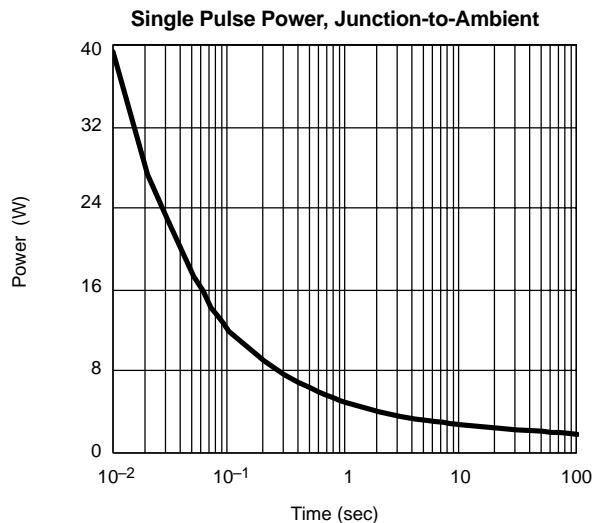
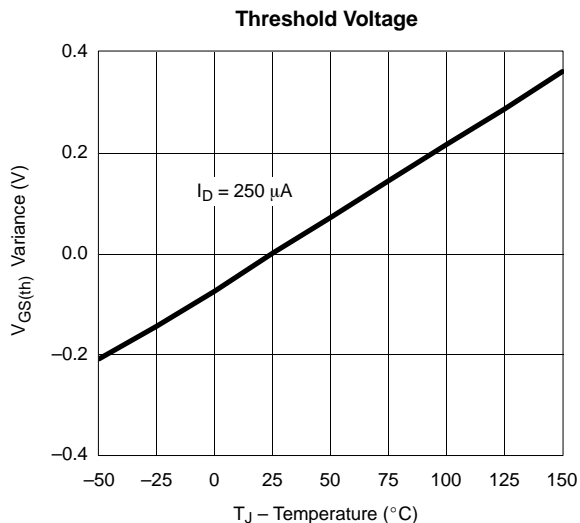




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