PIN DESCRIPTION

Pin No.	Symbol	Description
1	I_{ABCa}	Amplifier Bias Input A
2	D_a	Diode Bias A
3	$+IN_a$	Non-inverted Input A
4	$-IN_a$	Inverted Input A
5	VO_a	Output A
6	V−	Negative Supply
7	$IN_{BUFFERa}$	Buffer Input A
8	$VO_{BUFFERa}$	Buffer Output A
9	$VO_{BUFFERb}$	Buffer Output B
10	$IN_{BUFFERb}$	Buffer Input B
11	V+	Positive Supply
12	VO_b	Output B
13	$-IN_b$	Inverted Input B
14	$+IN_b$	Non-inverted Input B
15	D_b	Diode Bias B
16	I_{ABCb}	Amplifier Bias Input B

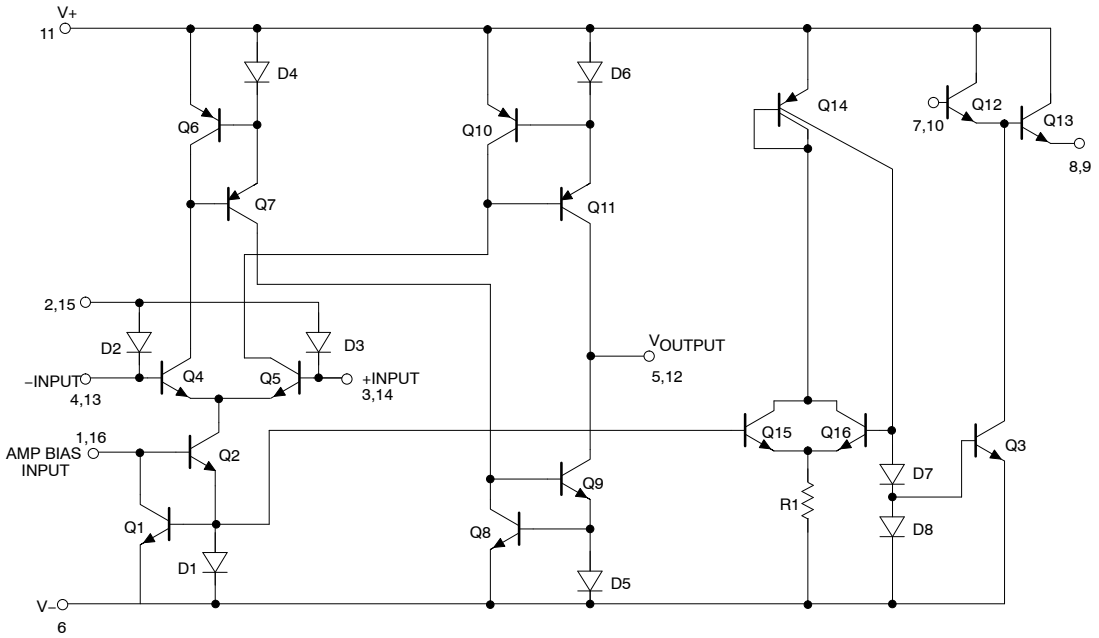
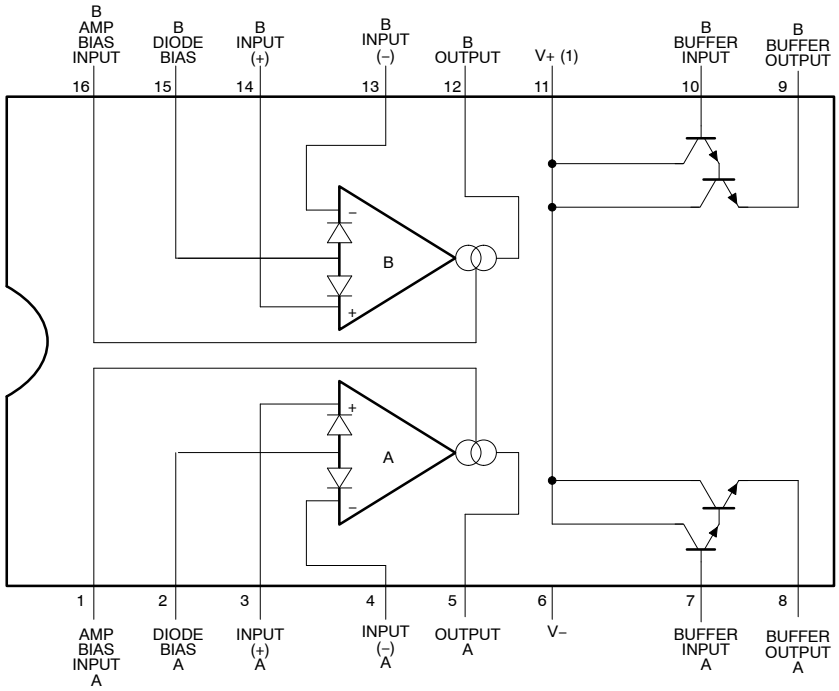


Figure 1. Circuit Schematic



NOTE: V+ of output buffers and amplifiers are internally connected.

Figure 2. Connection Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_S	44 V_{DC} or ±22	V
Power Dissipation, T_{amb} = 25 °C (Still Air) (Note 2)	P_D	1125	mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	140	°C/W
Differential Input Voltage	V_{IN}	±5.0	V
Diode Bias Current	I_D	2.0	mA
Amplifier Bias Current	I_{ABC}	2.0	mA
Output Short-Circuit Duration	I_{SC}	Indefinite	
Buffer Output Current (Note 3)	I_{OUT}	20	mA
Operating Temperature Range	T_{amb}	0 °C to +70 °C	°C
Operating Junction Temperature	T_J	150	°C
DC Input Voltage	V_{DC}	$+V_S$ to $-V_S$	
Storage Temperature Range	T_{stg}	–65 °C to +150 °C	°C
Lead Soldering Temperature (10 sec max)	T_{sld}	230	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For selections to a supply voltage above ±22 V, contact factory.
2. The following derating factors should be applied above 25 °C
   D package at 7.1 mW/°C.
3. Buffer output current should be limited so as to not exceed package dissipation.

ELECTRICAL CHARACTERISTICS (Note 4)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	 Overtemperature Range I_{ABC} 5.0 μA	V_{OS}		0.4 0.3	5.0 5.0	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of Input Offset Voltage			7.0		μV/°C
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA			0.5	5	mV
Input Offset Change	5.0 μA ≤ I_{ABC} ≤ 500 μA	V_{OS}		0.1		mV
Input Offset Current		I_{OS}		0.1	0.6	μA
$\Delta I_{OS}/\Delta T$	Avg. TC of Input Offset Current			0.001		μA/°C
Input Bias Current	 Overtemperature Range	I_{BIAS}		0.4 1.0	5.0 8.0	μA
$\Delta I_B/\Delta T$	Avg. TC of Input Current			0.01		μA/°C
Forward Transconductance	 Overtemperature Range	g_M	6700 5400	9600	13000	μmho
g_M Tracking				0.3		dB
Peak Output Current	R_L = 0, I_{ABC} = 5.0 μA R_L = 0, I_{ABC} = 500 μA R_L = 0, Overtemperature Range	I_{OUT}	 350 300	5.0 500	 650	μA
Peak Output Voltage Positive Negative	 R_L = ∞, 5.0 μA ≤ I_{ABC} ≤ 500 μA R_L = ∞, 5.0 μA ≤ I_{ABC} ≤ 500 μA	V_{OUT}	 +12 −12	 +14.2 −14.4		V
Supply Current	I_{ABC} = 500 μA, both channels	I_{CC}		2.6	4.0	mA
V_{OS} Sensitivity Positive Negative	 Δ V_{OS}/Δ V+ Δ V_{OS}/Δ V−			 20 20	 150 150	μV/V
Common-mode Rejection Ration		CMRR	80	110		dB
Common-mode Range			±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz			100		dB
Differential Input Current	I_{ABC} = 0, Input = ±4.0 V	I_{IN}		0.02	100	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)			0.2	100	nA
Input Resistance		R_{IN}	10	26		kΩ
Open-loop Bandwidth		B_W		2.0		MHz
Slew Rate	Unity Gain Compensated	SR		50		V/μs
Buffer Input Current	5	IN_{BUFFER}		0.4	5.0	μA
Peak Buffer Output Voltage	5	VO_{BUFFER}	10			V
ΔV_{BE} of Buffer	Refer to Buffer V_{BE} Test Circuit (Note 6)			0.5	5.0	mV

4. These specifications apply for V_S = ±15 V, T_{amb} = 25°C, amplifier bias current (I_{ABC}) = 500 μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for V_S = ±15 V, I_{ABC} = 500 μA, R_{OUT} = 5.0 kΩ connected from the buffer output to −V_S and the input of the buffer is connected to the transconductance amplifier output.
6. V_S = ±15, R_{OUT} = 5.0 kΩ connected from Buffer output to −V_S and 5.0 μA ≤ I_{ABC} ≤ 500 μA.

TYPICAL PERFORMANCE CHARACTERISTICS

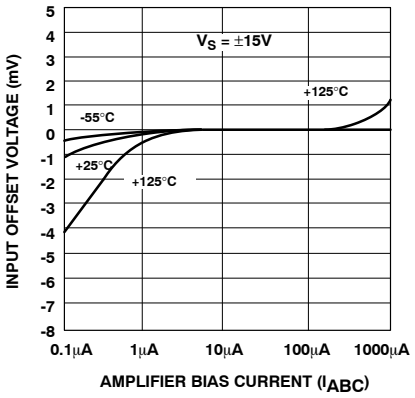


Figure 3. Input Offset Voltage

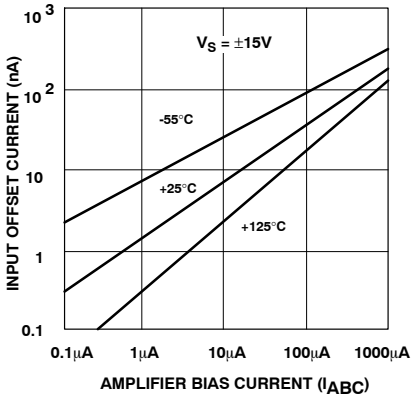


Figure 4. Input Bias Current

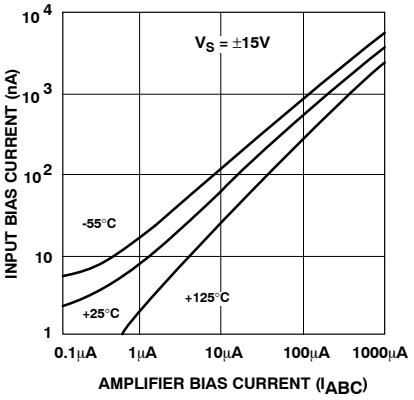


Figure 5. Input Bias Current

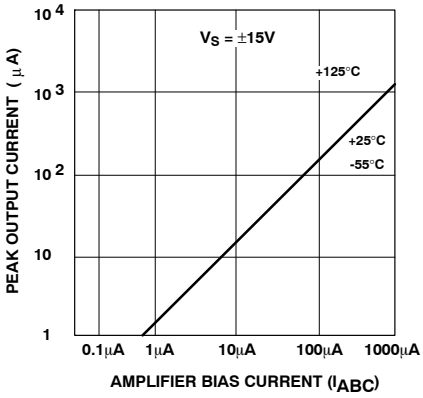


Figure 6. Peak Output Current

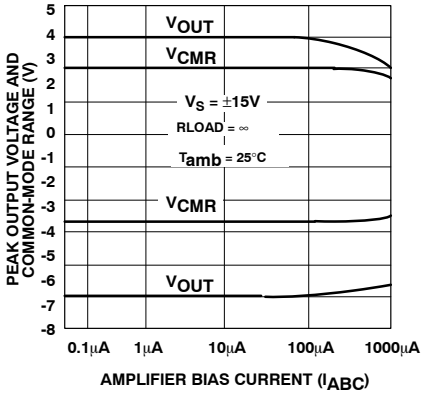


Figure 7. Peak Output Voltage and Common-Mode Range

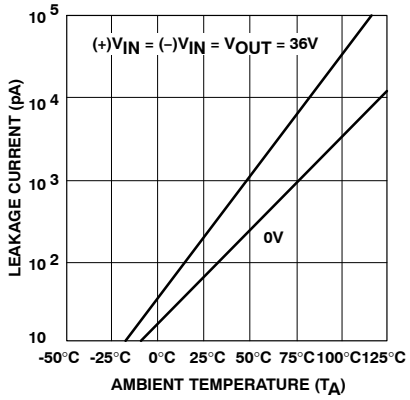


Figure 8. Leakage Current

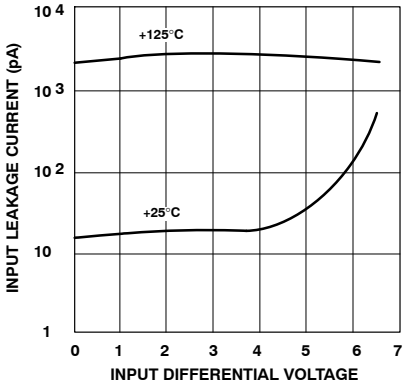


Figure 9. Input Leakage

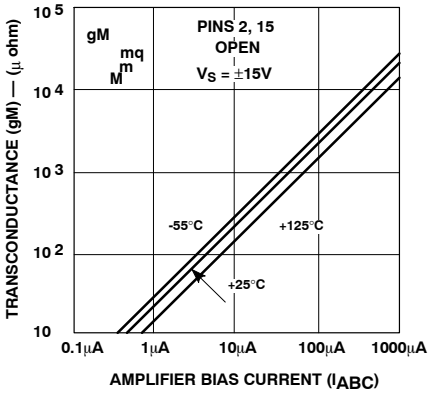


Figure 10. Transconductance

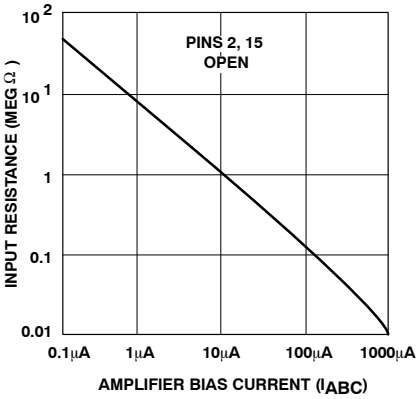


Figure 11. Input Resistance

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

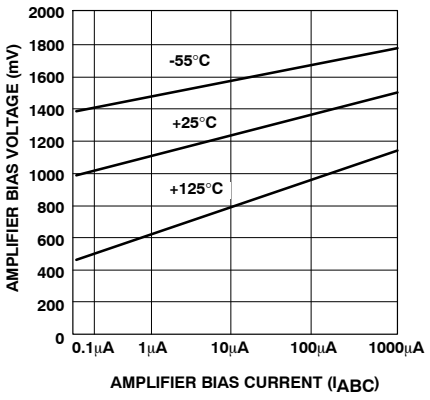


Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

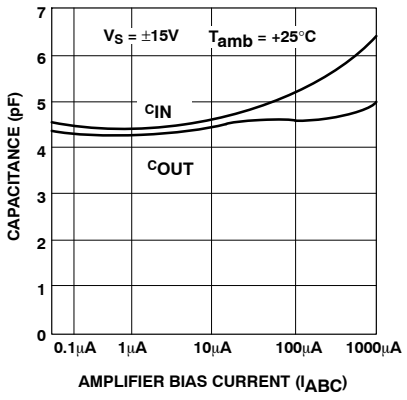


Figure 13. Input and Output Capacitance

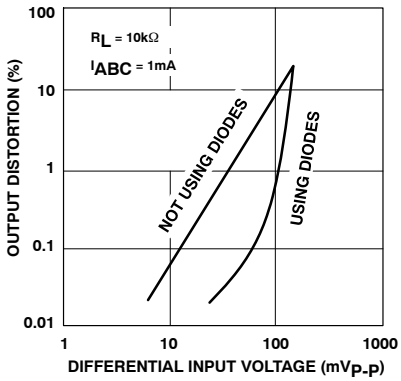


Figure 14. Distortion vs. Differential Input Voltage

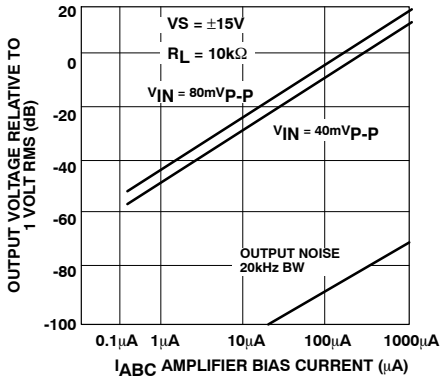


Figure 15. Voltage vs. Amplifier Bias Current

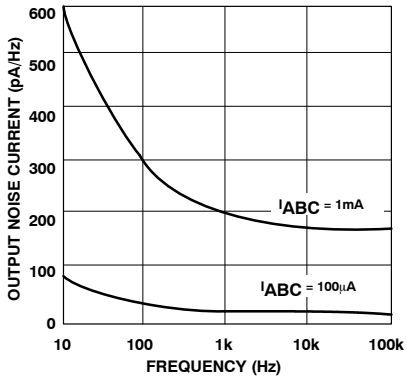


Figure 16. Noise vs. Frequency

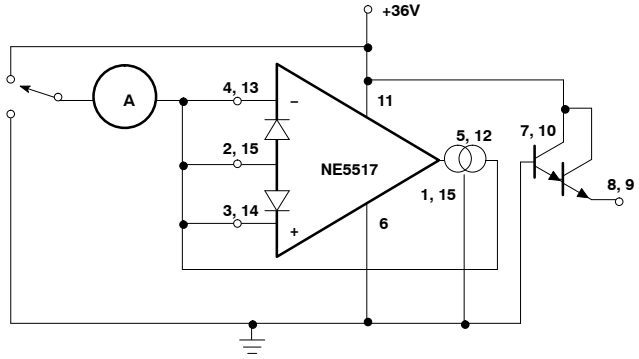


Figure 17. Leakage Current Test Circuit

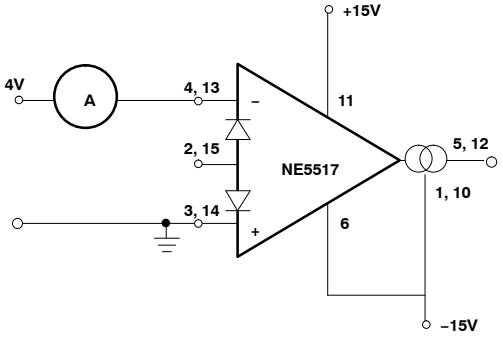


Figure 18. Differential Input Current Test Circuit

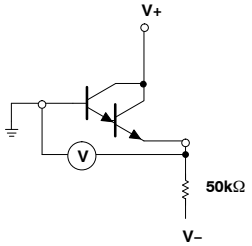


Figure 19. Buffer V_{BE} Test Circuit

APPLICATIONS

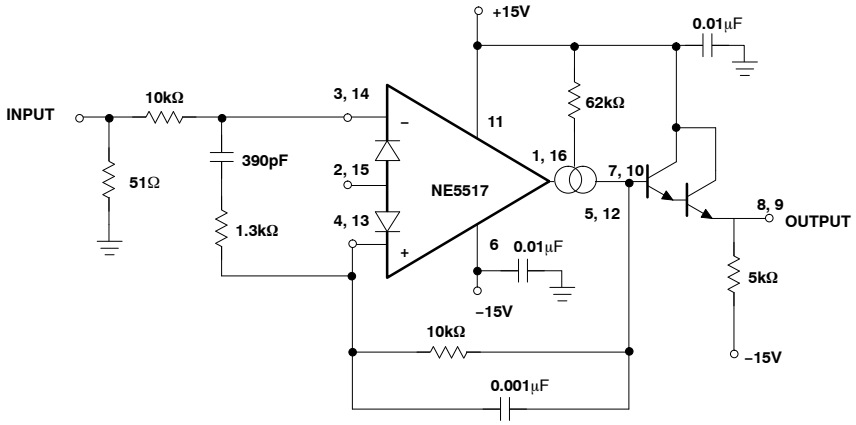


Figure 20. Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

Transconductance Amplifier

The transistor pair, Q_4 and Q_5, forms a transconductance stage. The ratio of their collector currents (I_4 and I_5, respectively) is defined by the differential input voltage, V_{IN}, which is shown in Equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \qquad \text{(eq. 1)}$$

Where V_{IN} is the difference of the two input voltages

$KT \cong 26$ mV at room temperature (300°k).

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \qquad \text{(eq. 2)}$$

If V_{IN} is small, the ratio of I_5 and I_4 will approach unity and the Taylor series of In function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \qquad \text{(eq. 3)}$$

$$\text{and } I_4 \cong I_5 \cong I_B$$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \qquad \text{(eq. 4)}$$

$$I_5 - I_4 = V_{IN} \frac{\left(I_B \frac{q}{}\right)}{2KT}$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN} \left(I_B \frac{q}{2KT} \right) = I_O \qquad \text{(eq. 5)}$$

The term $\frac{\left(I_B \frac{q}{}\right)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

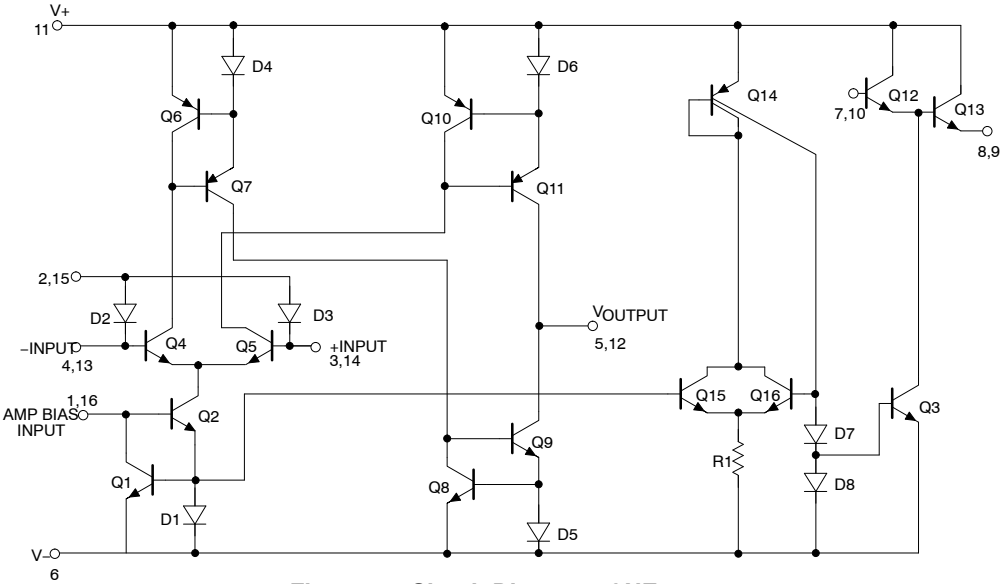


Figure 21. Circuit Diagram of NE5517

Linearizing Diodes

For V_{IN} greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since $I_4 + I_5 = I_B$ and $I_5 - I_4 = I_0$, that is: $I_4 = (I_B - I_0)$, $I_5 = (I_B + I_0)$

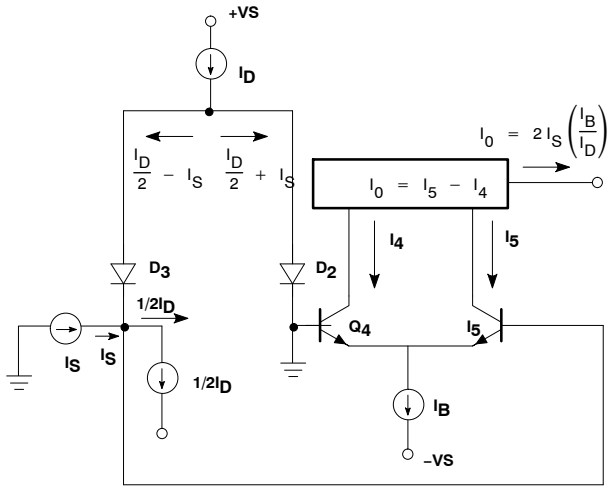


Figure 22. Linearizing Diode

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_O)}{1/2(I_B - I_O)} \qquad \text{(eq. 6)}$$

$$I_O = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I_D.

Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2.0 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 23, the voltage divider R_2, R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

(3) $g_M = 19.2\ I_{ABC}$
(g_M in μmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.

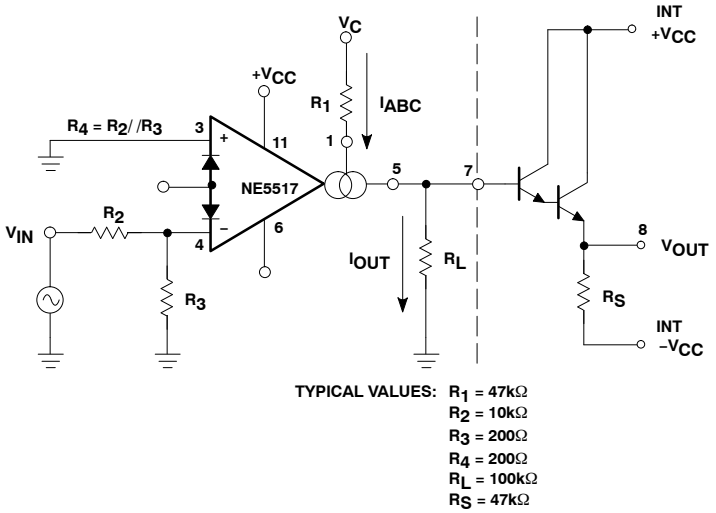


Figure 23.

Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, R_P, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance×input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

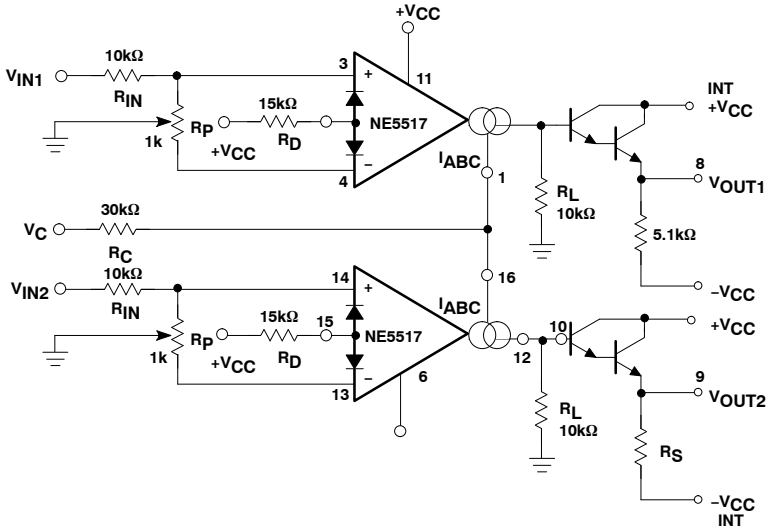


Figure 24. Gain-Controlled Stereo Amplifier

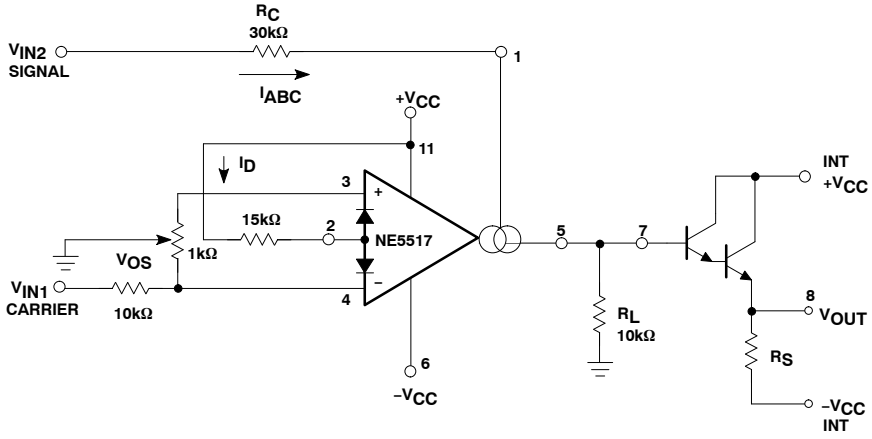


Figure 25. Amplitude Modulator

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 26 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_x = \frac{R + R_A}{g_M + R_A}$$

where g_M is approximately 19.21 μMHOs at room temperature. Figure 27 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 28 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A. Then, the frequency response rolls off at a 6dB per octave with the −3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 29. Higher order filters can be made using additional amplifiers as shown in Figures 30 and 31.

Voltage-Controlled Oscillators

Figure 32 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2.0 Hz to 200 kHz is possible by varying I_{ABC} from 1.0 mA to 10 μA.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5.0 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 33.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1.0 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to −2.0 mA. In this application, however, the current range is set through R_{REF} (10 kΩ) to 0 to −1.0 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA$$

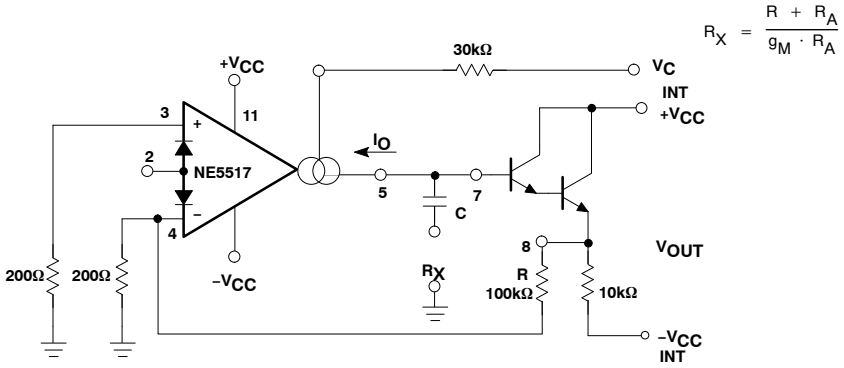


Figure 26. VCR

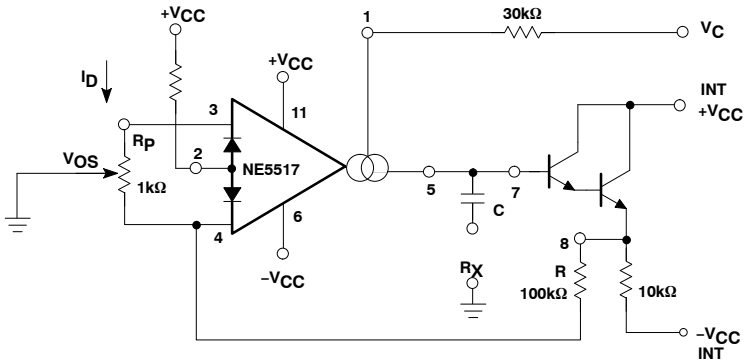
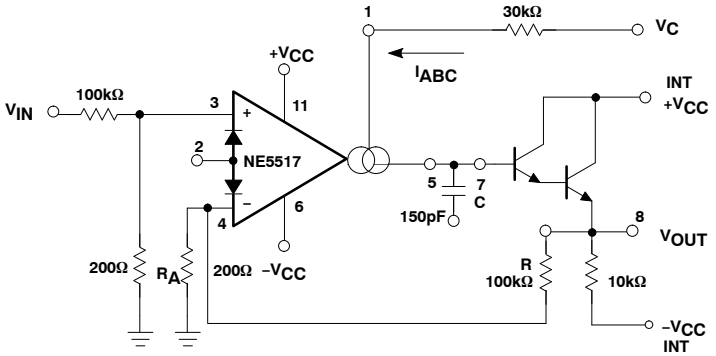


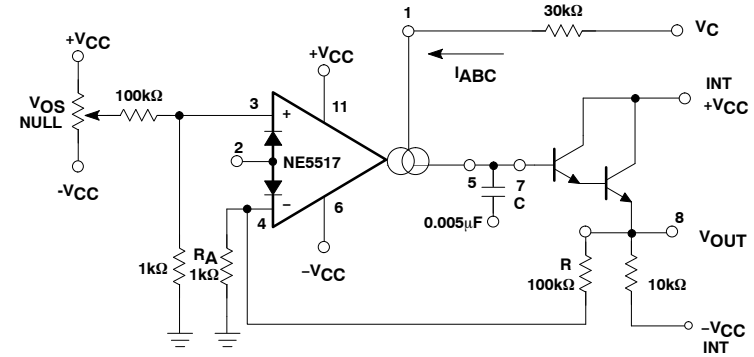
Figure 27. VCR with Linearizing Diodes



NOTE:

$$f_O = \frac{R_A g_M}{g(R + RA)\,2\pi C}$$

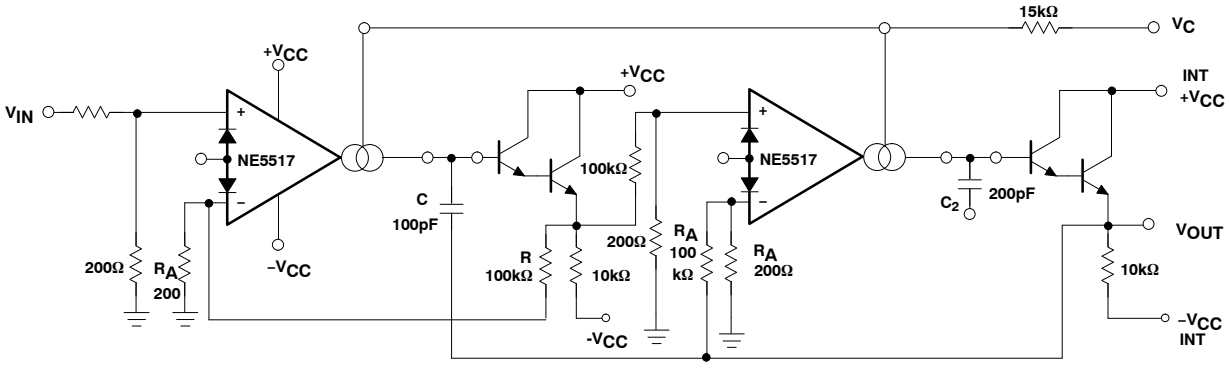
Figure 28. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{g(R + RA)\,2\pi C}$$

Figure 29. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{(R + R_A)\,2\pi C}$$

Figure 30. Butterworth Filter − 2nd Order

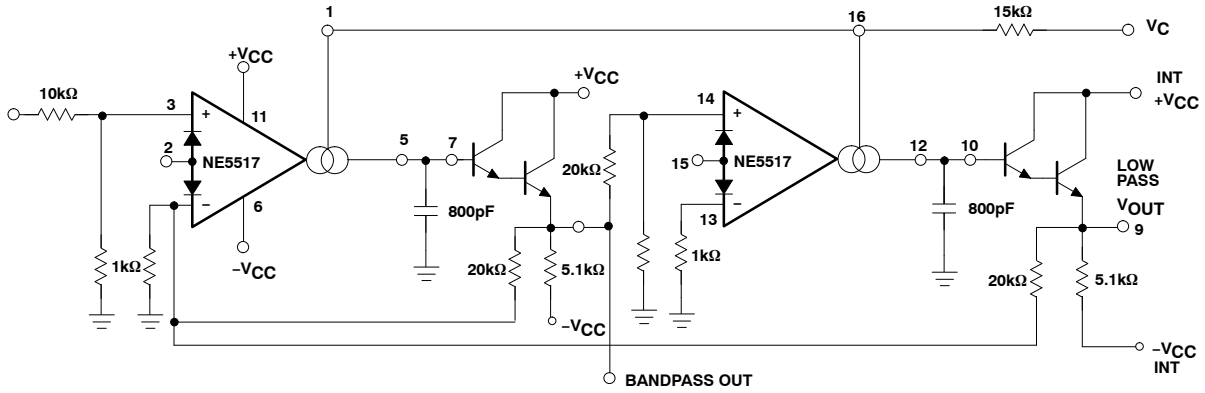


Figure 31. State Variable Filter

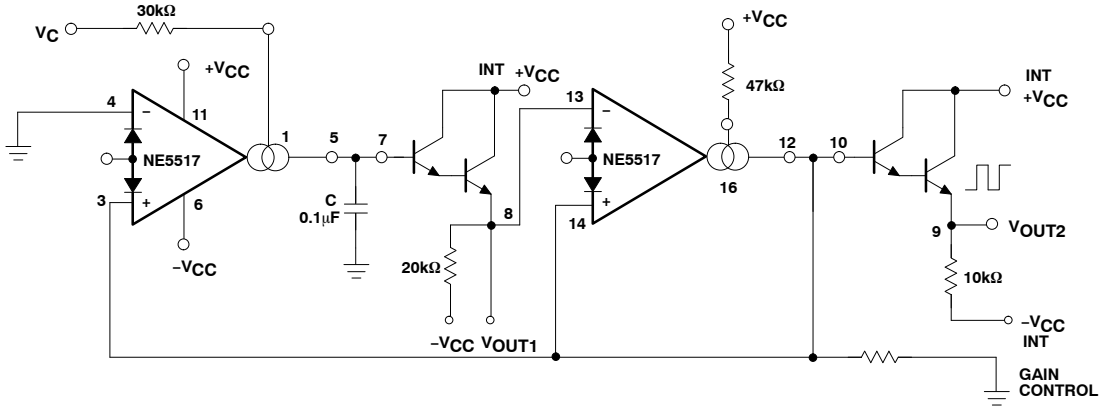
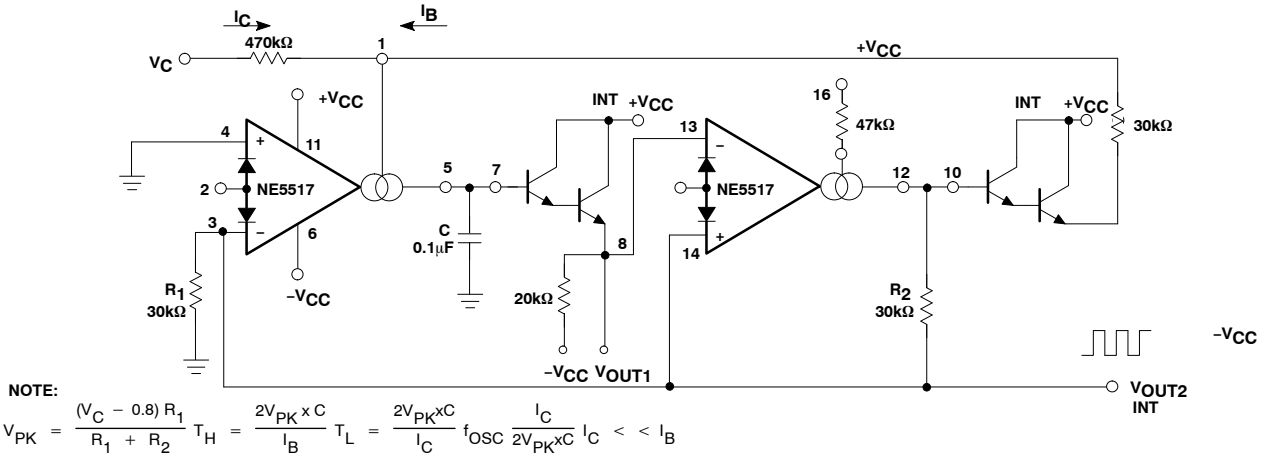


Figure 32. Triangle–Square Wave Generator (VCO)



NOTE:

$$V_{PK} = \frac{(V_C - 0.8)\,R_1}{R_1 + R_2} \quad T_H = \frac{2V_{PK} \times C}{I_B} \quad T_L = \frac{2V_{PK} \times C}{I_C} \quad f_{OSC} \frac{I_C}{2V_{PK} \times C} \quad I_C < < I_B$$

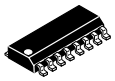
Figure 33. Sawtooth Pulse VCO

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NE5517DR2G	0 to +70 °C	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

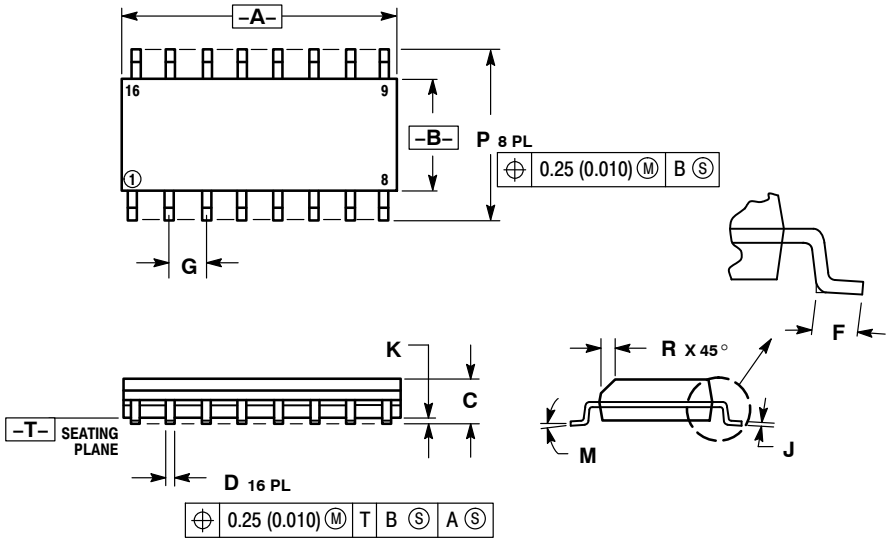
Intel is a registered trademark of Intel Corporation in the U.S. and/or other countries.



SCALE 1:1

SOIC–16
CASE 751B–05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

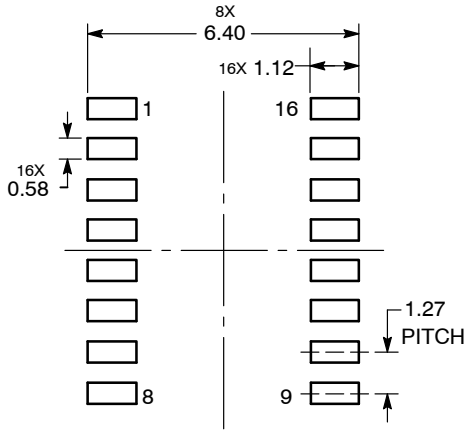
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC–16	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:

NE5517AN NE5517ANG NE5517D NE5517DG NE5517DR2 NE5517DR2G NE5517N NE5517NG AU5517DR2 AU5517DR2G