

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND	-0.5V to 17V
V_{DD} to DGND	-0.5V to 17V
AGND to DGND	-0.5V to $V_{DD} + 0.5V$
DGND to AGND	-0.5V to $V_{DD} + 0.5V$
V_{REF} to AGND,DGND	$\pm 25V$
R_{FB} to AGND,DGND	$\pm 25V$
Digital Inputs to DGND	-0.5V to $V_{DD} + 0.5V$
V_{OUT1} to AGND, DGND	-0.5V to $V_{DD} + 0.5V$
Maximum Junction Temperature	150°C
Operating Temperature Range	
Commercial (K, L Versions)	0°C to 70°C
Industrial (B, C Versions).....	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec).....	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
OUT1 [1]	[20] R_{FB}	LTC7545ABG
AGND [2]	[19] V_{REF}	LTC7545ABN
DGND [3]	[18] V_{DD}	LTC7545ABSW
DB11 (MSB) [4]	[17] \overline{WR}	LTC7545ACG
DB10 [5]	[16] \overline{CS}	LTC7545ACN
DB9 [6]	[15] DB0 (LSB)	LTC7545ACSW
DB8 [7]	[14] DB1	LTC7545AKG
DB7 [8]	[13] DB2	LTC7545AKN
DB6 [9]	[12] DB3	LTC7545AKSW
DB5 [10]	[11] DB4	LTC7545ALG
G PACKAGE N PACKAGE 20-LEAD PLASTIC SSOP 20-LEAD PDIP		LTC7545ALN
SW PACKAGE 20-LEAD PLASTIC SO WIDE		LTC7545ALSW
$T_{JMAX} = XXX^{\circ}C, \theta_{JA} = XXX^{\circ}C/W$ (G) $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 100^{\circ}C/W$ (N) $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 130^{\circ}C/W$ (SW)		

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V$ or $15V$, $V_{REF} = 10V$, $V_{OUT1} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC7545AK/AB			LTC7545AL/AC			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Accuracy										
	Resolution		●	12			12		Bits	
INL	Integral Nonlinearity (Relative Accuracy)	(Note 1)	$T_A = 25^{\circ}C$ T_{MIN} to T_{MAX}	●		± 0.5		± 0.5	LSB	
				●		± 0.5		± 0.5	LSB	
DNL	Differential Nonlinearity	Guaranteed Monotonic T_{MIN} to T_{MAX}	$T_A = 25^{\circ}C$ T_{MIN} to T_{MAX}	●		± 1		± 0.5	LSB	
				●		± 1		± 0.5	LSB	
GE	Gain Error	(Note 2)	$T_A = 25^{\circ}C$ T_{MIN} to T_{MAX}	●		± 2		± 1	LSB	
				●		± 3		± 2	LSB	
	Gain Temperature Coefficient	(Note 3) $\Delta Gain/\Delta Temperature$	●		1	5		1	5	ppm/ $^{\circ}C$
I_{LKG}	OUT1 Leakage Current	(Note 4)	$T_A = 25^{\circ}C$ T_{MIN} to T_{MAX}	●		± 10		± 10	nA	
				●		± 50		± 50	nA	
PSRR	Power Supply Rejection		●			± 0.002		± 0.002	%/%	
Reference Input										
R_{REF}	V_{REF} Input Resistance	(Note 5)	●	8	11	15	8	11	15	k Ω
AC Performance										
	Output Current Settling Time	(Notes 3, 6, 7)	●			1		1	μs	
	Propagation Delay	(Notes 3, 6, 8)	●			150		150	ns	
	Digital-to-Analog Glitch Impulse	(Notes 6, 9)	●		5		5		nV-sec	
	Multiplying Feedthrough Error	$V_{REF} = \pm 10V$, 10kHz Sine Wave	●		5		5		mV _{p-p}	
Analog Outputs										
C_{OUT}	Output Capacitance (Note 3)	DB0 to DB11 = 0V, WR, CS = 0V	C_{OUT1}	●	30	70	30	70	pF	
		DB0 to DB11 = V_{DD} , WR, CS = 0V	C_{OUT1}	●	60	150	60	150	pF	

ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V$, $V_{REF} = 10V$, $V_{OUT1} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	ALL GRADES			UNITS	
			MIN	TYP	MAX		
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4		V	
V_{IL}	Digital Input Low Voltage		●		0.8	V	
I_{IN}	Digital Input Current		●	0.001	±1	μA	
C_{IN}	Digital Input Capacitance	(Note 3) $V_{IN} = 0V$	●		8	pF	
Timing Characteristics (Note 3)							
t_{CS}	\overline{CS} to \overline{WR} Setup Time		●	100		ns	
t_{CH}	\overline{CS} to \overline{WR} Hold Time		●	0		ns	
t_{WR}	Write Pulse Width		●	100		ns	
t_{DS}	Data Setup Time		●	100		ns	
t_{DH}	Data Hold Time		●	5		ns	
Power Supply							
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
I_{DD}	Supply Current	All Digital Inputs = V_{IH} or V_{IL}	●		2		mA
		All Digital Inputs = $0V$ or V_{DD}	●	10	100		μA

$V_{DD} = 15V$, $V_{REF} = 10V$, $V_{OUT1} = AGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	ALL GRADES			UNITS	
			MIN	TYP	MAX		
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	13.5		V	
V_{IL}	Digital Input Low Voltage		●		1.5	V	
I_{IN}	Digital Input Current		●		±1	μA	
C_{IN}	Digital Input Capacitance	(Note 3) $V_{IN} = 0V$	●		8	pF	
Timing Characteristics (Note 3)							
t_{CS}	\overline{CS} to \overline{WR} Setup Time		●	75		ns	
t_{CH}	\overline{CS} to \overline{WR} Hold Time		●	0		ns	
t_{WR}	Write Pulse Width		●	75		ns	
t_{DS}	Data Setup Time		●	60		ns	
t_{DH}	Data Hold Time		●	5		ns	
Power Supply							
V_{DD}	Supply Voltage		●	14.25	15	15.75	V
I_{DD}	Supply Current	All Digital Inputs = V_{IH} or V_{IL}	●		2		mA
		All Digital Inputs = $0V$ or V_{DD}	●	10	100		μA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: $\pm 0.5LSB = \pm 0.012\%$ of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT1} with DAC register loaded to all 0s.

Note 5: Typical temperature coefficient is 100ppm/°C.

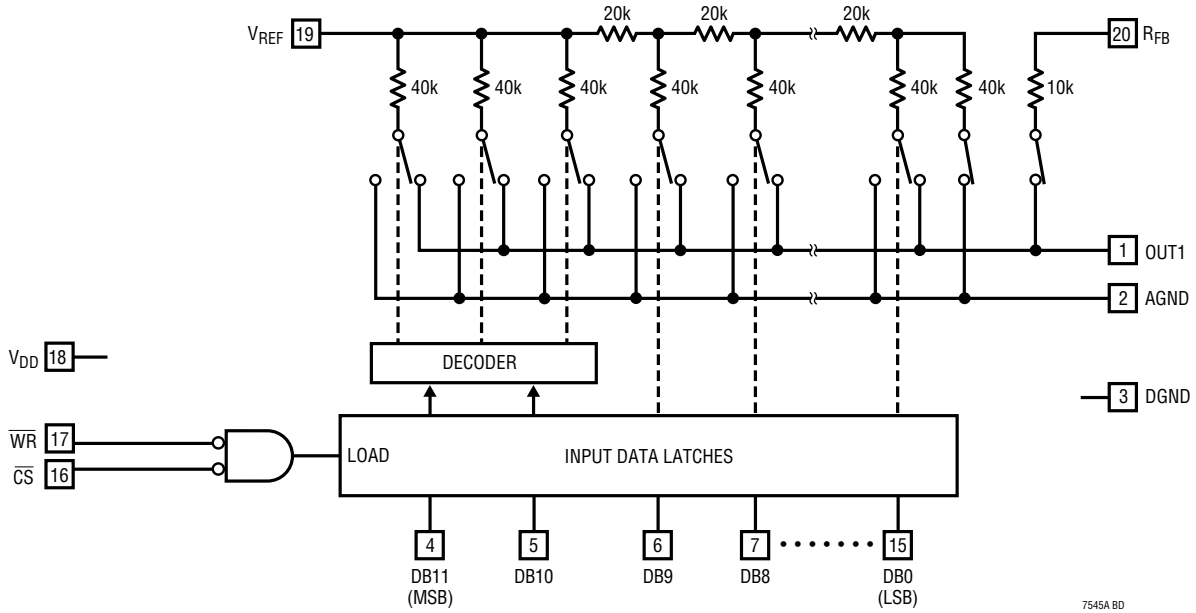
Note 6: $OUT1$ load = 100Ω in parallel with 13pF.

Note 7: To 0.01% for a full-scale change, measured from the falling edge of WR , $CS = 0V$.

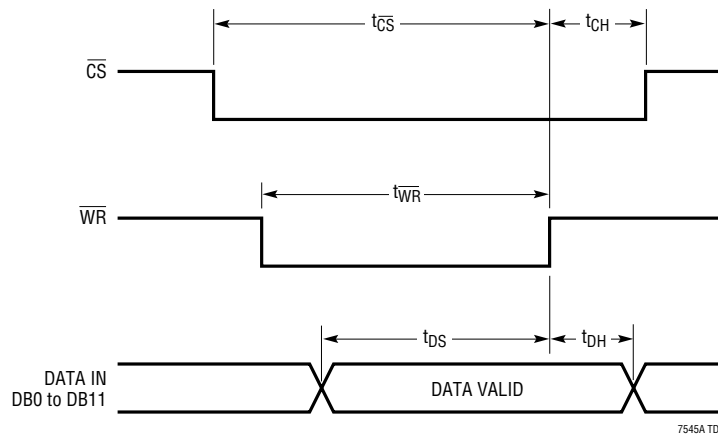
Note 8: From digital input change to 90% of final analog output.

Note 9: $V_{REF} = 0V$. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

BLOCK DIAGRAM

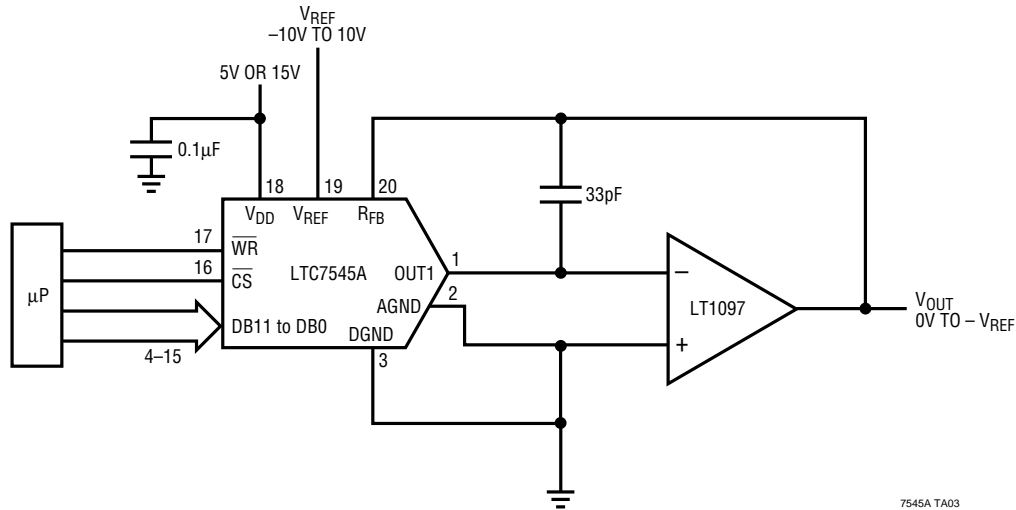


TIMING DIAGRAM



TYPICAL APPLICATIONS

Unipolar Operation (2-Quadrant Multiplication)



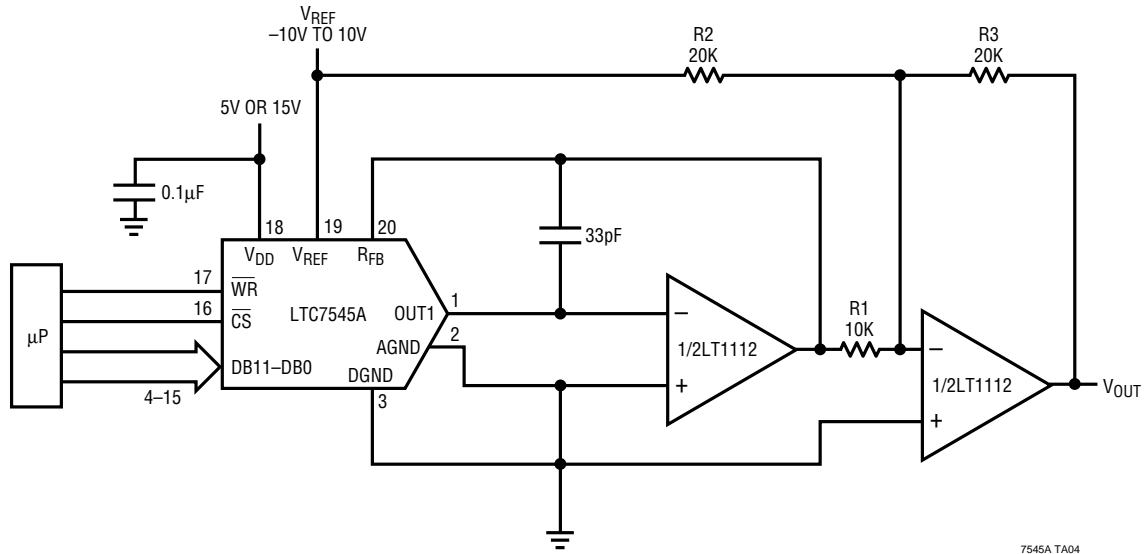
7545A TA03

Table 1. Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC LATCH			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{REF}$ (4095/4096)
1000	0000	0000	$-V_{REF}$ (2048/4096) = $-V_{REF}/2$
0000	0000	0001	$-V_{REF}$ (1/4096)
0000	0000	0000	0V

TYPICAL APPLICATIONS

Bipolar Operation (4-Quadrant Multiplication)



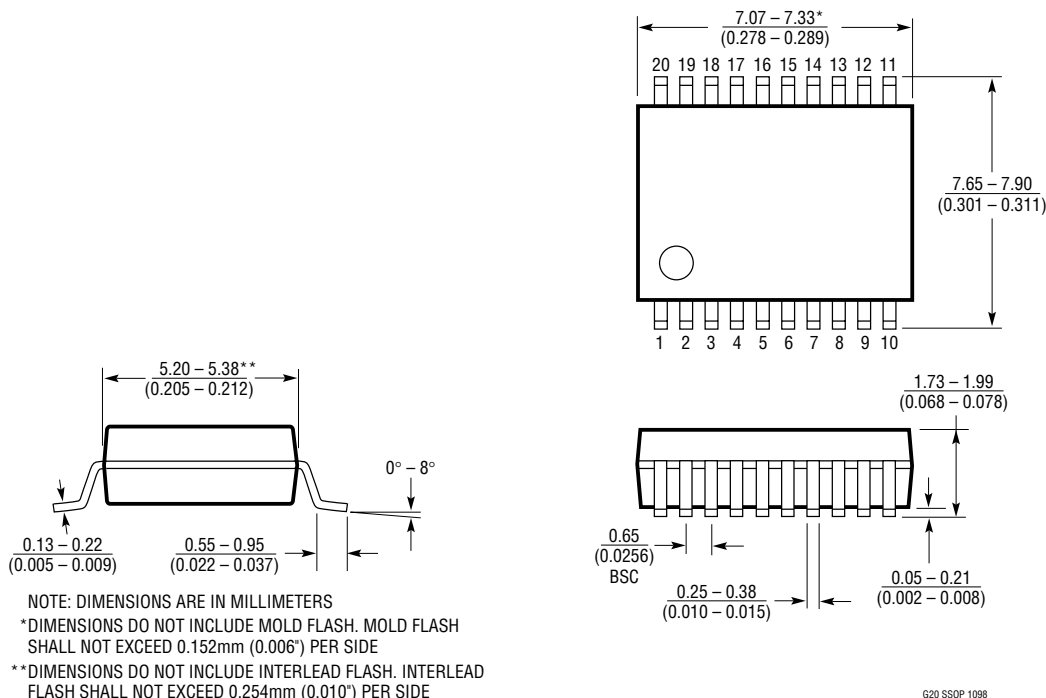
7545A TA04

Table 2. Bipolar Offset Binary Code Table

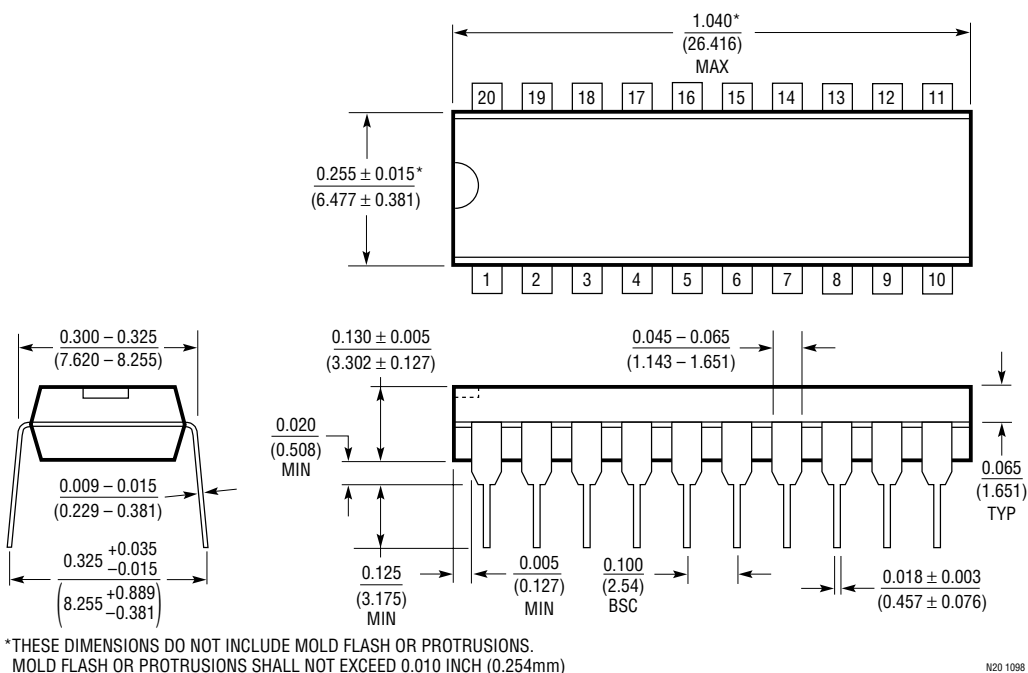
DIGITAL INPUT BINARY NUMBER IN DAC LATCH			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	V_{REF} (2047/2048)
1000	0000	0001	V_{REF} (1/2048)
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}$ (1/2048)
0000	0000	0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

G Package
20-Lead Plastic SSOP (0.209)
 (LTC DWG # 05-08-1640)

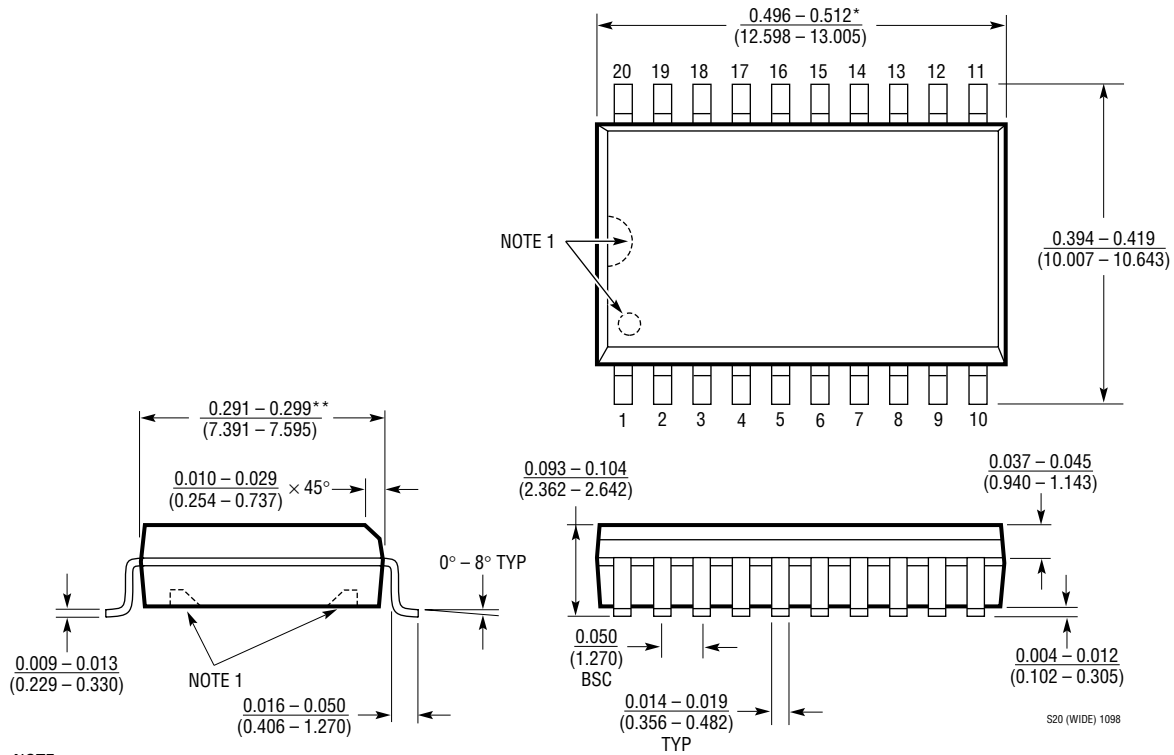


N Package
20-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
 (LTC DWG # 05-08-1620)



NOTE:
 1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
 THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
 *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTON	COMMENTS
LTC1257	Complete Serial I/O V _{OUT} 12-Bit DAC	5V to 15V Single Supply in 8-Pin SO and PDIP
LTC1450/LTC1450L	Complete Parallel Input V _{OUT} 12-Bit DACs	Rail-to-Rail V _{OUT} , 3V/5V Single Supply, 12-Bit or (8 + 4) Bit Loading
LTC1451/LTC1452/LTC1453	Complete Serial I/O V _{OUT} 12-Bit DACs	Rail-to-Rail V _{OUT} , 3V/5V Single Supply in 8-Pin SO and PDIP
LTC7541A	Parallel I/O Multiplying I _{OUT} 12-Bit DAC	12-Bit Wide Parallel Input
LTC7543/LTC8143	Serial I/O Multiplying I _{OUT} 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)
LTC8043	Serial I/O Multiplying I _{OUT} 12-Bit DAC	8-Pin SO and PDIP

Mouser Electronics

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