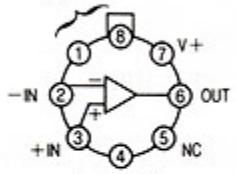
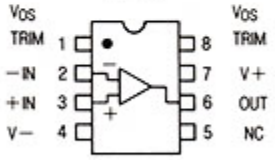
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
  OP-07/OP-07A ..... −55°C to 125°C
  OP-07E/OP-07C ..... 0°C to 70°C
Storage Temperature Range
  All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NO.	OFFSET VOLTAGE (MAX)
TOP VIEW OFFSET ADJUST  V− (CASE) METAL CAN H PACKAGE	OP-07AH OP-07H OP-07EH OP-07CH	25μV 75μV 75μV 150μV
TOP VIEW  HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE	OP-07AJ8 OP-07J8 OP-07EJ8 OP-07CJ8 OP-07EN8 OP-07CN8	25μV 75μV 75μV 150μV 75μV 150μV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	25		30	75	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0		0.2	1.0	μV/Month
I_{OS}	Input Offset Current			0.3	2.0		0.4	2.8	nA
I_B	Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μV_{P-P}
	Input Noise Voltage Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA_{P-P}
	Input Noise Current Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 4)	30	80		20	60		MΩ
	Input Resistance Common Mode			200			200		GΩ
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 4)	300 150	500 400		200 150	500 400		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μS
GBW	Closed Loop Bandwidth	A_{VCL} = +1 (Note 4)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	V_O = 0, I_O = 0, f = 10Hz		60			60		Ω
P_d	Power Dissipation	V_S = ±15V V_S = ±3V		75 4	120 6		75 4	120 6	mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mV

See Notes on page 4.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		25	60		60	200	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	●		 0.2 0.2	 0.6 0.6		 0.3 0.3	 1.3 1.3	μV/°C
I_{OS}	Input Offset Current		●		0.8	4.0		1.2	5.6	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		5	25		8	50	pA/°C
I_B	Input Bias Current		●		±1.0	±4.0		±2.0	±6.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		8	25		13	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	123		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106		94	106		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	200	400		150	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±12.0	±12.6		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		30	75		60	150	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.3	1.5		0.4	2.0	μV/Month
I_{OS}	Input Offset Current			0.5	3.8		0.8	6.0	nA
I_B	Input Bias Current			±1.2	±4.0		±1.8	±7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.65	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
I_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		15	35	pA_{p-p}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 4)	15	50		8	33		MΩ
	Input Resistance Common Mode			160			120		GΩ
	Input Voltage Range		±13.5	±14.0		±13.0	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	106	123		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	94	106		90	104		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	200 150	500 400		120 100	400 400		V/mV
V_O	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±11.5	±13.0 ±12.8 ±12.0		V
SR	Slewing Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.25		0.1	0.25		V/μS
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, $f = 10Hz$		60			60		Ω
P_d	Power Dissipation	$V_S = \pm 15V$. $V_S = \pm 3V$.		75 4	120 6		80 4	150 8	mW mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mV

See Notes on page 4.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	UNITS
V_{OS}	Input Offset Voltage		●		45	130		85	250	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	●		 0.3 0.3	 1.3 1.3		 0.5 0.4	 1.8 1.6	μV/°C
I_{OS}	Input Offset Current		●		0.9	5.3		1.6	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		8	35		12	50	pA/°C
I_B	Input Bias Current		●		±1.5	±5.5		±2.2	±9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		13	35		18	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	103	123		97	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	90	104		86	100		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	180	450		100	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±11.0	±12.6		V

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Offset voltage for the OP-07A is measured 60 seconds after power is applied. All other grades are measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

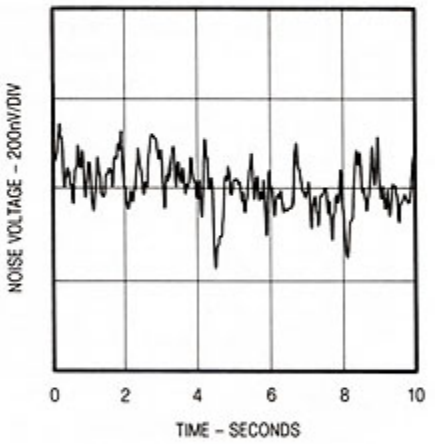
Note 3: Long term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.

Note 4: This parameter is guaranteed by design.

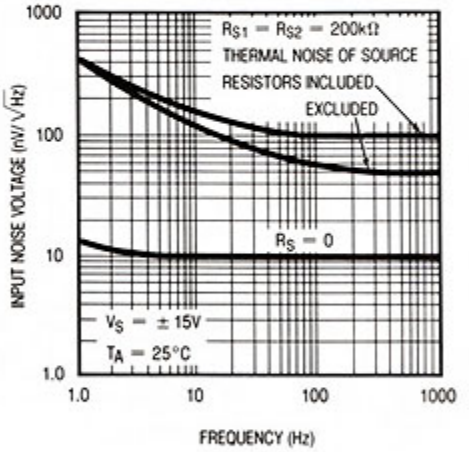
Note 5: The OP-07D is available by special request.

TYPICAL PERFORMANCE CHARACTERISTICS

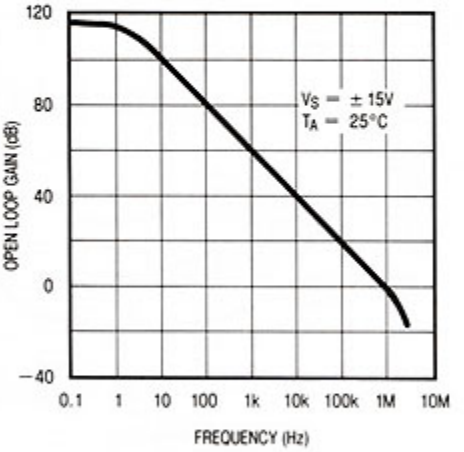
Low Frequency Noise (Closed Loop Gain = 25,000)



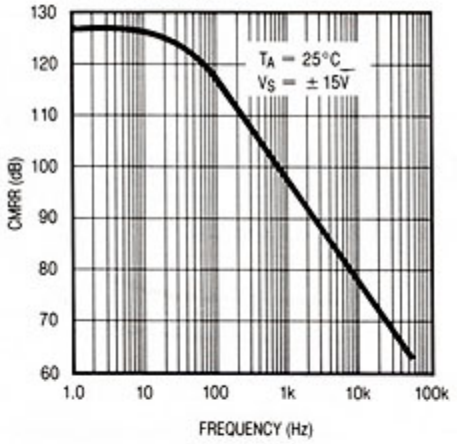
Total Input Noise Voltage vs Frequency



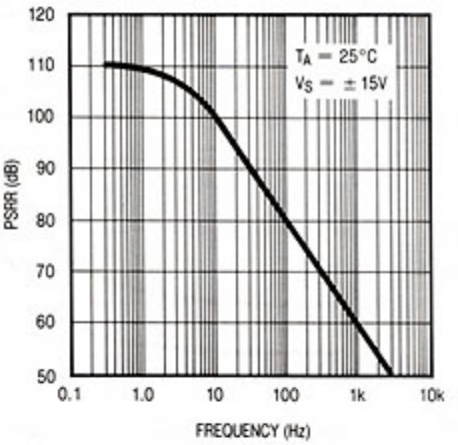
Open-Loop Frequency Response



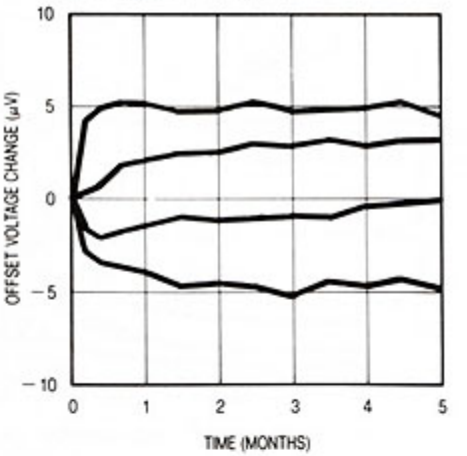
Common Mode Rejection Ratio vs Frequency



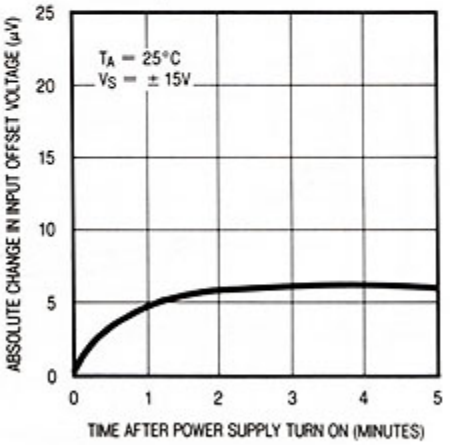
Power Supply Rejection Ratio vs Frequency



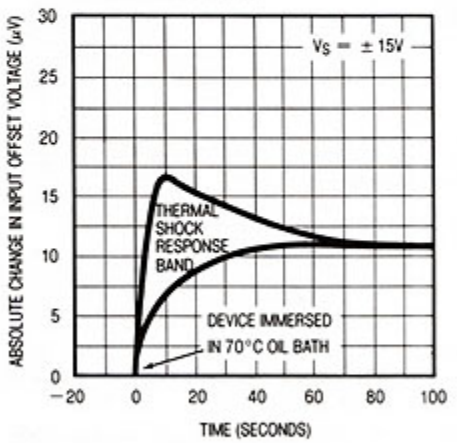
Long Term Stability of Four Representative Units



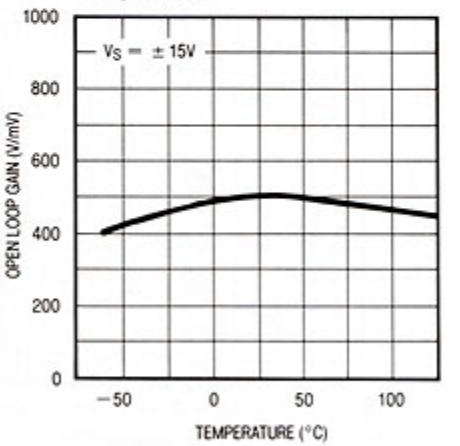
Warm-Up Drift



Offset Voltage Change Due to Thermal Shock

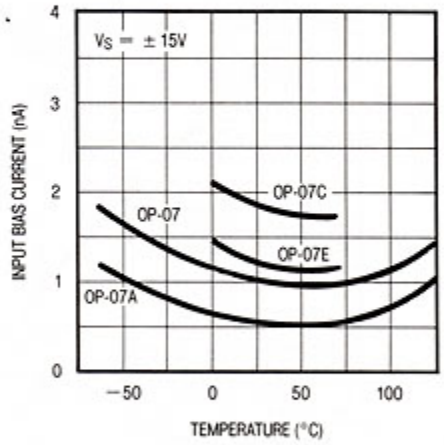


Open-Loop Gain vs Temperature

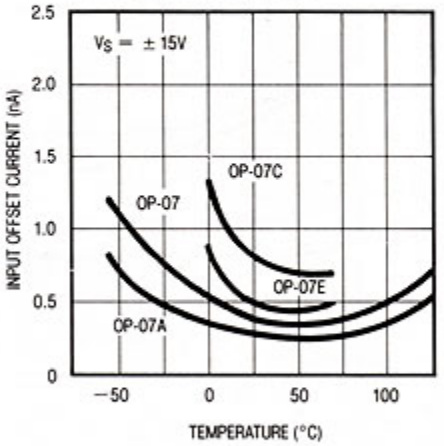


TYPICAL PERFORMANCE CHARACTERISTICS

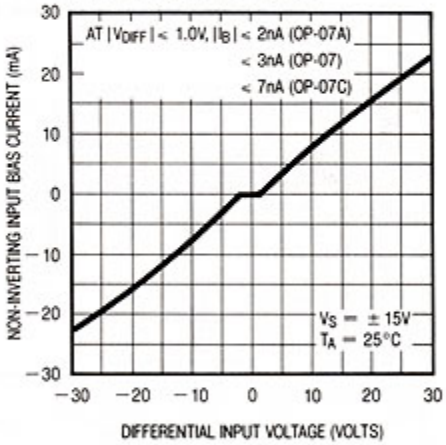
Input Bias Current vs Temperature



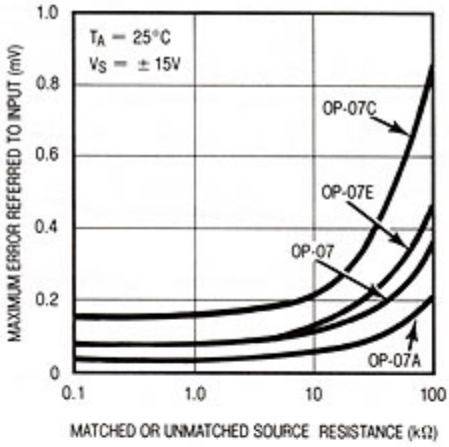
Input Offset Current vs Temperature



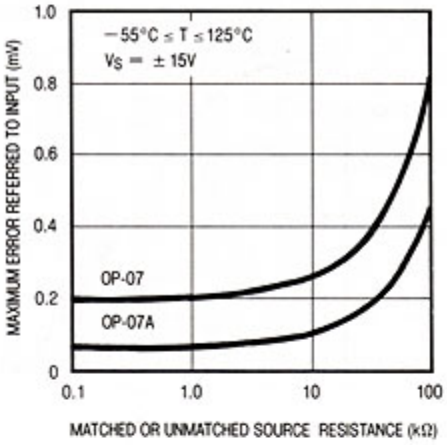
Input Bias Current vs Differential Input Voltage



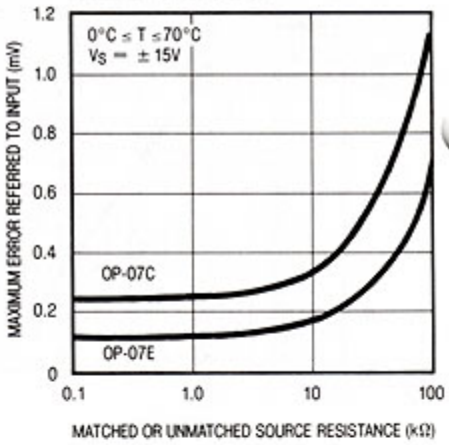
Maximum Error vs Source Resistance



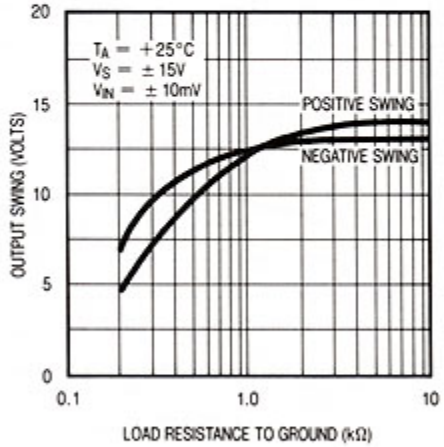
Maximum Error vs Source Resistance



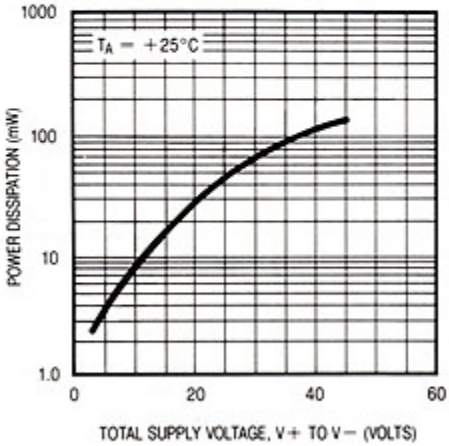
Maximum Error vs Source Resistance



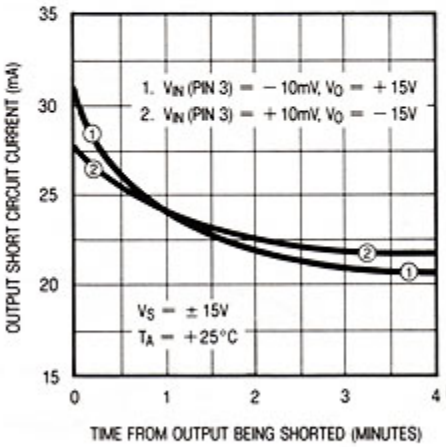
Output Voltage vs Load Resistance



Power Consumption vs Power Supply

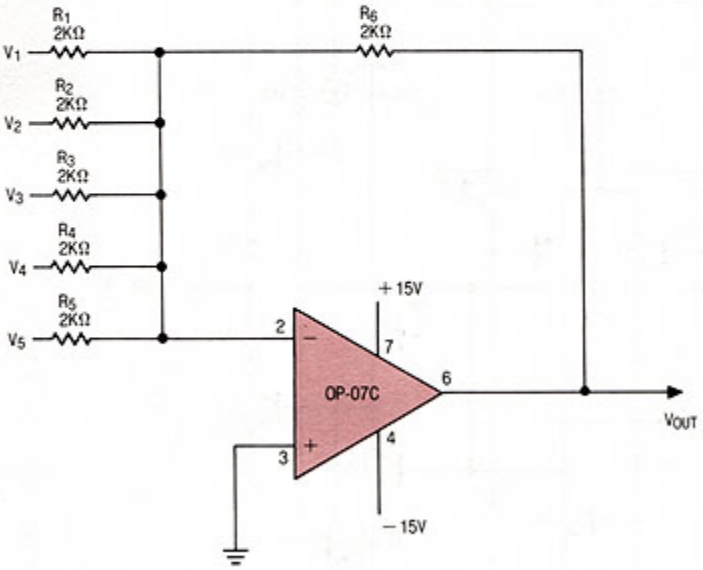


Output Short-Circuit Current vs Time

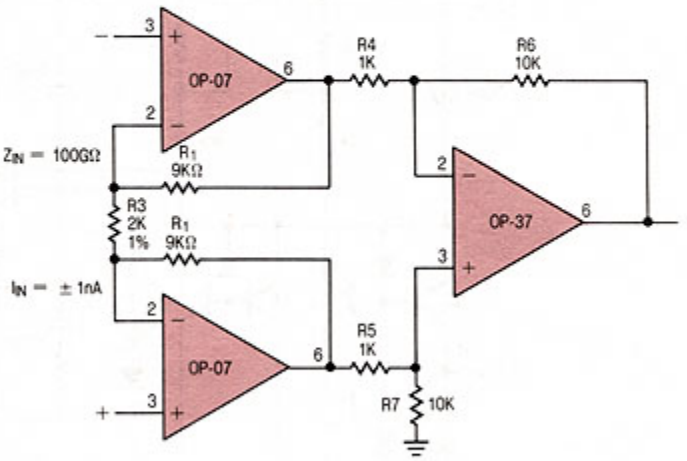


TYPICAL APPLICATIONS

Precision Summing Amplifier



Instrumentation Amplifier

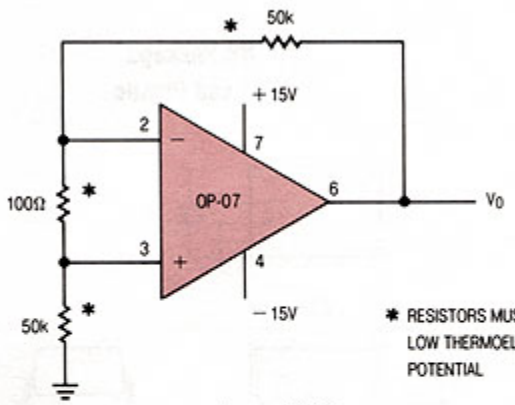


$$A_V = \frac{R6}{R4}\left(\frac{2R1}{R3} + 1\right)$$

$$A_V = 100$$

TEST CIRCUIT DIAGRAMS

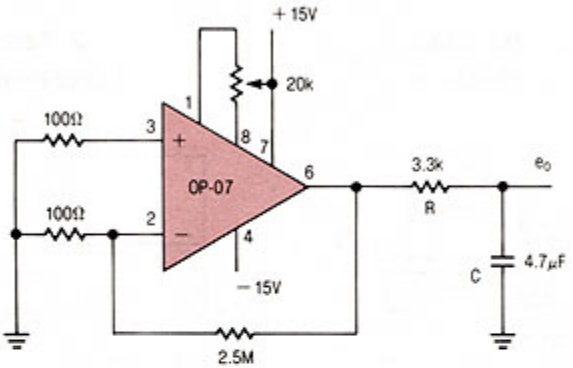
Offset Voltage Test Circuit †



* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL

$$A_V = 1000$$

Offset Nulling and Low Frequency Noise Test Circuit



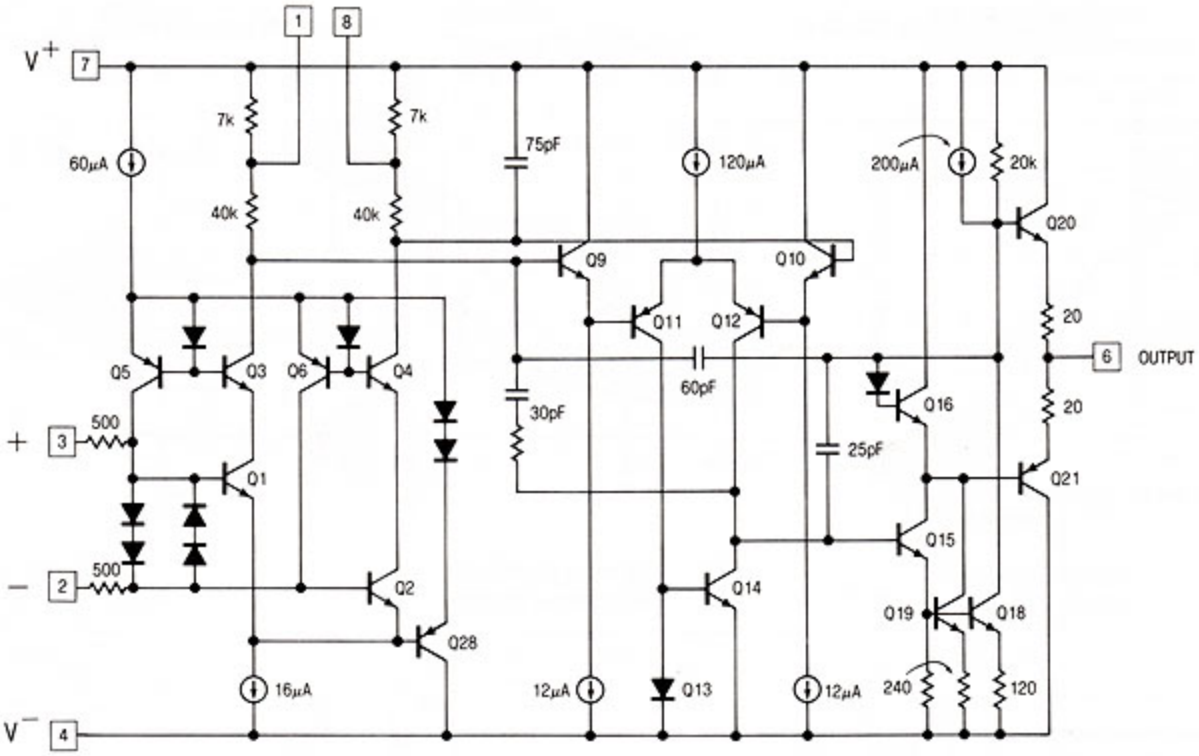
NOTES:
1) RC APPROXIMATELY 10Hz FILTER
2) OBSERVE OUTPUT FOR 10 SECONDS
$A_V = 25000$

† This circuit is also used as the burn-in configuration with supply voltages changed to ±20 Volts.

Application Tip:

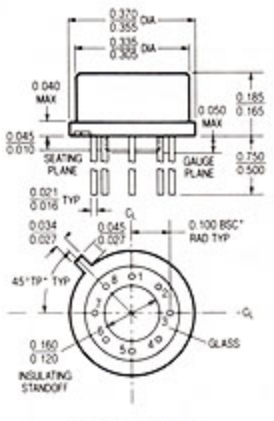
When the OP-07 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

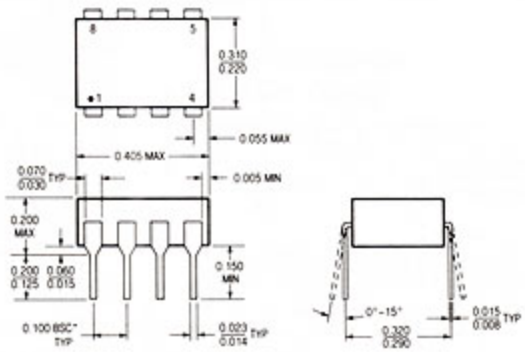
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

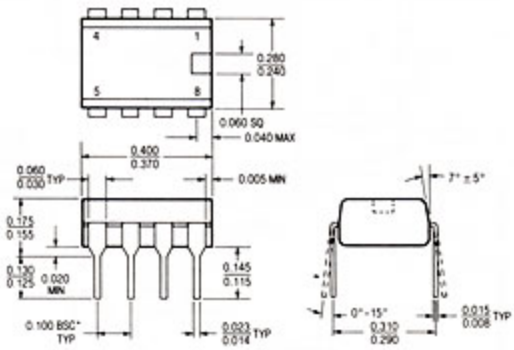
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

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