

Voltage-Output, 12-Bit DACs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND	-0.3V, +17V	Continuous Power Dissipation (any package)	
V _{DD} to DGND	-0.3V, +17V	to +75°C	450mW
V _{DD} to V _{SS}	-0.3V, +34V	derate above +75°C	6mW/°C
AGND to DGND	-0.3V, V _{DD}	Operating Temperature Ranges:	
Digital Input Voltage to GND	-0.3V, V _{DD} +0.3V	MAX507_C_, MAX508_C_	0°C to +70°C
V _{OUT} to AGND (Note 1)	V _{SS} , V _{DD}	MAX507_E_, MAX508_E_	-40°C to +85°C
V _{OUT} to V _{SS} (Note 1)	0V, +34V	MAX507_M_, MAX508_M_	-55°C to +125°C
V _{OUT} to V _{DD} (Note 1)	-34V, 0V	Storage Temperature Range	-65°C to +150°C
REFOUT to AGND (Note 1)	-0.3V, V _{DD} +0.3V	Lead Temperature (soldering, 10 sec)	+300°C

Note 1: The output can be shorted to either supply rail if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Single Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
STATIC PERFORMANCE								
Resolution	N			12			Bits	
Relative Accuracy	INL	T _A = +25°C	MAX507/508A			±1/2	LSB	
			MAX507/508B			±3/4		
		T _A = T _{MIN} to T _{MAX}	MAX507/508A			±3/4		
			MAX507/508B			±1		
Differential Nonlinearity	DNL					±1	LSB	
Unipolar Offset Error		T _A = +25°C					±3	LSB
		T _A = T _{MIN} to T _{MAX}					±5	
DAC Gain Error						±2	LSB	
Full-Scale Output Voltage Error		V _{DD} = +12V or +15V	T _A = +25°C			±0.2	%FSR	
			T _A = T _{MIN} to T _{MAX}			±0.6		
Full-Scale Output Voltage Change		V _{DD} over full range	T _A = +25°C			±0.12	%FSR/V	
			T _A = T _{MIN} to T _{MAX}			±0.2		
Full-Scale Tempco		MAX507/508_C/E				±30	ppm	
		MAX507/508_M				±40	FSR/°C	
Unipolar Offset Error Change		V _{DD} = +12V ± 5% or +15V ± 5%				±1	mV	

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MAX507/MAX508

ELECTRICAL CHARACTERISTICS (continued)

Single Supply ($V_{DD} = +11.4V$ to $+15.75V$, $V_{SS} = AGND = DGND = 0V$, $R_L = 2k\Omega$, $C_L = 100pF$, REFOUT unloaded, all grades, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Reference Output		$V_{DD} = +12V$ or $+15V$	$T_A = +25^\circ C$	4.99		5.01	V
Reference Voltage Change		$V_{DD} = +12V \pm 5\%$ or $+15V \pm 5\%$	$T_A = +25^\circ C$			2	mV/V
			$T_A = T_{MIN}$ to T_{MAX}			6	
Reference Temperature Coefficient		MAX507/508_C/E			± 30		ppm/ $^\circ C$
		MAX507/508_M			± 40		
Reference Load Sensitivity		$I_{LOAD} = 0\mu A$ to $100\mu A$				± 1	mV
ANALOG OUTPUT							
Ranges (Note 2)						0 to 5	V
						0 to 10	
Output Range Resistors				15		30	k Ω
DC Output Impedance					0.5		Ω
Short-Circuit Current					40		mA
DYNAMIC PERFORMANCE (Note 3)							
Voltage-Output Slew Rate				2			V/ μs
V_{OUT} Settling Time			To $\pm 1/2$ LSB for full-scale change			5	μs
Digital Feedthrough					10		nV-s
Digital-to-Analog Glitch Impulse			Major carry transition		30		nV-s
Output Load Resistance (Note 2)			$V_{OUT} = 0V$ to $+10V$	2			k Ω
POWER SUPPLIES							
V_{DD} Range			For specified performance	11.4		15.75	V
I_{DD}		Outputs unloaded	$T_A = +25^\circ C$			9	mA
			$T_A = T_{MIN}$ to T_{MAX}			12	

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MAX507/MAX508

ELECTRICAL CHARACTERISTICS

Dual Supply ($V_{DD} = +11.4V$ to $+15.75V$, $V_{SS} = -11.4V$ to $-15.75V$, $DGND = AGND = 0V$, $R_L = 2k\Omega$, $C_L = 100pF$, $REFOUT$ unloaded, all grades, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	$T_A = +25^\circ C$	MAX507/508A			$\pm 1/2$	LSB
			MAX507/508B			$\pm 3/4$	
		$T_A = T_{MIN}$ to T_{MAX}	MAX507/508A			$\pm 3/4$	
			MAX507/508B			± 1	
Differential Nonlinearity	DNL					± 1	LSB
Bipolar Zero Offset Error	BZOE	MAX507/508A	$T_A = +25^\circ C$			± 2	LSB
			$T_A = T_{MIN}$ to T_{MAX}			± 4	
		MAX507/508B	$T_A = +25^\circ C$			± 3	
			$T_A = T_{MIN}$ to T_{MAX}			± 5	
DAC Gain Error						± 2	LSB
Full-Scale Output Voltage Error		$V_{DD} = +15V$, $V_{SS} = -15V$	$T_A = +25^\circ C$			± 0.2	%FSR
			$T_A = T_{MIN}$ to T_{MAX}			± 0.6	
		$V_{DD} = +12V$, $V_{SS} = -12V$	$T_A = +25^\circ C$			± 0.2	
			$T_A = T_{MIN}$ to T_{MAX}			± 0.6	
Full-Scale Output Change with V_{DD}		$V_{DD} = +12V \pm 5\%$ or $+15V \pm 5\%$ $V_{SS} = -12V$ or $-15V$	$T_A = +25^\circ C$			± 0.12	%FSR/V
			$T_A = T_{MIN}$ to T_{MAX}			± 0.2	
Full-Scale Output Change with V_{SS}	V_{SS}	$V_{SS} = -12V \pm 5\%$ or $-15V \pm 5\%$ $V_{DD} = +12V$ or $+5V$			0.01		%FSR/V
Full-Scale Tempco		MAX507/508_C/E			± 30		ppm FSR/ $^\circ C$
		MAX507/508_M			± 40		
Bipolar Zero Offset Change		$V_{DD} = +12V \pm 5\%$ or $+15V \pm 5\%$ $V_{SS} = -12V$ or $-15V$ $V_{SS} = -12V \pm 5\%$ or $-15V \pm 5\%$ $V_{DD} = +12V$ or $+15V$			± 1		mV
					± 1		
REFERENCE							
Reference Output		$V_{DD} = +12V$ or $+15V$	$T_A = +25^\circ C$	4.99	5.01		V
Reference Output Change		V_{DD} over full range	$T_A = +25^\circ C$			2	mV/V
			$T_A = T_{MIN}$ to T_{MAX}			6	
Reference Temperature Coefficient		MAX507/508_C/E			± 30		ppm/ $^\circ C$
		MAX507/508_M			± 40		
Reference Load Sensitivity		$I_{LOAD} = 0\mu A$ to $100\mu A$			± 1		mV

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MAX507/MAX508

ELECTRICAL CHARACTERISTICS (continued)

Dual Supply ($V_{DD} = +11.4V$ to $+15.75V$, $V_{SS} = -11.4V$ to $-15.75V$, $DGND = AGND = 0V$, $R_L = 2k\Omega$, $C_L = 100pF$, $REFOUT$ unloaded, all grades, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG OUTPUT						
Ranges (Notes 2, 4)			0 to +5 or +10, -5 to +5			V
Output Range Resistors			15		30	k Ω
DC Output Impedance				0.5		Ω
Short-Circuit Current				40		mA
DYNAMIC PERFORMANCE (Note 3)						
Voltage-Output Slew Rate			2			V/ μ s
V_{OUT} Settling Time		to $\pm 1/2$ LSB			5	μ s
Digital Feedthrough				10		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		30		nV-s
Output Load Resistance		$V_{OUT} = -5V$ to $+10V$	2			k Ω
POWER SUPPLIES						
V_{DD} Range		For specified performance	11.4		15.75	V
V_{SS} Range		For specified performance	-11.4		-15.75	V
I_{DD}		Outputs unloaded	$T_A = +25^\circ C$		9	mA
			$T_A = T_{MIN}$ to T_{MAX}		12	
I_{SS}		Outputs unloaded	$T_A = +25^\circ C$		3	mA
			$T_A = T_{MIN}$ to T_{MAX}		5	

Voltage-Output, 12-Bit DACs with Internal Reference

ELECTRICAL CHARACTERISTICS

Single or Dual Supply ($V_{DD} = +11.4V$ to $+15.75V$, $V_{SS} = 0V$ to $-15.75V$, $DGND = AGND = 0V$, $REFOUT$ unloaded, $R_L = 2k\Omega$, $C_L = 100pF$, all grades, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
V_{INH}			2.4			V
V_{INL}					0.8	V
Input Current	I_{IN}	D0-D11	$T_A = +25^\circ C$		± 1	μA
			$T_A = T_{MIN}$ to T_{MAX}		± 10	
I_{INH}		\overline{CS} , \overline{WR} , \overline{LDAC} , \overline{CLR}	$T_A = +25^\circ C$		± 1	μA
			$T_A = T_{MIN}$ to T_{MAX}		± 10	
I_{INL}		\overline{CS} , \overline{WR} , \overline{LDAC} , \overline{CLR}	$T_A = +25^\circ C$		± 150	μA
			$T_A = T_{MIN}$ to T_{MAX}		± 200	
Digital Input Capacitance				8		pF

TIMING CHARACTERISTICS

(All grades, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
\overline{CS} Pulse Width (Note 5)	t_1	$T_A = +25^\circ C$	80			ns
		$T_A = T_{MIN}$ to T_{MAX}	100			
\overline{WR} Pulse Width	t_2	$T_A = +25^\circ C$	80			ns
		$T_A = T_{MIN}$ to T_{MAX}	100			
\overline{CS} to \overline{WR} Setup Time (Note 5)	t_3		0			ns
\overline{CS} to \overline{WR} Hold Time (Note 5)	t_4		0			ns
Data to \overline{WR} Setup Time	t_5	$T_A = +25^\circ C$	100			ns
		$T_A = T_{MIN}$ to T_{MAX}	110			
Data to \overline{WR} Hold Time	t_6		10			ns
\overline{LDAC} Pulse Width	t_7	$T_A = +25^\circ C$	80			ns
		$T_A = T_{MIN}$ to T_{MAX}	100			
\overline{CLR} Pulse Width (MAX507)	t_8	$T_A = +25^\circ C$	80			ns
		$T_A = T_{MIN}$ to T_{MAX}	100			

Note 2: V_{OUT} must be less than $(V_{DD} - 2.5V)$.

Note 3: Dynamic performance is included for design guidance, not subject to test.

Note 4: The $0V$ to $+5V$ or $+10V$ ranges can be used with $V_{SS} = -5V$ with no degradation.

Note 5: $\overline{CS} = \overline{CSLSB}$ and \overline{CSMSB} for MAX508.

Voltage-Output, 12-Bit DACs with Internal Reference

MAX507/MAX508

Detailed Description Digital-to-Analog Converters

The MAX507/MAX508 are 12-bit, voltage-output DACs. The DAC output voltage has the same polarity as the reference, allowing single-supply operation.

The basic DAC circuit consists of a laser-trimmed, thin-film, R-2R resistor array with NMOS voltage switches (Figure 1).

Output-Buffer Amplifier

The output amplifier is noninverting and configurable for a gain of 1 or 2. Three output voltage ranges can be configured for: 0V to +5V, 0V to +10V, and -5V to +5V. The output amplifier can drive 2kΩ in parallel with 100pF connected to GND.

The MAX507/MAX508 can operate from a single supply with a 0V to +5V or a 0V to +10V output range by tying VSS to 0V. However, the speed and current-sinking capability of the amplifier decreases as the output falls within 0.5V of VSS. Speed and current-sinking capability can be maintained by including a negative supply. Table 1 lists the allowable single and dual supplies for each range.

The output amplifier's small-signal bandwidth is typically 2MHz. Output noise is approximately $25\text{nV}/\sqrt{\text{Hz}}$ at 1kHz, and output broadband noise is approximately $25\mu\text{VRMS}$.

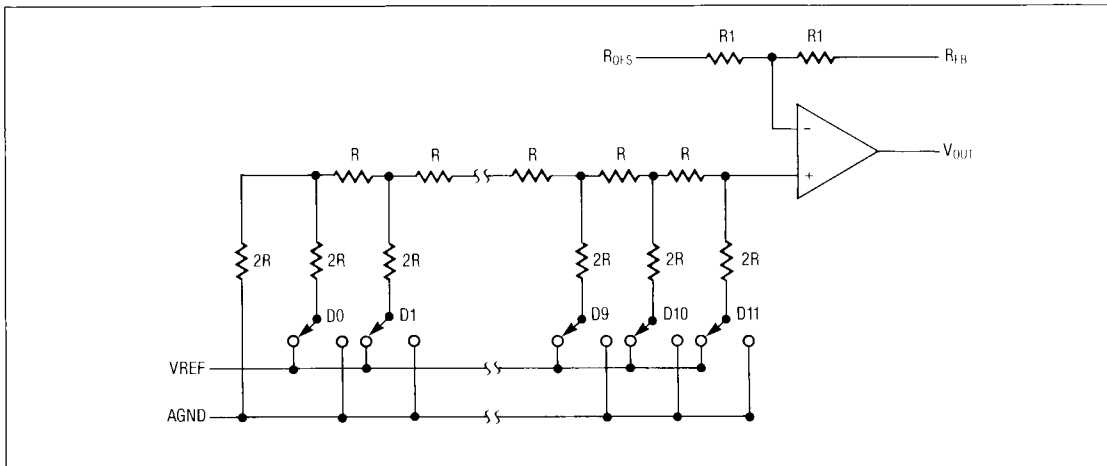


Figure 1. Simplified MAX507 DAC Circuit

Table 1. Output Voltage Range vs. Supply Voltage

Range	Single Supply	Dual Supply	
	VDD	VDD	VSS
0V to +5V	+11.4V to +15.75V	+11.4V to +15.75V	-4.5V to -15.75V
0V to +10V	+14.25V to +15.75V	+14.25V to +15.75V	-4.5V to -15.75V
-5V to +5V		+11.4V to +15.75V	-11.4V to -15.75V

Voltage-Output, 12-Bit DACs with Internal Reference

Voltage Reference

The voltage at REFOUT is $5V \pm 10mV$ at $+25^{\circ}C$. The reference is internally connected to the DAC and is buffered to accommodate the DAC's variable impedance. This buffer is capable of driving the DAC, the R_{OF}S resistor, and up to $500\mu A$ of external current. MAX507/MAX508 specifications are determined with the internal reference. The reference should be decoupled at REFOUT with 10Ω in series with the recommended decoupling capacitors, $10\mu F$ in parallel with $0.1\mu F$.

Digital Inputs and Interface Logic

All logic inputs are compatible with both TTL and 5V CMOS logic. Supply current is specified for TTL input levels, but is reduced by about $450\mu A$ when the data inputs are driven near DGND or V_{DD}. The control inputs (CLR, LDAC, WR, CS, CSMSB, and CSLSB) each draw $100\mu A$ from I_{DD} when low.

MAX507 Interface

Table 2 is the MAX507 truth table. The MAX507 accepts a 12-bit input word that can be latched or transferred directly to the DAC. CS and WR control the input latch, and LDAC transfers information from the input latch to the DAC latch.

Table 2. MAX507 Truth Table

CLR	LDAC	WR	CS	Function
1	0	0	0	Both latches transparent
1	1	1	X	Both latches latched
1	1	X	1	Both latches latched
1	1	0	0	Input latch transparent
1	1	↑	0	Input latch latched
1	0	1	1	DAC latch transparent
1	↑	1	1	DAC latch latched
0	X	X	X	DAC latch all 0s
↑	1	1	1	DAC latch latched with 0s; output at 0V or -5V
↑	0	0	0	Both latches transparent; output follows input data

1 = High State
0 = Low State
X = Don't Care
↑ = Rising Edge

The input latch is transparent when \overline{CS} and \overline{WR} are low; the DAC latch is transparent when \overline{LDAC} is low. Data is latched within the input latch on the rising edge of WR when CS is low. The rising edge of LDAC latches data into the DAC when CS and WR are low. After CS and WR are high, LDAC must be held low for t_7 or longer (Figure 2).

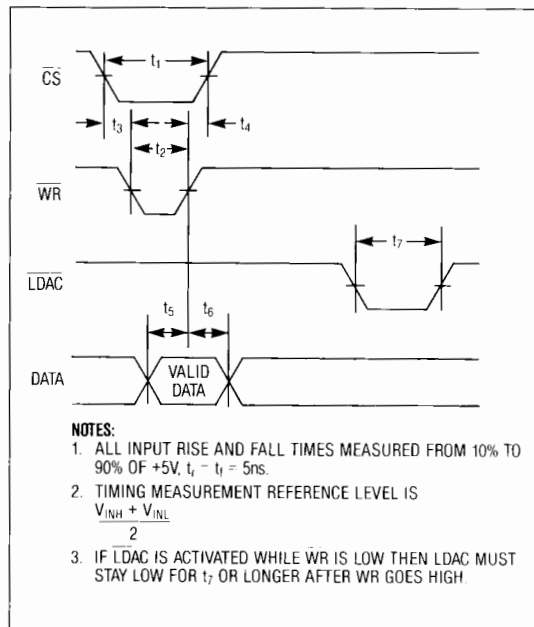


Figure 2. MAX507 Timing Diagram

The DAC latch is reset to zeros with \overline{CLR} low. \overline{CLR} acts as a zero override when the input latch and DAC latch are transparent. Then, a low-to-high \overline{CLR} transition loads all zeros into the DAC latch, and the output remains low (0V to -5V).

MAX508 Interface

The MAX508's 8-bit-wide data bus interfaces with 8-bit μP s. The MAX508 contains an input latch and a DAC latch. The data held in the DAC latch determines the output of the DAC. Table 3 is the MAX508 truth table, Figure 3 shows the input control logic, and Figure 4 shows the write-cycle timing.

Voltage-Output, 12-Bit DACs with Internal Reference

MAX507/MAX508

Table 3. MAX508 Truth Table

CSLSB	CSMSB	WR	LDAC	Function
0	1	0	1	Loads LSBs to input latches
0	1	↑	1	Locks LSBs in input latches
↑	1	0	1	Locks LSBs in input latches
1	0	0	1	Loads MSBs to input latches
1	0	↑	1	Locks MSBs in input latches
1	↑	0	1	Locks MSBs in input latches
1	1	1	0	Loads input into DAC latch
1	1	1	↑	Locks input into DAC latch
1	0	0	0	Loads MSBs to input latches and loads input into DAC latch
1	1	1	1	No data transfer

1 = High State 0 = Low State ↑ = Rising Edge

Right-justified data is loaded into the MAX508 using CSMSB, CSLSB, and WR. Data can be latched into the input latch on the rising edge of WR for the most significant bit (MSB) and least significant bit (LSB), or on the rising edge of CSMSB for the MSB and CSLSB for the LSB. Either the MSB or the LSB can be loaded first.

The complete, 12-bit word loads into the DAC register when LDAC is low, and latches on LDAC's rising edge. LDAC is asynchronous and independent of WR, so it is ideal for simultaneously updating multiple MAX508 outputs. Because LDAC can occur during a write cycle, it must stay low for t_7 (or longer) after WR goes high to ensure correct data is latched to the output.

The MAX508 output can be updated in two write cycles by tying CSMSB and LDAC. In this automatic transfer mode, CSLSB and WR latch the lower 8 bits into the input latch; then CSMSB, WR, and LDAC load the upper 4 bits into the input latch and transfer the 12-bit word into the DAC latch. Alternatively, the MAX507 can be updated in two writes by tying CSLSB to LDAC if the upper 4 bits are input first, followed by the lower 8 bits.

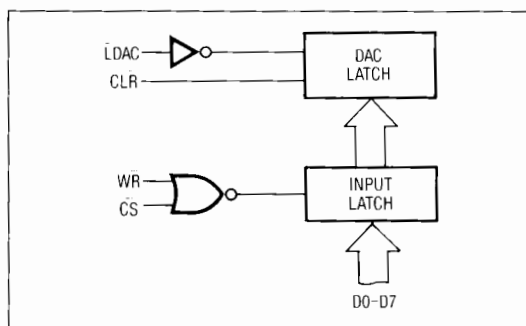


Figure 3a. MAX507 Input Control Logic

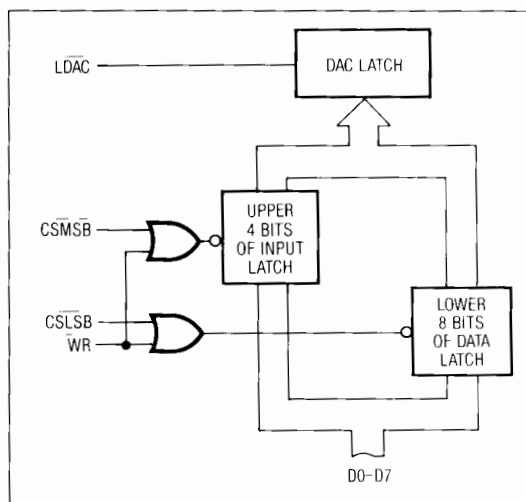


Figure 3b. MAX508 Input Control Logic

Voltage-Output, 12-Bit DACs with Internal Reference

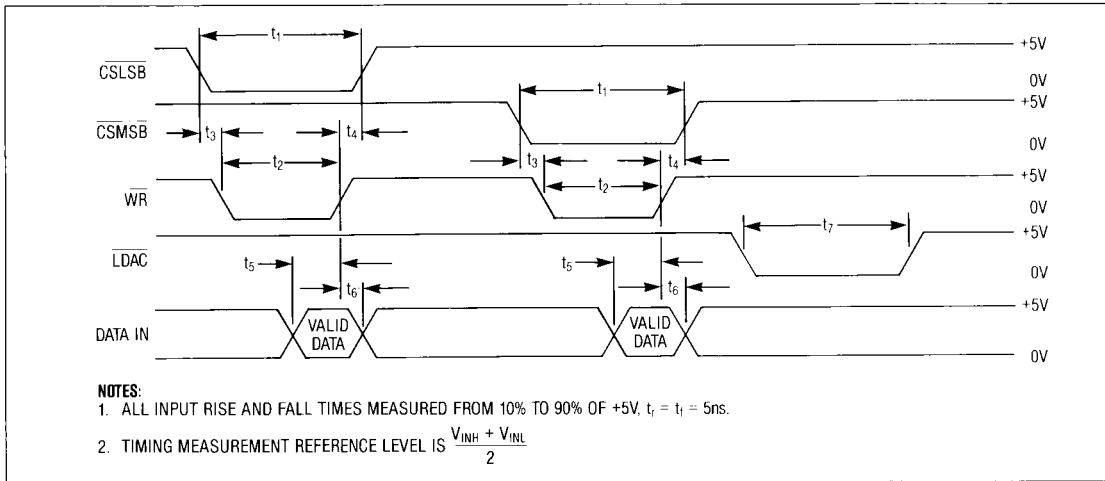


Figure 4. MAX508 Timing Diagram

Unipolar Configuration

The MAX507/MAX508 are set up for a 0V to +5V unipolar output range by connecting R_{OFS} , R_{FB} , and V_{OUT} (Figure 5). The converters operate from either a single or a dual supply in this configuration. See Table 4 for the DAC-latch contents (input) vs. analog output (output). In this range, 1LSB = $V_{REF} (2^{-12})$.

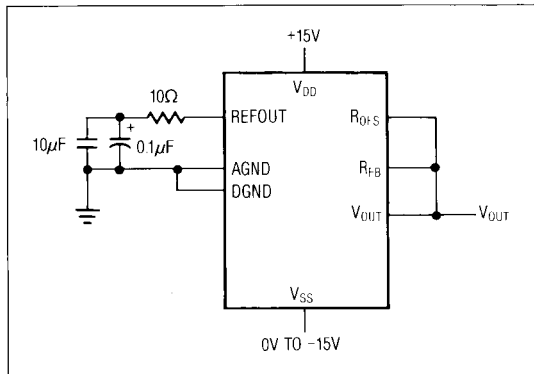


Figure 5. Unipolar Configuration (0V to +5V Output)

Table 4. Unipolar-Code Table (0V to +5V Output)

INPUT			OUTPUT
1111	1111	1111	$(V_{REF}) \frac{4095}{4096}$
1000	0000	0001	$(V_{REF}) \frac{2049}{4096}$
1000	0000	0000	$(V_{REF}) \frac{2048}{4096} = +V_{REF}/2$
0111	1111	1111	$(V_{REF}) \frac{2047}{4096}$
0000	0000	0001	$(V_{REF}) \frac{1}{4096}$
0000	0000	0000	0V

A 0V to +10V unipolar output range is set up by connecting R_{OFS} to AGND and R_{FB} to V_{OUT} (Figure 6). See Table 5 for the DAC-latch contents (input) vs. analog output (output). The MAX507/MAX508 operate from either a single or a dual supply in this configuration. In this range, 1LSB = $V_{REF} (2^{-11})$.

Voltage-Output, 12-Bit DACs with Internal Reference

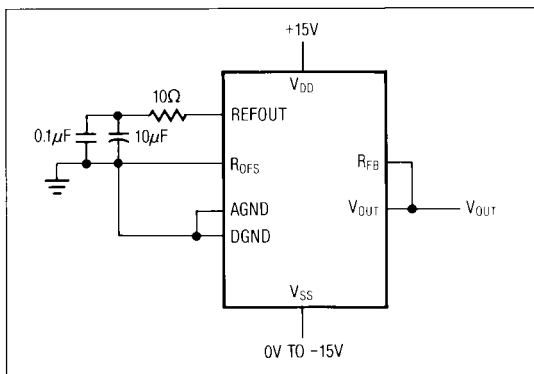


Figure 6. Unipolar Configuration (0V to +10V Output)

Table 5. Unipolar-Code Table (0V to +10V Output)

INPUT			OUTPUT
1111	1111	1111	$+2 (VREF) \frac{4095}{4096}$
1000	0000	0001	$+2 (VREF) \frac{2049}{4096}$
1000	0000	0000	$+2 (VREF) \frac{2048}{4096} = +VREF$
0111	1111	1111	$+2 (VREF) \frac{2047}{4096}$
0000	0000	0001	$+2 (VREF) \frac{1}{4096}$
0000	0000	0000	0V

Bipolar Configuration

A -5V to +5V bipolar range is set up by connecting R_{0FS} to REFOUT and R_{FB} to V_{OUT}, and operating from dual power supplies (Table 1). See Table 6 for the DAC-latch contents (input) vs. analog output (output). In this range, 1LSB = (2) VREF (2⁻¹¹) = (VREF) 1/2048.

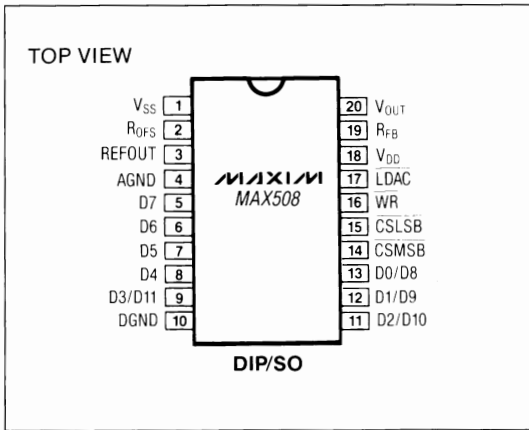
Table 6. Bipolar-Code Table (-5V to +5V Output)

INPUT			OUTPUT
1111	1111	1111	$(+VREF) \frac{2047}{2048}$
1000	0000	0001	$(+VREF) \frac{1}{2048}$
1000	0000	0000	0V
0111	1111	1111	$(-VREF) \frac{1}{2048}$
0000	0000	0001	$(-VREF) \frac{2047}{2048}$
0000	0000	0000	$(-VREF) \frac{2048}{2048} = -VREF$

MAX507/MAX508

Voltage-Output, 12-Bit DACs with Internal Reference

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX508ACPP	0°C to +70°C	20 Narrow Plastic DIP	±1/2
MAX508BCPP	0°C to +70°C	20 Narrow Plastic DIP	±3/4
MAX508ACWP	0°C to +70°C	20 Wide SO	±1/2
MAX508BCWP	0°C to +70°C	20 Wide SO	±3/4
MAX508BC/D	0°C to +70°C	Dice*	±3/4
MAX508AEPP	-40°C to +85°C	20 Narrow Plastic DIP	±1/2
MAX508BEPP	-40°C to +85°C	20 Narrow Plastic DIP	±3/4
MAX508AEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX508BEWP	-40°C to +85°C	20 Wide SO	±3/4
MAX508AMJP	-55°C to +125°C	20 Narrow Cerdip**	±1/2
MAX508BMJP	-55°C to +125°C	20 Narrow Cerdip**	±3/4

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** Contact factory for availability and processing to MIL-STD-883.

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