Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +30V
PGND to GND .....±0.3V
SYNC/$\overline{SHDN}$ to GND .....-0.3V to +30V
EXT, REF to GND ..... -0.3V to (V_{LDO} + 0.3V)
LDO, FREQ, FB, CS+ to GND .....-0.3V to +6V
LDO Output Current ..... -1mA to +20mA
REF Output Current ..... -1mA to +1mA
LDO Short Circuit to GND ..... Momentary
REF Short Circuit to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering,10sec).....+300°C
Soldering Temperature (Reflow).....+300°C
Lead(Pb)-Free Packages .....+260°C
Packages Containing Lead(Pb).....+240°C

Electrical Characteristics

(V_{CC} = V_{LDO} = +5V, R_{OSC} = 200kΩ, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range, V_{CC}	MAX668		3		28	V
	MAX669		1.8		28	
Input Voltage Range with V_{CC} Tied to LDO			2.7		5.5	V
FB Threshold			1.225	1.250	1.275	V
FB Threshold Load Regulation	Typically 0.013% per mV on CS+; V_{CS}+ range is 0 to 100mV for 0 to full load current.			0.013		%/mV
FB Threshold Line Regulation	Typically 0.012% per % duty factor on EXT; EXT duty factor for a step-up is: 100% (1 – V_{IN}/V_{OUT})			0.012		%/%
FB Input Current	V_{FB} = 1.30V			1	20	nA
Current Limit Threshold			85	100	115	mV
Idle Mode Current-Sense Threshold			5	15	25	mV
CS+ Input Current	CS+ forced to GND			0.2	1	µA
V_{CC} Supply Current (Note 1)	V_{FB} = 1.30V, V_{CC} = 3V to 28V			220	350	µA
Shutdown Supply Current (V_{CC})	SYNC/$\overline{SHDN}$ = GND, V_{CC} = 28V			3.5	6	µA
REFERENCE AND LDO REGULATORS						
LDO Output Voltage	LDO load = ∞ to 400Ω	5V ≤ V_{CC} ≤ 28V (includes LDO dropout)	4.50	5.00	5.50	V
		3V ≤ V_{CC} ≤ 28V (includes LDO dropout)	2.65		5.50	
Undervoltage Lockout Threshold	Sensed at LDO, falling edge, hysteresis = 1%, MAX668 only		2.40	2.50	2.60	V
REF Output Voltage	No load, C_{REF} = 0.22µF		1.225	1.250	1.275	V
REF Load Regulation	REF load = 0 to 50µA			-2	-10	mV
REF Undervoltage Lockout Threshold	Rising edge, 1% hysteresis		1.0	1.1	1.2	V
OSCILLATOR						
Oscillator Frequency	R_{OSC} = 200kΩ ±1%		225	250	275	kHz
	R_{OSC} = 100kΩ ±1%		425	500	575	
	R_{OSC} = 500kΩ ±1%		85	100	115	

Electrical Characteristics (continued)

(V_{CC} = V_{LDO} = +5V, R_{OSC} = 200kΩ, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle	R_{OSC} = 200kΩ ±1%	87	90	93	%
	R_{OSC} = 100kΩ ±1%	86	90	94	
	R_{OSC} = 500kΩ ±1%	86	90	94	
Minimum EXT Pulse Width			290		ns
Minimum SYNC Input-Pulse Duty Cycle			20	45	%
Minimum SYNC Input Low Pulse Width			50	200	ns
SYNC Input Rise/Fall Time	Not tested			200	ns
SYNC Input Frequency Range		100		500	kHz
SYNC/$\overline{SHDN}$ Falling Edge to Shutdown Delay			70		µs
SYNC/$\overline{SHDN}$ Input High Voltage	3.0V < V_{CC} < 28V	2.0			V
	1.8V < V_{CC} < 3.0V (MAX669)	1.5			
SYNC/$\overline{SHDN}$ Input Low Voltage	3.0V < V_{CC} < 28V			0.45	V
	1.8V < V_{CC} < 3.0V (MAX669)			0.30	
SYNC/$\overline{SHDN}$ Input Current	$V_{SYNC/\overline{SHDN}}$ = 5V		0.5	3.0	µA
	$V_{SYNC/\overline{SHDN}}$ = 28V		1.5	6.5	
EXT Sink/Source Current	EXT forced to 2V		1		A
EXT On-Resistance	EXT high or low		2	5	Ω

Electrical Characteristics

(V_{CC} = V_{LDO} = +5V, R_{OSC} = 200kΩ, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER					
Input Voltage Range, V_{CC}	MAX668		3	28	V
	MAX669		1.8	28	
Input Voltage Range with V_{CC} Tied to LDO			2.7	5.5	V
FB Threshold			1.22	1.28	V
FB Input Current	V_{FB} = 1.30V			20	nA
Current-Limit Threshold			85	115	mV
Idle Mode Current-Sense Threshold			3	27	mV
CS+ Input Current	CS+ forced to GND			1	µA
V_{CC} Supply Current (Note 1)	V_{FB} = 1.30V, V_{CC} = 3V to 28V			350	µA
Shutdown Supply Current (V_{CC})	SYNC/$\overline{SHDN}$ = GND, V_{CC} = 28V			6	µA
REFERENCE AND LDO REGULATORS					
LDO Output Voltage	LDO load = ∞ to 400Ω	5V ≤ V_{CC} ≤ 28V (includes LDO dropout)	4.50	5.50	V
		3V ≤ V_{CC} ≤ 28V (includes LDO dropout)	2.65	5.50	
LDO Undervoltage Lockout Threshold	Sensed at LDO, falling edge, hysteresis = 1%, MAX669 only		2.40	2.60	V

Electrical Characteristics (continued)

(V_{CC} = V_{LDO} = +5V, R_{OSC} = 200kΩ, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

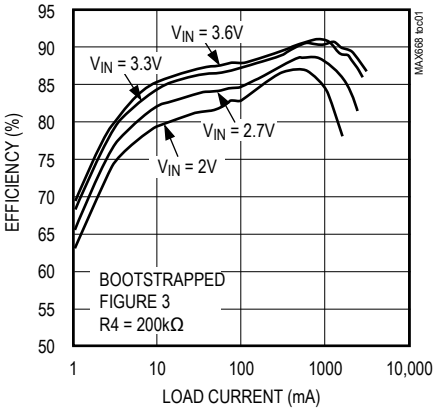
PARAMETER	CONDITIONS	MIN	MAX	UNITS
REF Output Voltage	No load, C_{REF} = 0.22µF	1.22	1.28	V
REF Load Regulation	REF load = 0 to 50µA		-10	mV
REF Undervoltage Lockout Threshold	Rising edge, 1% hysteresis	1.0	1.2	V
OSCILLATOR				
Oscillator Frequency	R_{OSC} = 200kΩ ±1%	222	278	kHz
	R_{OSC} = 100kΩ ±1%	425	575	
	R_{OSC} = 500kΩ ±1%	85	115	
Maximum Duty Cycle	R_{OSC} = 200kΩ ±1%	87	93	%
	R_{OSC} = 100kΩ ±1%	86	94	
	R_{OSC} = 500kΩ ±1%	86	94	
Minimum SYNC Input-Pulse Duty Cycle			45	%
Minimum SYNC Input Low Pulse Width			200	ns
SYNC Input Rise/Fall Time	Not tested		200	ns
SYNC Input Frequency Range		100	500	kHz
SYNC/$\overline{SHDN}$ Input High Voltage	3.0V < V_{CC} < 28V	2.0		V
	1.8V < V_{CC} < 3.0V (MAX669)	1.5		
SYNC/$\overline{SHDN}$ Input Low Voltage	3.0V < V_{CC} < 28V		0.45	V
	1.8V < V_{CC} < 3.0V (MAX669)		0.30	
SYNC/$\overline{SHDN}$ Input Current	$V_{SYNC/\overline{SHDN}}$ = 5V		3.0	µA
	$V_{SYNC/\overline{SHDN}}$ = 28V		6.5	
EXT On-Resistance	EXT high or low		5	Ω

Note 1: This is the V_{CC} current consumed when active but not switching. Does not include gate-drive current.
Note 2: Limits at T_A = -40°C are guaranteed by design.

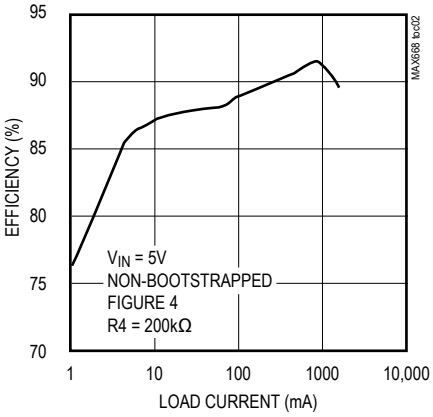
Typical Operating Characteristics

(Circuits of Figures 2, 3, 4, and 5; T_A = +25°C; unless otherwise noted.)

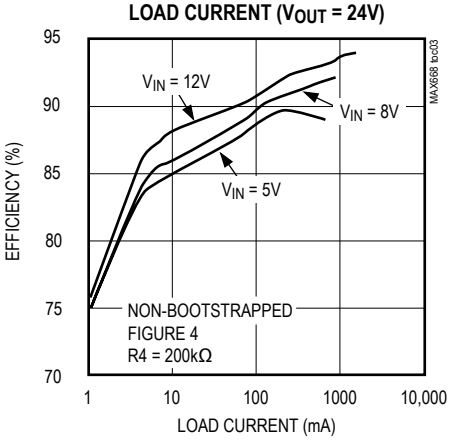
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



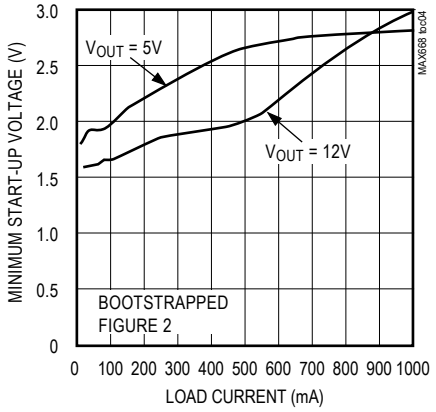
MAX668 EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 12V)



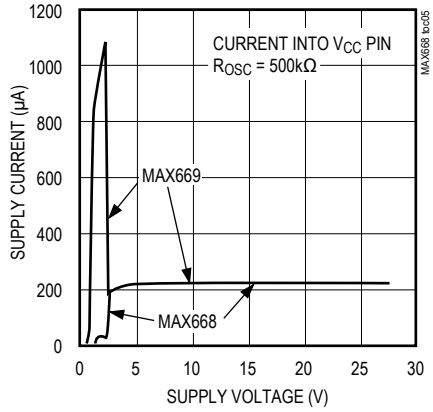
MAX668 EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 24V)



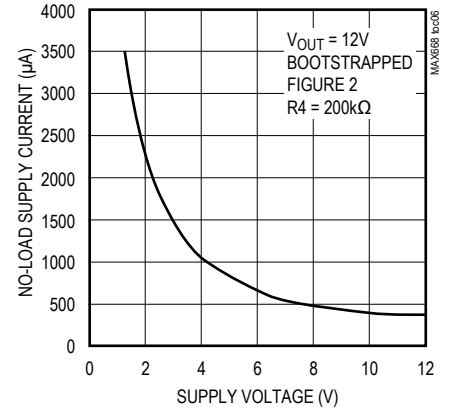
MAX669 MINIMUM START-UP VOLTAGE vs. LOAD CURRENT



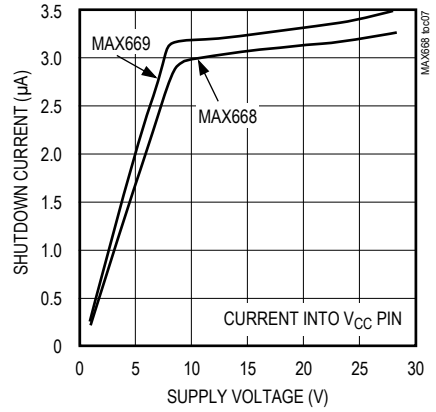
SUPPLY CURRENT vs. SUPPLY VOLTAGE



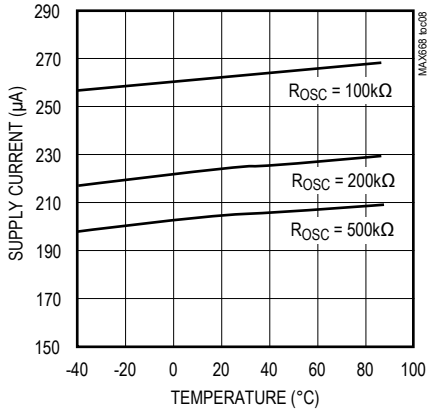
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



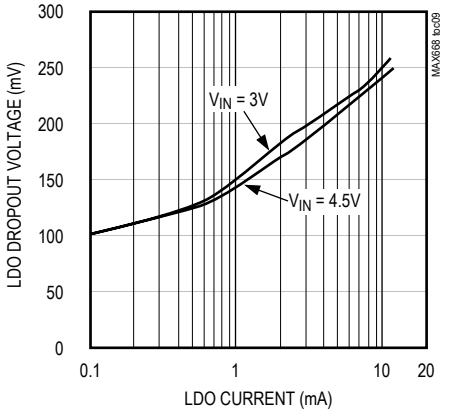
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



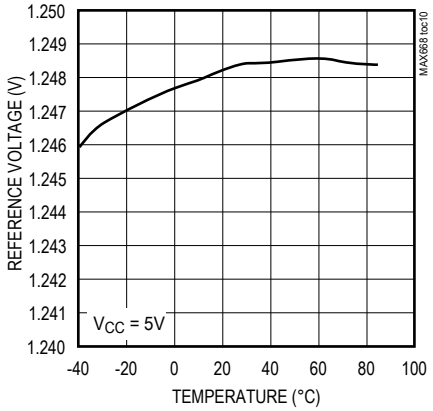
LDO DROPOUT VOLTAGE vs. LDO CURRENT



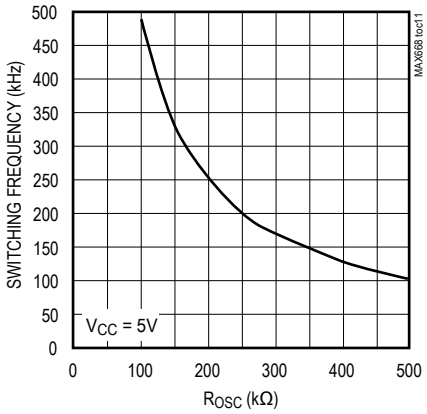
Typical Operating Characteristics (continued)

(Circuits of Figures 2, 3, 4, and 5; T_A = +25°C; unless otherwise noted.)

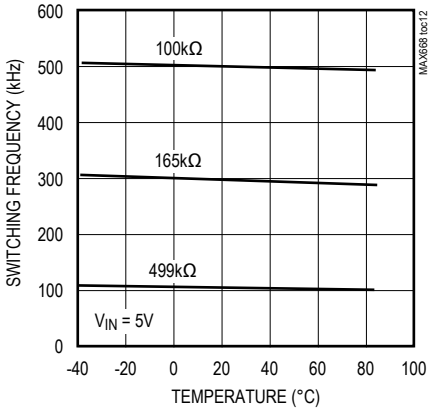
REFERENCE VOLTAGE vs. TEMPERATURE



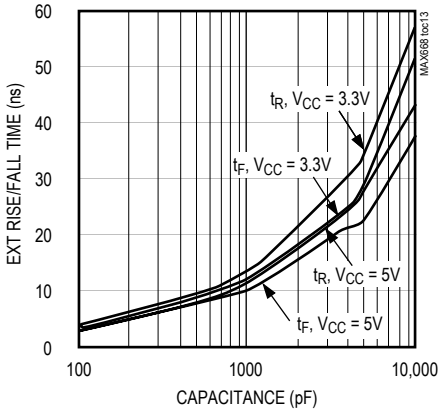
SWITCHING FREQUENCY vs. ROSC



SWITCHING FREQUENCY vs. TEMPERATURE



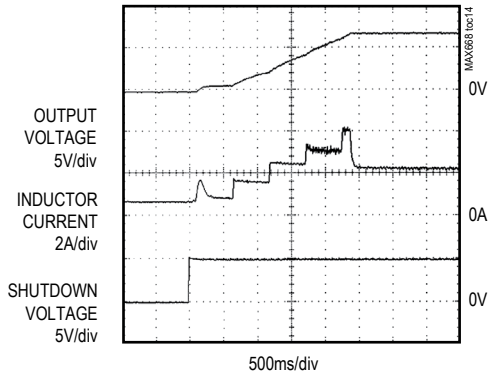
EXT RISE/FALL TIME vs. CAPACITANCE



Typical Operating Characteristics (continued)

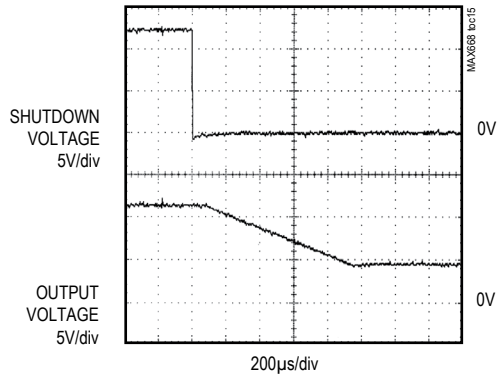
(Circuits of Figures 2, 3, 4, and 5; T_A = +25°C; unless otherwise noted.)

EXITING SHUTDOWN



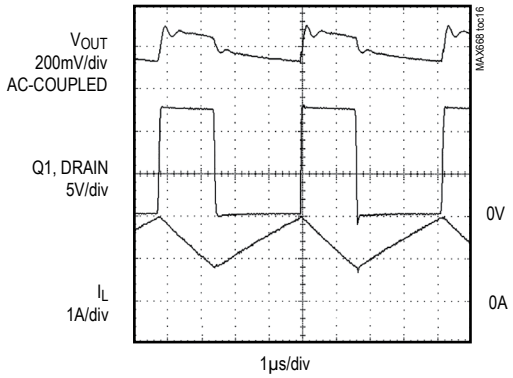
MAX668, V_{IN} = 5V, V_{OUT} = 12V, LOAD = 1.0A, R_{OSC} = 100kW, LOW VOLTAGE, NON-BOOTSTRAPPED

ENTERING SHUTDOWN



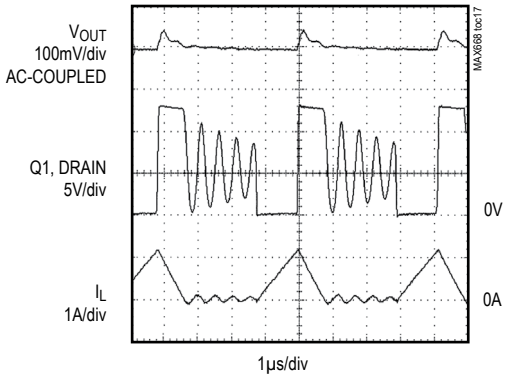
MAX668, V_{IN} = 5V, V_{OUT} = 12V, LOAD = 1.0A, LOW VOLTAGE, NON-BOOTSTRAPPED

HEAVY-LOAD SWITCHING WAVEFORM



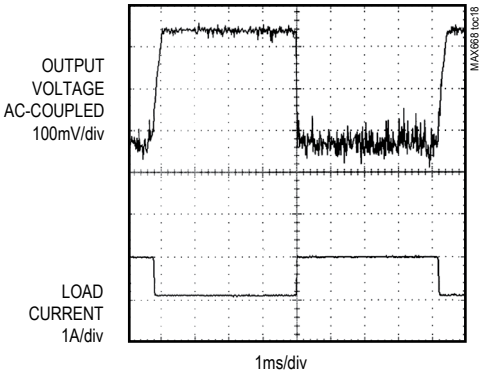
MAX668, V_{IN} = 5V, V_{OUT} = 12V, I_{LOAD} = 1.0A, LOW VOLTAGE, NON-BOOTSTRAPPED

LIGHT-LOAD SWITCHING WAVEFORM



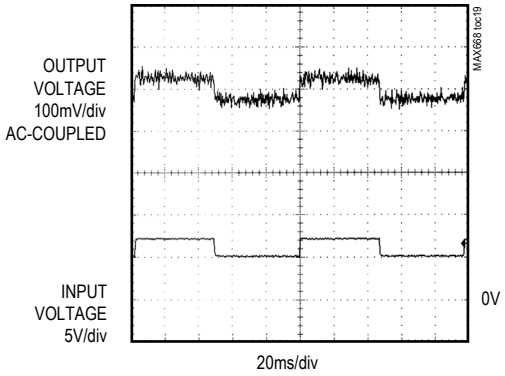
MAX668, V_{IN} = 5V, V_{OUT} = 12V, I_{LOAD} = 0.1A, LOW VOLTAGE, NON-BOOTSTRAPPED

LOAD-TRANSIENT RESPONSE



MAX668, V_{IN} = 5V, V_{OUT} = 12V, I_{LOAD} = 0.1A TO 1.0A, LOW VOLTAGE, NON-BOOTSTRAPPED

LINE-TRANSIENT RESPONSE



MAX668, V_{IN} = 5V TO 8V, V_{OUT} = 12V, LOAD = 1.0A, HIGH VOLTAGE, NON-BOOTSTRAPPED

Pin Description

PIN	NAME	FUNCTION
1	LDO	5V On-Chip Regulator Output. This regulator powers all internal circuitry including the EXT gate driver. Bypass LDO to GND with a 1µF or greater ceramic capacitor.
2	FREQ	Oscillator Frequency Set Input. A resistor from FREQ to GND sets the oscillator from 100kHz (R_{OSC} = 500kΩ) to 500kHz (R_{OSC} = 100kΩ). $f_{OSC} = 5 \times 10^{10} / R_{OSC}$. R_{OSC} is still required if an external clock is used at SYNC/$\overline{SHDN}$. (See *SYNC/$\overline{SHDN}$ and FREQ Inputs* section.)
3	GND	Analog Ground
4	REF	1.25V Reference Output. REF can source 50µA. Bypass to GND with a 0.22µF ceramic capacitor.
5	FB	Feedback Input. The FB threshold is 1.25V.
6	CS+	Positive Current-Sense Input. Connect a current-sense resistor, R_{CS}, between CS+ and PGND.
7	PGND	Power Ground for EXT Gate Driver and Negative Current-Sense Input
8	EXT	External MOSFET Gate-Driver Output. EXT swings from LDO to PGND.
9	V_{CC}	Input Supply to On-Chip LDO Regulator. V_{CC} accepts inputs up to 28V. Bypass to GND with a 0.1µF ceramic capacitor.
10	SYNC/$\overline{SHDN}$	Shutdown control and Synchronization Input. There are three operating modes: • SYNC/$\overline{SHDN}$ low: DC-DC off. • SYNC/$\overline{SHDN}$ high: DC-DC on with oscillator frequency set at FREQ by R_{OSC}. • SYNC/$\overline{SHDN}$ clocked: DC-DC on with operating frequency set by SYNC clock input. DC-DC conversion cycles initiate on rising edge of input clock.

Detailed Description

The MAX668/MAX669 current-mode PWM controllers operate in a wide range of DC-DC conversion applications, including boost, SEPIC, flyback, and isolated output configurations. Optimum conversion efficiency is maintained over a wide range of loads by employing both PWM operation and Maxim's proprietary Idle Mode control to minimize operating current at light loads. Other features include shutdown, adjustable internal operating frequency or synchronization to an external clock, soft start, adjustable current limit, and a wide (1.8V to 28V) input range.

MAX668 vs. MAX669 Differences

Differences between the MAX668 and MAX669 relate to their use in bootstrapped or non-bootstrapped circuits (Table 1). The MAX668 operates with inputs as low as 3V and can be connected in *either* a bootstrapped or non-bootstrapped (IC powered from input supply or other source) configuration. When not bootstrapped, the MAX668 has no restriction on output voltage. When bootstrapped, the output cannot exceed 28V.

The MAX669 is optimized for low input voltages (down to 1.8V) and *requires* bootstrapped operation (IC powered from V_{OUT}) with output voltages no greater than 28V. Bootstrapping is required because the MAX669 does not have undervoltage lockout, but instead drives EXT with an open-loop, 50% duty-cycle start-up oscillator when LDO is below 2.5V. It switches to closed-loop operation only when LDO exceeds 2.5V. If a non-bootstrapped connection is used with the MAX669 and if V_{CC} (the input voltage) remains below 2.7V, the output voltage will soar above the regulation point. Table 2 recommends the appropriate device for each biasing option.

Table 1. MAX668/MAX669 Comparison

FEATURE	MAX668	MAX669
V_{CC} Input Range	3V to 28V	1.8V to 28V
Operation	Bootstrapped or nonbootstrapped. V_{CC} can be connected to input, output, or other voltage source such as a logic supply.	Must be bootstrapped (V_{CC} must be connected to boosted output voltage, V_{OUT}).
Undervoltage Lockout	IC stops switching for LDO below 2.5V.	No
Soft-Start	Yes	When LDO is above 2.5V

PWM Controller

The heart of the MAX668/MAX669 current-mode PWM controller is a BiCMOS multi-input comparator that simultaneously processes the output-error signal, the current-sense signal, and a slope-compensation ramp (Figure 1). The main PWM comparator is direct summing, lacking a traditional error amplifier and its associated phase shift. The direct summing configuration approaches ideal cycle-by-cycle control over the output voltage since there is no conventional error amp in the feedback path.

In PWM mode, the controller uses fixed-frequency, current-mode operation where the duty ratio is set by the input/output voltage ratio (duty ratio = (V_{OUT} - V_{IN})/V_{IN} in the boost configuration). The current-mode feedback loop regulates peak inductor current as a function of the output error signal.

At light loads the controller enters Idle mode. During Idle mode, switching pulses are provided only as needed to service the load, and operating current is minimized to provide best light-load efficiency. The minimum-current comparator threshold is 15mV, or 15% of the full-load value (I_{MAX}) of 100mV. When the controller is synchronized to an external clock, Idle Mode occurs only at very light loads.

Bootstrapped/Non-Bootstrapped Operation

Low-Dropout Regulator (LDO)

Several IC biasing options, including bootstrapped and non-bootstrapped operation, are made possible by an on-chip, low-dropout 5V regulator. The regulator input is at V_{CC}, while its output is at LDO. All MAX668/MAX669 functions, including EXT, are internally powered from LDO. The V_{CC}-to-LDO dropout voltage is typically 200mV (300mV max at 12mA), so that when V_{CC} is less than 5.2V, LDO is typically V_{CC} - 200mV. When LDO is in dropout, the MAX668/MAX669 still operate with V_{CC} as low as 3V (as long as LDO exceeds 2.7V), but with reduced amplitude FET drive at EXT. The maximum V_{CC} input voltage is 28V.

LDO can supply up to 12mA to power the IC, supply gate charge through EXT to the external FET, and supply small external loads. When driving particularly large FETs at high switching rates, little or no LDO current may be available for external loads. For example, when switched at 500kHz, a large FET with 20nC gate charge requires 20nC x 500kHz, or 10mA.

V_{CC} and LDO allow a variety of biasing connections to optimize efficiency, circuit quiescent current, and full-load start-up behavior for different input and output voltage ranges. Connections are shown in Figure 2, Figure 3, Figure 4, and Figure 5. The characteristics of each are outlined in Table 1.

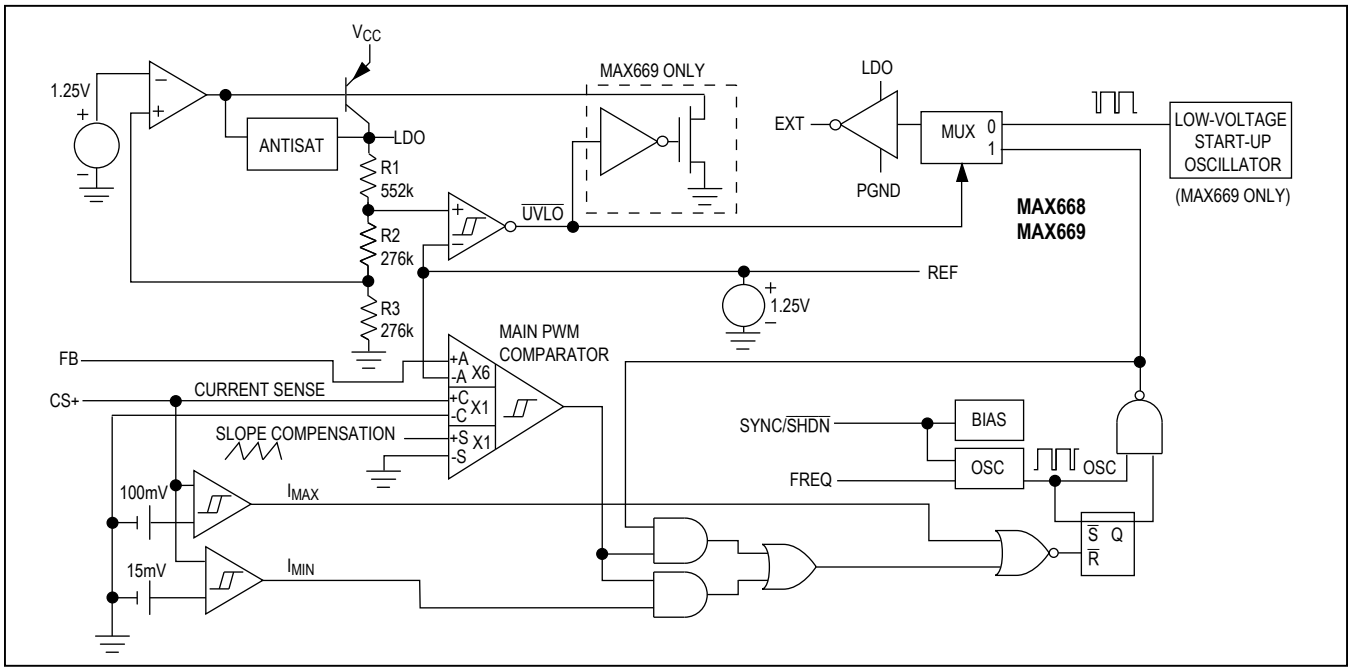


Figure 1. MAX668/MAX669 Functional Diagram

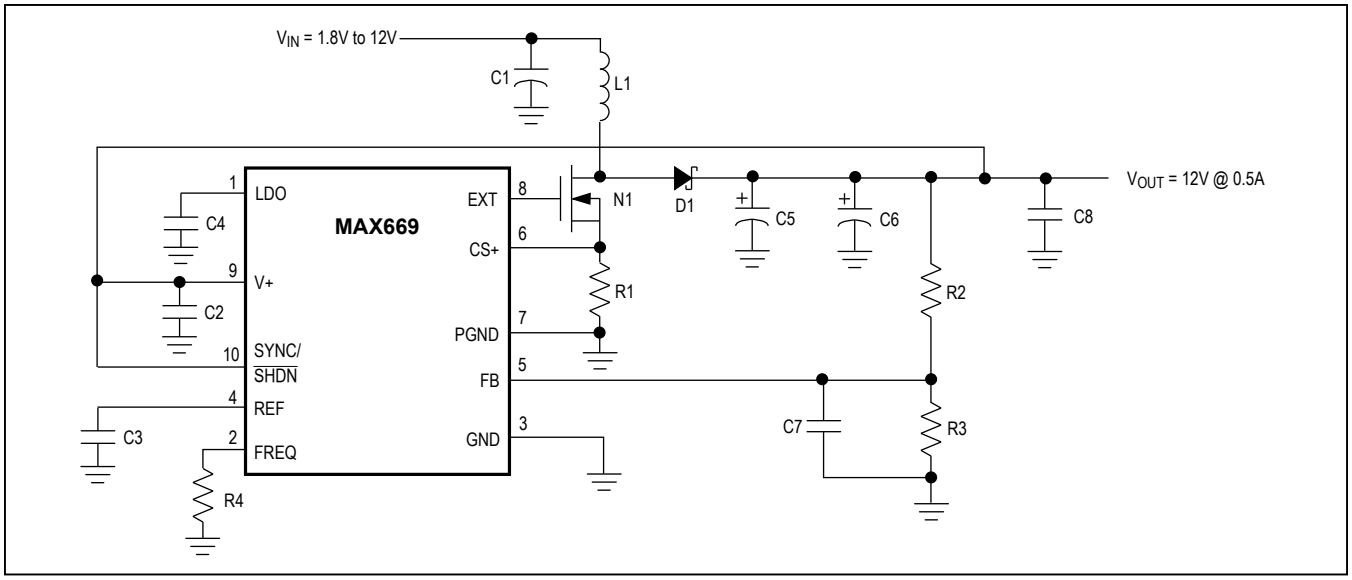


Figure 2. MAX669 High-Voltage Bootstrapped Configuration

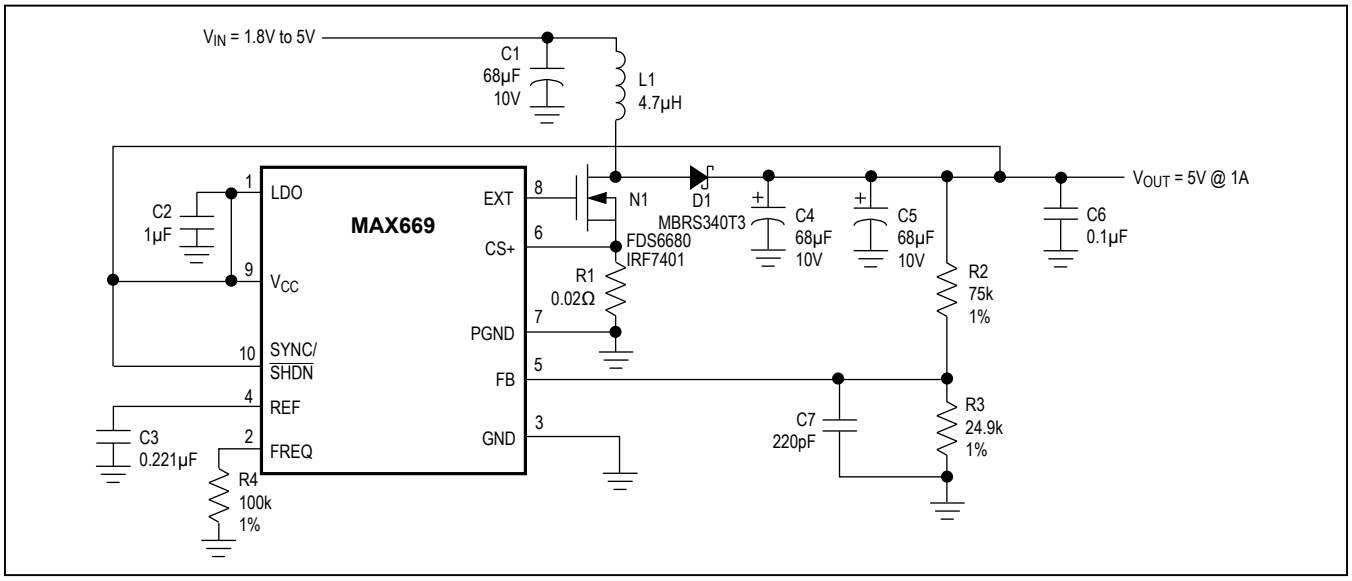


Figure 3. MAX669 Low-Voltage Bootstrapped Configuration

Bootstrapped Operation

With bootstrapped operation, the IC is powered from the circuit output (V_{OUT}). This improves efficiency when the input voltage is low, since EXT drives the FET with a higher gate voltage than would be available from the low-voltage input. Higher gate voltage reduces the FET on-resistance, increasing efficiency. Other (undesirable) characteristics of bootstrapped operation are increased IC operating power (since it has a higher operating voltage) and reduced ability to start up with high load current at low input voltages. If the input voltage range extends below 2.7V, then bootstrapped operation with the MAX669 is the only option.

With V_{CC} connected to V_{OUT}, as in Figure 2, EXT voltage swing is 5V when V_{CC} is 5.2V or more, and V_{CC} - 0.2V when V_{CC} is less than 5.2V. If the output voltage does not exceed 5.5V, the on-chip regulator can be disabled by connecting V_{CC} to LDO (Figure 3). This eliminates the LDO forward drop and supplies maximum gate drive to the external FET.

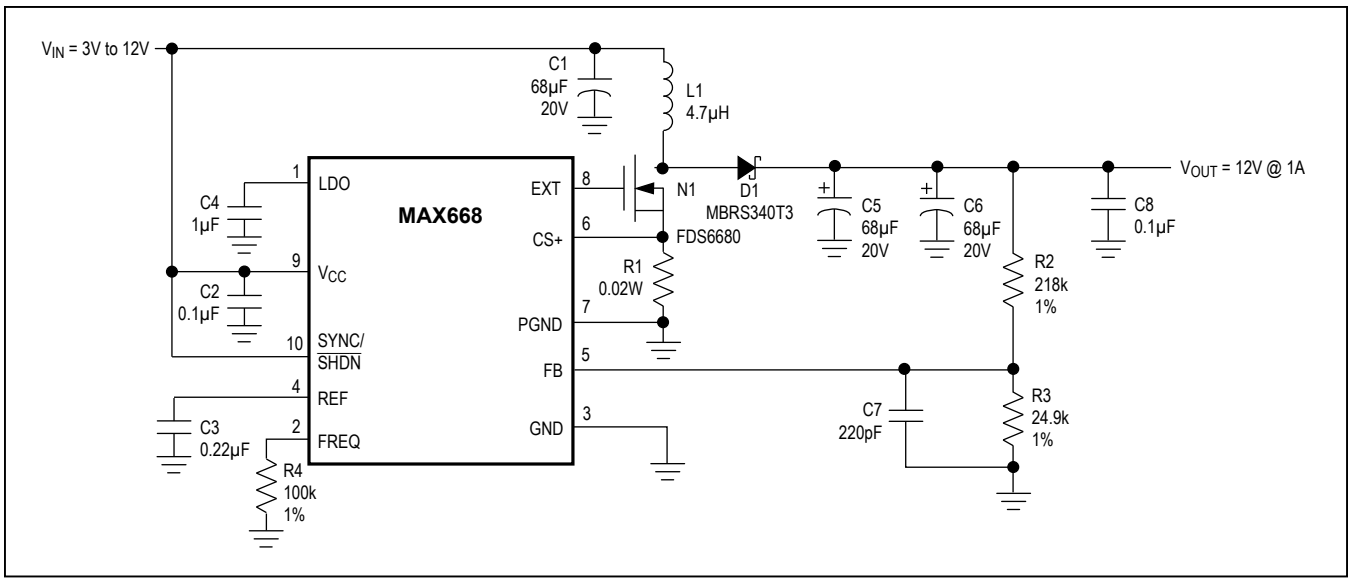


Figure 4. MAX668 High-Voltage Non-Bootstrapped Configuration

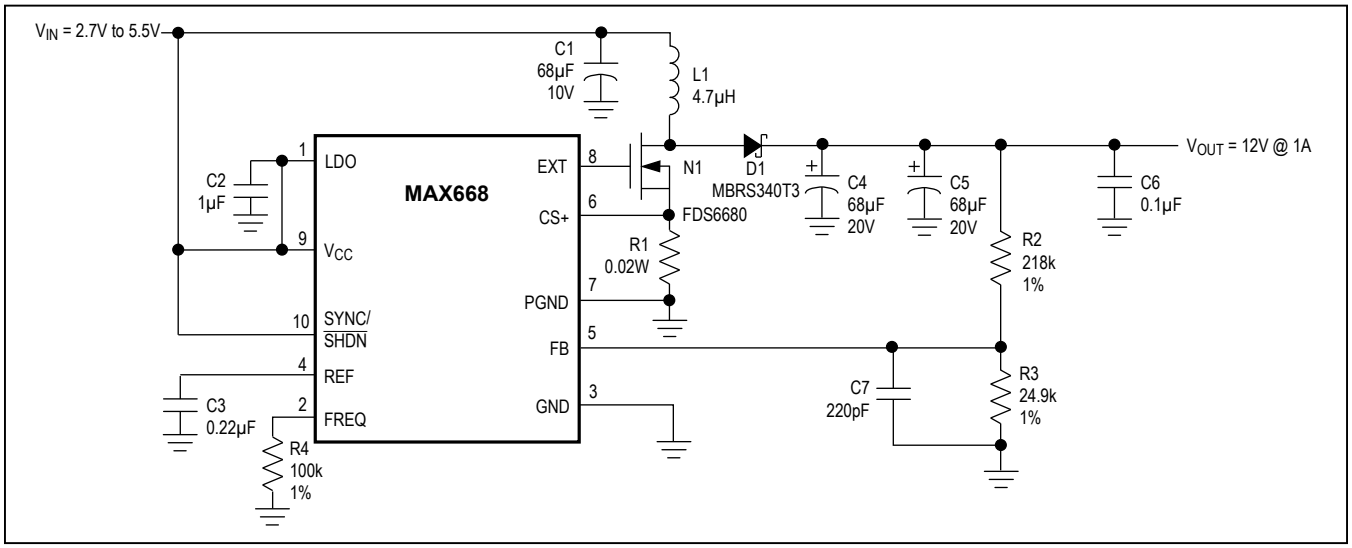


Figure 5. MAX668 Low-Voltage Non-Bootstrapped Configuration

Non-Bootstrapped Operation

With non-bootstrapped operation, the IC is powered from the input voltage (V_{IN}) or another source, such as a logic supply. Non-bootstrapped operation (Figure 4) is recommended (but not required) for input voltages above 5V, since the EXT amplitude (limited to 5V by LDO) at this voltage range is no higher than it would be with bootstrapped operation. Note that non-bootstrapped operation is *required* if the output voltage exceeds 28V, since this level is too high to safely connect to V_{CC}. Also note that **only the MAX668 can be used with non-bootstrapped operation**.

If the input voltage does not exceed 5.5V, the on-chip regulator can be disabled by connecting V_{CC} to LDO (Figure 5). This eliminates the regulator forward drop and supplies the maximum gate drive to the external FET for lowest on-resistance. Disabling the regulator also reduces the non-bootstrapped minimum input voltage from 3V to 2.7V.

Table 2. Bootstrapped and Non-Bootstrapped Configurations

CONFIGURATION	FIGURE	USE WITH:	INPUT VOLTAGE RANGE* (V)	OUTPUT VOLTAGE RANGE (V)	COMMENTS
High-Voltage, Bootstrapped	Figure2	MAX669	1.8 to 28	3V to 28	**Connect V_{CC} to V_{OUT}**. Provides maximum external FET gate drive for low-voltage (Input <3V) to high-voltage (output >5.5V) boost circuits. V_{OUT} cannot exceed 28V.
Low-Voltage, Bootstrapped	Figure3	MAX669	1.8 to 5.5	2.7 to 5.5	**Connect V_{OUT} to V_{CC} and LDO**. Provides maximum possible external FET gate drive for low-voltage designs, but limits V_{OUT} to 5.5V or less.
High-Voltage, Non-Bootstrapped	Figure4	MAX668	3 to 28	V_{IN} to ∞	**Connect V_{IN} to V_{CC}**. Provides widest input and output range, but external FET gate drive is reduced for V_{IN} below 5V.
Low-Voltage, Non-Bootstrapped	Figure5	MAX668	2.7 to 5.5	V_{IN} to ∞	**Connect V_{IN} to V_{CC} and LDO**. FET gate-drive amplitude = V_{IN} for logic-supply (input 3V to 5.5V) to high-voltage (output >5.5V) boost circuits. IC operating power is less than in Figure 4, since IC current does not pass through the LDO regulator.
Extra IC supply, Non-Bootstrapped	None	MAX668	Not Restricted	V_{IN} to ∞	**Connect V_{CC} and LDO to a separate supply (V_{BIAS}) that powers only the IC**. FET gate-drive amplitude = V_{BIAS}. Input power source (V_{IN}) and output voltage range (V_{OUT}) are not restricted, except that V_{OUT} must exceed V_{IN}.

** For standard step-up DC-DC circuits (as in Figures 2, 3, 4, and 5), regulation cannot be maintained if V_{IN} exceeds V_{OUT}. SEPIC and transformer-based circuits do not have this limitation.*

In addition to the configurations shown in Table 2, the following guidelines may help when selecting a configuration:

1) If V_{IN} is ever below 2.7V, V_{CC} *must* be bootstrapped to V_{OUT} and the MAX669 must be used. If V_{OUT} never exceeds 5.5V, LDO may be shorted to V_{CC} and V_{OUT} to eliminate the dropout voltage of the LDO regulator.
2) If V_{IN} is greater than 3.0V, V_{CC} can be powered from V_{IN}, rather than from V_{OUT} (non-bootstrapped). This can save quiescent power consumption, especially when V_{OUT} is large. If V_{IN} never exceeds 5.5V, LDO may be shorted to V_{CC} and V_{IN} to eliminate the dropout voltage of the LDO regulator.
3) If V_{IN} is in the 3V to 4.5V range (i.e., 1-cell Li-Ion or 3-cell NiMH battery range), bootstrapping V_{CC} from V_{OUT}, although not required, may increase overall efficiency by increasing gate drive (and reducing FET resistance) at the expense of quiescent power consumption.
4) If V_{IN} always exceeds 4.5V, V_{CC} should be tied to V_{IN}, since bootstrapping from V_{OUT} does not increase gate drive from EXT but does increase quiescent power dissipation.

SYNC/$\overline{SHDN}$ and FREQ Inputs

The SYNC/$\overline{SHDN}$ pin provides both external-clock synchronization (if desired) and shutdown control. When SYNC/$\overline{SHDN}$ is low, all IC functions are shut down. A logic high at SYNC/$\overline{SHDN}$ selects operation at a frequency set by R_{OSC}, connected from FREQ to GND. The relationship between f_{OSC} and R_{OSC} is:

$$R_{OSC} = 5 \times 10^{10}/f_{OSC}$$

So a 500kHz operating frequency, for example, is set with R_{OSC} = 100kΩ.

Rising clock edges on SYNC/$\overline{SHDN}$ are interpreted as synchronization inputs. If the sync signal is lost while SYNC/$\overline{SHDN}$ is high, the internal oscillator takes over at the end of the last cycle and the frequency is returned to the rate set by R_{OSC}. If sync is lost with SYNC/$\overline{SHDN}$ low, the IC waits for 70µs before shutting down. This maintains output regulation even with intermittent sync signals. When an external sync signal is used, Idle mode switchover at the 15mV current-sense threshold is disabled so that Idle mode only occurs at very light loads. Also, R_{OSC} should be set for a frequency 15% below the SYNC clock rate:

$$R_{OSC(SYNC)} = 5 \times 10^{10} / (0.85 \times f_{SYNC})$$

Soft-Start

The MAX668/MAX669 feature a “digital” soft start which is preset and requires no external capacitor. Upon startup, the peak inductor increments from 1/5 of the value set by R_{CS}, to the full current-limit value, in five steps over 1024 cycles of f_{OSC} or f_{SYNC}. For example, with an f_{OSC} of 200kHz, the complete soft-start sequence takes 5ms. See the *Typical Operating Characteristics* for a photo of soft-start operation. Soft-start is implemented: 1) when power is first applied to the IC, 2) when exiting shutdown with power already applied, and 3) when exiting undervoltage lockout. The MAX669’s soft-start sequence does not start until LDO reaches 2.5V.

Design Procedure

The MAX668/MAX669 can operate in a number of DCDC converter configurations including step-up, SEPIC (single-ended primary inductance converter), and flyback. The following design discussions are limited to step-up, although SEPIC and flyback examples are shown in the *Application Circuits* section.

Setting the Operating Frequency

The MAX668/MAX669 can be set to operate from 100kHz to 500kHz. Choice of operating frequency will depend on number of factors:

1) Noise considerations may dictate setting (or synchronizing) f_{OSC} above or below a certain frequency or band of frequencies, particularly in RF applications.
2) Higher frequencies allow the use of smaller value (hence smaller size) inductors and capacitors.
3) Higher frequencies consume more operating power both to operate the IC and to charge and discharge the gate of the external FET. This tends to reduce efficiency at light loads; however, the MAX668/MAX669’s Idle mode feature substantially increases light-load efficiency.
4) Higher frequencies may exhibit poorer overall efficiency due to more transition losses in the FET; however, this shortcoming can often be nullified by trading some of the inductor and capacitor size benefits for lower-resistance components.

The oscillator frequency is set by a resistor, R_{OSC}, connected from FREQ to GND. R_{OSC} must be connected whether or not the part is externally synchronized R_{OSC} is in each case:

$$R_{OSC} = 5 \times 10^{10} / f_{OSC}$$

when *not* using an external clock.

$$R_{OSC(SYNC)} = 5 \times 10^{10} / (0.85 \times f_{SYNC})$$

when using an external clock, f_{SYNC}.

Setting the Output Voltage

The output voltage is set by two external resistors (R2 and R3, Figure 2, Figure 3, Figure 4, and Figure 5). First select a value for R3 in the 10kΩ to 1MΩ range. R2 is then given by:

$$R2 = R3 [(V_{OUT}/V_{REF}) - 1]$$

where V_{REF} is 1.25V.

Determining Inductance Value

For most MAX668/MAX669 boost designs, the inductor value (L_{IDEAL}) can be derived from the following equation, which picks the optimum value for stability based on the MAX668/MAX669’s internally set slope compensation:

$$L_{IDEAL} = V_{OUT} / (4 \times I_{OUT} \times f_{OSC})$$

The MAX668/MAX669 allow significant latitude in inductor selection if L_{IDEAL} is not a convenient value. This may happen if L_{IDEAL} is a not a standard inductance (such as 10µH, 22µH, etc.), or if L_{IDEAL} is too large to be obtained with suitable resistance and saturation-current rating in the desired size. Inductance values smaller than L_{IDEAL} may be used with no adverse stability effects; however, the peak-to-peak inductor current (I_{LPP}) will rise as L is reduced. This has the effect of raising the required I_{LPK} for a given output power and also requiring larger output capacitance to maintain a given output ripple. An inductance value larger than L_{IDEAL} may also be used, but output-filter capacitance must be increased by the same proportion that L has to L_{IDEAL}. See the *Capacitor Selection* section for more information on determining output filter values.

Due to the MAX668/MAX669's high switching frequencies, inductors with any core materials that exhibit low core loss (ferrite, or equivalent) are recommended for best efficiency performance.

Determining Peak Inductor Current

The peak inductor current required for a particular output is:

$$I_{LPEAK} = I_{LDC} + (I_{LPP} / 2)$$

where I_{LDC} is the average DC input current and I_{LPP} is the inductor peak-to-peak ripple current. The I_{LDC} and I_{LPP} terms are determined as follows:

$$I_{LDC} = \frac{I_{OUT}\ (V_{OUT} + V_D)}{(V_{IN} - V_{SW})}$$

where V_D is the forward voltage drop across the Schottky rectifier diode (D1), and V_{SW} is the drop across the external FET, when on.

$$I_{LPP} = \frac{(V_{IN} - V_{SW})\ (V_{OUT} + V_D - V_{IN})}{L \times f_{OSC}\ \ (V_{OUT} + V_D)}$$

where L is the inductor value. The saturation rating of the selected inductor should meet or exceed the calculated value for I_{LPEAK}, although most coil types can be operated up to 20% over their saturation rating without difficulty. In addition to the saturation criteria, the inductor should have as low a series resistance as possible. For continuous inductor current, the power loss in the inductor resistance, P_{LR}, is approximated by:

$$P_{LR} \cong (I_{OUT} \times V_{OUT} / V_{IN})^2 \times R_L$$

where R_L is the inductor series resistance.

Once the peak inductor current is selected, the current-sense resistor (R_{CS}) is determined by:

$$R_{CS} = 85mV / I_{LPEAK}$$

For high peak inductor currents (>1A), Kelvin sensing connections should be used to connect CS+ and PGND to R_{CS}. PGND and GND should be tied together at the ground side of R_{CS}.

Power MOSFET Selection

The MAX668/MAX669 drive a wide variety of N-channel power MOSFETs (NFETs). Since LDO limits the EXT output gate drive to no more than 5V, a logic-level NFET is required. Best performance, especially at low input voltages (below 5V), is achieved with low-threshold NFETs that specify on-resistance with a gate-source voltage (V_{GS}) of 2.7V or less. When selecting an NFET, key parameters can include:

1) Total gate charge (Q_g)
2) Reverse transfer capacitance or charge (C_{RSS})
3) On-resistance ($R_{DS(ON)}$)
4) Maximum drain-to-source voltage ($V_{DS(MAX)}$)
5) Minimum threshold voltage ($V_{TH(MIN)}$)

At high switching rates, dynamic characteristics (parameters 1 and 2 above) that predict switching losses may have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Q_g includes all capacitances associated with charging the gate. In addition, this parameter helps predict the current needed to drive the gate at the selected operating frequency. The continuous LDO current for the FET gate is:

$$I_{GATE} = Q_g \times f_{OSC}$$

For example, the MMFT3055L has a typical Q_g of 7nC (at V_{GS} = 5V); therefore, the I_{GATE} current at 500kHz is 3.5mA. Use the FET manufacturer's *typical* value for Q_g in the above equation, since a maximum value (if supplied) is usually too conservative to be of use in estimating I_{GATE}.

Diode Selection

The MAX668/MAX669's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Ensure that the diode's average current rating is adequate using the diode manufacturer's data, or approximate it with the following formula:

$$I_{DIODE} = I_{OUT} + \frac{I_{LPEAK} - I_{OUT}}{3}$$

Also, the diode reverse breakdown voltage must exceed V_{OUT}. For high output voltages (50V or above), Schottky diodes may not be practical because of this voltage requirement. In these cases, use a high-speed silicon rectifier with adequate reverse voltage.

Capacitor Selection

Output Filter Capacitor

The minimum output filter capacitance that ensures stability is:

$$C_{OUT(MIN)} = \frac{(7.5V \times L / L_{IDEAL})}{(2\pi R_{CS} \times V_{IN(MIN)} \times f_{OSC})}$$

where $V_{IN(MIN)}$ is the minimum expected input voltage. Typically $C_{OUT(MIN)}$, though sufficient for stability, will not be adequate for low output voltage ripple. Since output ripple in boost DC-DC designs is dominated by capacitor equivalent series resistance (ESR), a capacitance value 2 or 3 times larger than $C_{OUT(MIN)}$ is typically needed. Low-ESR types must be used. Output ripple due to ESR is:

$$V_{RIPPLE(ESR)} = I_{LPEAK} \times ESR_{COUT}$$

Input Capacitor

The input capacitor (C_{IN}) in boost designs reduces the current peaks drawn from the input supply and reduces noise injection. The value of C_{IN} is largely determined by the source impedance of the input supply. High source impedance requires high input capacitance, particularly as the input voltage falls. Since step-up DC-DC converters act as “constant-power” loads to their input supply, input current rises as input voltage falls. Consequently, in low-input-voltage designs, increasing C_{IN} and/or lowering its ESR can add as many as five percentage points to conversion efficiency. A good starting point is to use the same capacitance value for C_{IN} as for C_{OUT}.

Bypass Capacitors

In addition to C_{IN} and C_{OUT}, three ceramic bypass capacitors are also required with the MAX668/MAX669. Bypass REF to GND with 0.22µF or more. Bypass LDO to GND with 1µF or more. And bypass V_{CC} to GND with 0.1µF or more. All bypass capacitors should be located as close to their respective pins as possible.

Compensation Capacitor

Output ripple voltage due to C_{OUT} ESR affects loop stability by introducing a left half-plane zero. A small capacitor connected from FB to GND forms a pole with the feedback resistance that cancels the ESR zero. The optimum compensation value is:

$$C_{FB} = C_{OUT} \times \frac{ESR_{COUT}}{(R2 \times R3) / (R2 + R3)}$$

where R2 and R3 are the feedback resistors (Figure 2, Figure 3, Figure 4, and Figure 5). If the calculated value for C_{FB} results in a non-standard capacitance value, values from $0.5C_{FB}$ to $1.5C_{FB}$ will also provide sufficient compensation.

Applications Information

Starting Under Load

In non-bootstrapped configurations (Figure 4, and Figure 5), the MAX668 can start up with any combination of output load and input voltage at which it can operate when already started. In other words, there are no special limitations to start up in non-bootstrapped circuits.

In bootstrapped configurations with the MAX668 or MAX669, there may be circumstances where full load current can only be applied after the circuit has started and the output is near its set value. As the input voltage drops, this limitation becomes more severe. This characteristic of all bootstrapped designs occurs when the MOSFET gate is not fully driven until the output voltage rises. This is problematic because a heavily loaded output cannot rise until the MOSFET has low on-resistance. In such situations, low-threshold FETs ($V_{TH} < V_{IN(MIN)}$) are the most effective solution. The *Typical Operating Characteristics* section shows plots of startup voltage versus load current for a typical bootstrapped design.

Layout Considerations

Due to high current levels and fast switching waveforms that radiate noise, proper PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting GND, PGND, the input bypass-capacitor ground lead, and the output-filter ground lead to a single point (star ground configuration). Also, minimize trace lengths to reduce stray capacitance, trace resistance, and radiated noise. The trace between the external gain-setting resistors and the FB pin must be extremely short, as must the trace between GND and PGND.

Application Circuits

Low-Voltage Boost Circuit

Figure 3 shows the MAX669 operating in a low-voltage boost application. The MAX669 is configured in the bootstrapped mode to improve low input voltage performance. The IRF7401 nMOSFET was selected for Q1 in this application because of its very low 0.7V gate threshold voltage (V_{GS}). This circuit provides a 5V output at greater than 2A of output current and operates with input voltages as low as 1.8V. Efficiency is typically in the 85% to 90% range.

+12V Boost Application

Figure 5 shows the MAX668 operating in a 5V to 12V boost application. This circuit provides output currents of greater than 1A at a typical efficiency of 92%. The MAX668 is operated in non-bootstrapped mode to minimize the input supply current. This achieves maximum light-load efficiency. If input voltages below 5V are used, the IC should be operated in bootstrapped mode to achieve best low-voltage performance.

4-Cell to +5V SEPIC Power Supply

Figure 6 shows the MAX668 in a SEPIC (single-ended primary inductance converter) configuration. This configuration is useful when the input voltage can be either larger or smaller than the output voltage, such as when converting four NiMH, NiCd, or Alkaline cells to a 5V output. The SEPIC configuration is often a good choice for combined step-up/step-down applications.

The nMOSFET (Q1) must be selected to withstand a drain-to-source voltage (V_{DS}) greater than the sum of the input and output voltages. The coupling capacitor (C2) must be a low-ESR type to achieve maximum efficiency. C2 must also be able to handle high ripple currents; ordinary tantalum capacitors should not be used for high-current designs.

The circuit in Figure 6 provides greater than 1A output current at 5V when operating with an input voltage from 3V to 25V. Efficiency will typically be between 70% and 85%, depending upon the input voltage and output current.

Isolated +5V to +5V Power Supply

The circuit of Figure 7 provides a 5V isolated output at 400mA from a 5V input power supply. Transformer T1 provides electrical isolation for the forward path of the converter, while the TLV431 shunt regulator and MOC211 opto-isolator provide an isolated feedback error voltage for the converter. The output voltage is set by resistors R2 and R3 such that the mid-point of the divider is 1.24V (threshold of TLV431). Output voltage can be adjusted from 1.24V to 6V by selecting the proper ratio for R2 and R3. For output voltages greater than 6V, substitute the TL431 for the TLV431, and use 2.5V as the voltage at the midpoint of the voltage-divider.

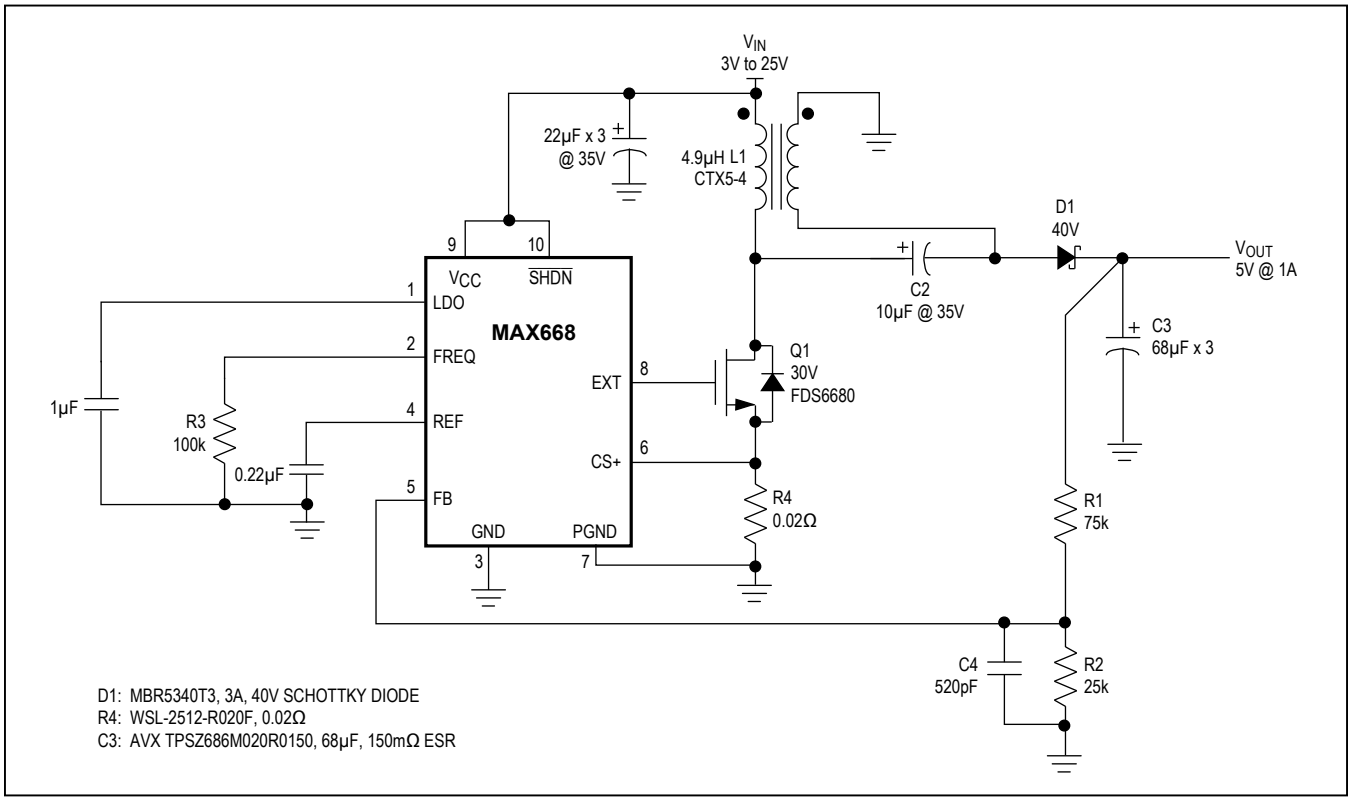


Figure 6. MAX668 in SEPIC Configuration

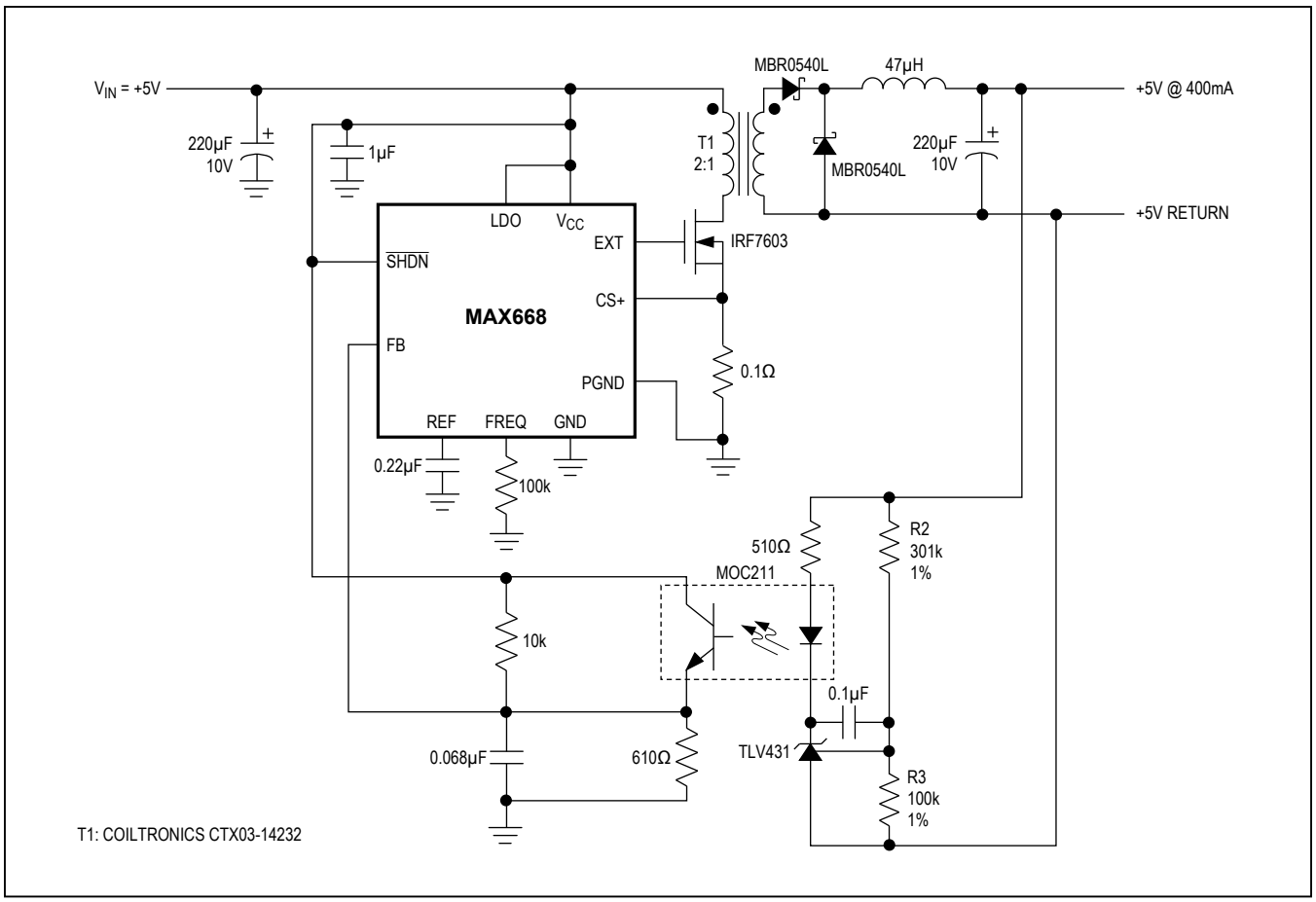


Figure 7. Isolated +5V to +5V at 400mA Power Supply

Package Information

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PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10-2	21-0061	90-0330

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	1/12	Added automotive qualified part and updated lead-free and leaded soldering temperatures	1, 2
3	6/16	Updated verbiage in *Determining Inductance Value* section	14

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