Ordering Information

Part Number	Options RoHS Compliant	Package	Surface Mount	Gullwing	Tape & Reel	Quantity
ACPL-312T	-000E	DIP 8				50 per tube
	-300E	DIP 8 Gullwing	X	X		50 per tube
	-500E		X	X	X	1000 per reel

Note:- option x20E for UL1577 5000Vrms for 1minute will be offered upon request

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-312T-500E to order product of gullwing DIP-8 package in Tape and Reel packaging with RoHS compliant.

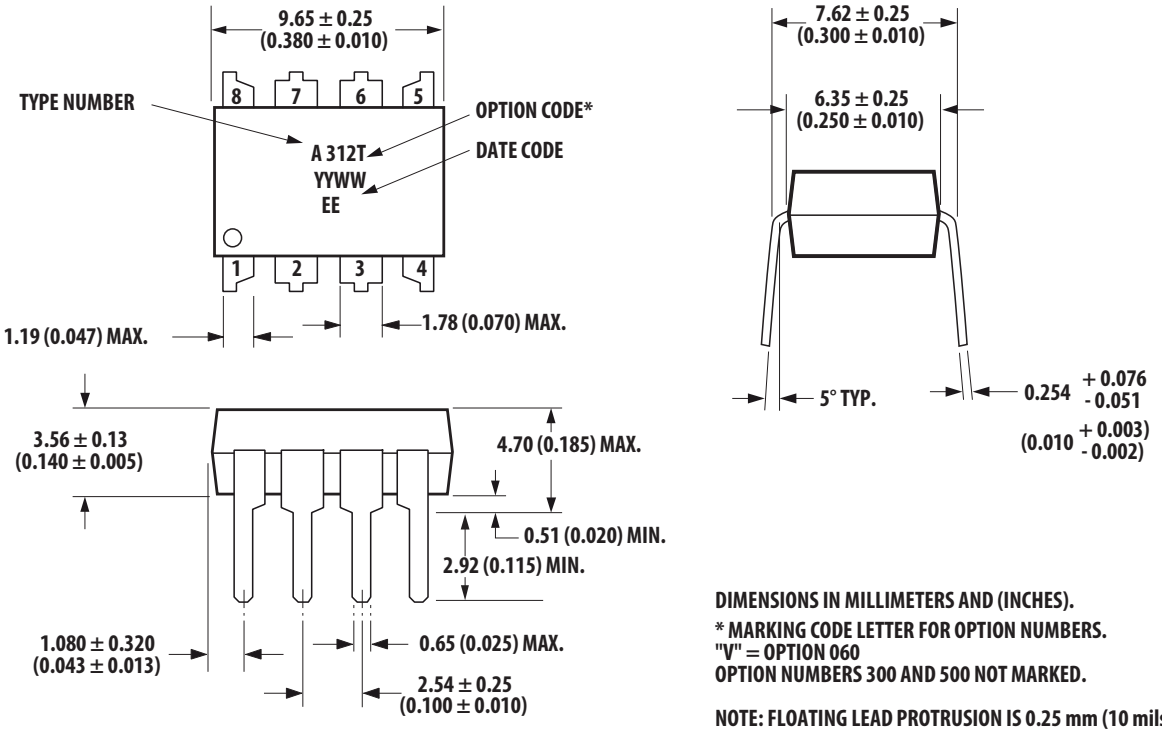
Example 2:

ACPL-312T-000E to order product of DIP-8 package in tube packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-312T-000E standard DIP8 package

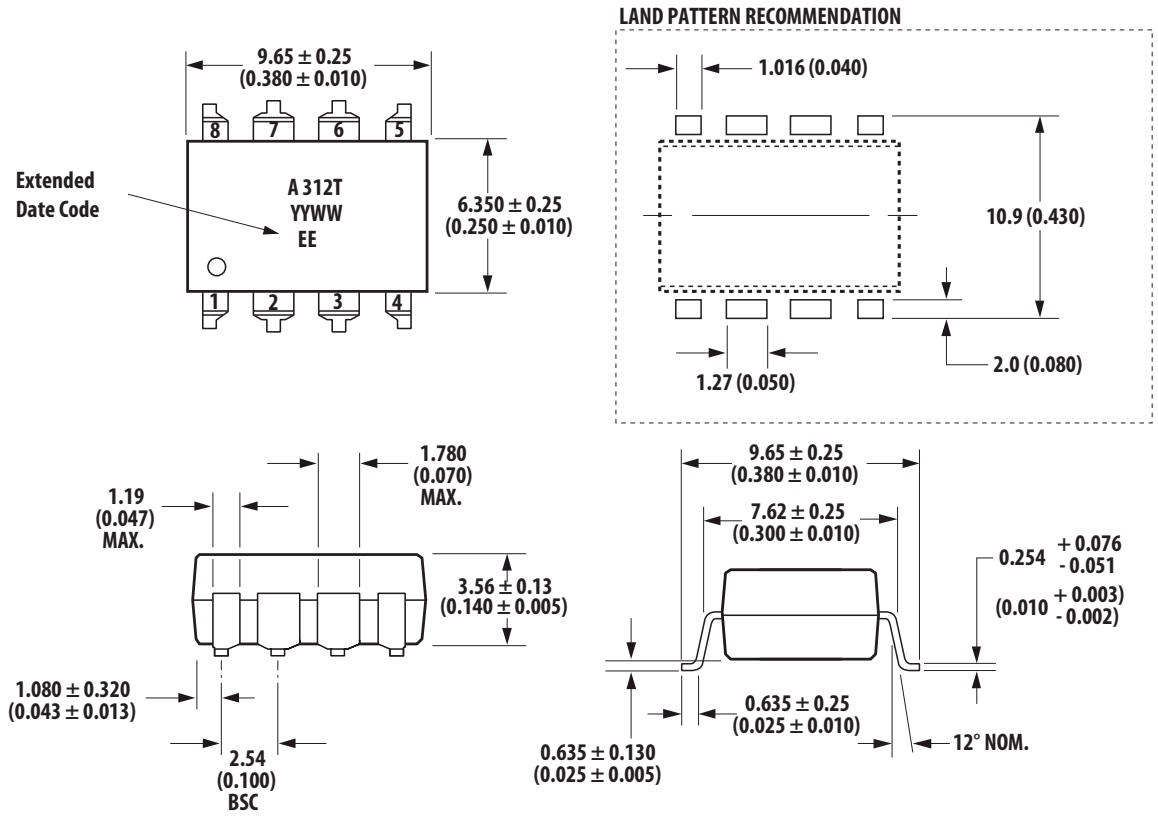


DIMENSIONS IN MILLIMETERS AND (INCHES).

*** MARKING CODE LETTER FOR OPTION NUMBERS.**
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

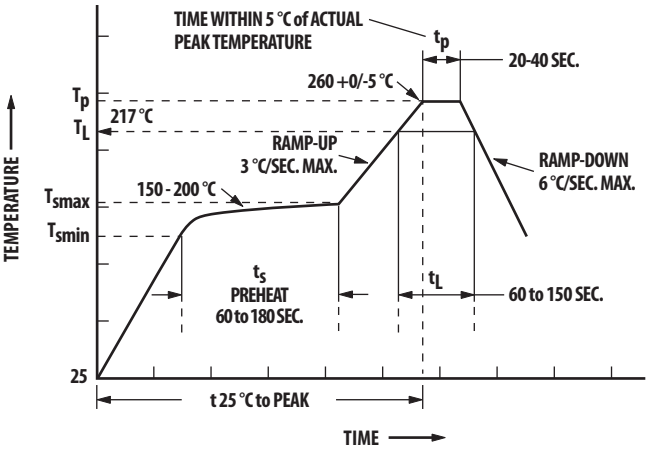
Gull Wing Surface Mount Option 300E and 500E



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Recommended Pb-Free IR Profile



Notes:
The time from 25 °C to peak temperature = 8 minutes max.
T_{smax} = 200 °C, T_{smin} = 150 °C
Non-halide flux should be used

Regulatory Information

The ACPL-312T-000E is approved by the following organizations:

UL

Recognized under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS}

CSA

CSA Component Acceptance Notice #5, File CA88324.

IEC/EN/DIN EN 60747-5-2

IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884Teil 2):2003-01

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0110)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics

Description	Symbol	ACPL-312T	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤150 V rms		I-IV	
for rated mains voltage ≤300 V rms		I-IV	
for rated mains voltage ≤3450V rms		I-III	
for rated mains voltage ≤3600V rms			
for rated mains voltage ≤1000V rms			
Climatic Classification		55/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{PEAK}
Input to Output Test Voltage, Method b† V_{IORM} x 1.875 = V_{PR}, 100% Production Test t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{PEAK}
Input to Output Test Voltage, Method a† V_{IORM} x 1.5 = V_{PR}, 100% Type and Sample Test t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{PEAK}
Highest Allowable Overvoltage† (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Thermal Derating curve, Figure 11.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{10} = 500 V	R_{IO}	$\geq 10^9$	Ω

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	125	°C	
Average Input Current	$I_{F(AVG)}$		20	mA	1
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Supply Voltage	$(V_{CC} - V_{EE})$	0	35	Volts	
Input Current (Rise/Fall Time)	$t_{r(IN)} / t_{f(IN)}$		500	ns	
Output Voltage	$V_{O(PEAK)}$	0	V_{cc}	Volts	
Output Power Dissipation	P_O		370	mW	3
Total Power Dissipation	P_T		400	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	125	°C
Power Supply Voltage	$(V_{CC} - V_{EE})$	15	30	Volts
Input Current	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V

DC Electrical Specifications

Over recommended operating conditions

(T_A = -40 to 125°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.5	1.5		A	V_O = (V_{CC} - 4 V)	2,3,17	5
		2.0			A	V_O = (V_{CC} - 15 V)		2
Low Level Output Current	I_{OL}	0.5	2.0		A	V_O = (V_{EE} + 2.5 V)	5,6 ,18	5
		2.0			A	V_O = (V_{EE} + 15 V)		2
High Level Output Voltage	V_{OH}	(V_{CC} - 4)	(V_{CC} - 3)		V	I_O = -100 mA	1,3, 19	6,7
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA	4,6,20	
High Level Supply Current	I_{CCH}		2.5	5.0	mA	Output Open, I_F = 7 to 16mA	7,8	
Low Level Supply Current	I_{CCL}		2.5	5.0	mA	Output Open, V_F = -3.0 to +0.8 V		
Threshold Input Current Low to High	I_{FLH}		0.8	5.0	mA	I_O = 0 mA, V_O > 5 V	9, 15, 21	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V		9	
Input Forward Voltage	V_F	1.2	1.5	1.95	V	I_F = 10 mA	16	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	B_{VR}	5.0			V	I_R = 10 µA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	11.0	12.3	13.5	V	V_O > 5 V, I_F = 10 mA	22, 34	
	V_{UVLO-}	9.5	10.7	12.0	V			
UVLO Hysteresis	U_{VLOHYS}		1.6		V			

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

AC Electrical Specifications

Over recommended operating conditions

(T_A = -40 to 125°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%	10, 11, 12,13, 14, 23	16
Propagation Delay Time to Low Output Level	t_{PHL}	0.10	0.30	0.50	µs			
Pulse Width Distortion	PWD			0.3	µs			17
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-0.35		0.35	µs		35, 36	12
Rise Time	T_r		0.1		µs		23	
Fall Time	T_f		0.1		µs			
UVLO Turn On Delay	$t_{UVLO\ ON}$		0.8		µs	V_O > 5 V, I_F = 10 mA	22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6		µs	V_O < 5 V, I_F = 10 mA		15
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	25	35		kV/µs	T_A = 25°C, I_F = 10 to 16 mA, V_{CM} = 1500 V, V_{CC} = 30 V	24	13, 14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	25	35		kV/µs	T_A = 25°C, V_{CM} = 1500 V, V_F = 0 V, VCC = 30 V		13, 15

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Package Characteristics

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}	3750			V_{RMS}	RH < 50%, t = 1 min. T_A = 25°C		8, 11
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V_{DC}		11
Capacitance (Input-Output)	C_{I-O}		0.8		pF	f = 1 MHz		18
LED-to-Case Thermal Resistance	θ_{LC}		467		°C/W	Thermocouple located at center underside of package	28	
LED-to-Detector Thermal Resistance	θ_{LD}		442		°C/W			
Detector-to-Case Thermal Resistance	θ_{DC}		126		°C/W			

*All typicals at T_A = 25°C.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refers to your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.0727 mA/°C. '
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with IO peak minimum = 2.0 A. See Applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 70°C free-air temperature at a rate of 5.0 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 5.0 mW/°C. The maximum LED junction temperature should not exceed 150°C.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%. 8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 Vrms for 1 second (leakage detection current limit, II-O ≤ 5 µA).
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 Vrms for 1 second (leakage detection current limit, II-O ≤ 5 µA).
9. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 Vrms for 1 second (leakage detection current limit, II-O ≤ 5 µA).
10. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
11. The difference between t_{PHL} and t_{PLH} between any two ACPL-312T parts under the same test condition.
12. Pins 1 and 4 need to be connected to LED common.
13. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15.0 V).
14. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V).
15. This load condition approximates the gate load of a 1200 V/75A IGBT.
16. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.

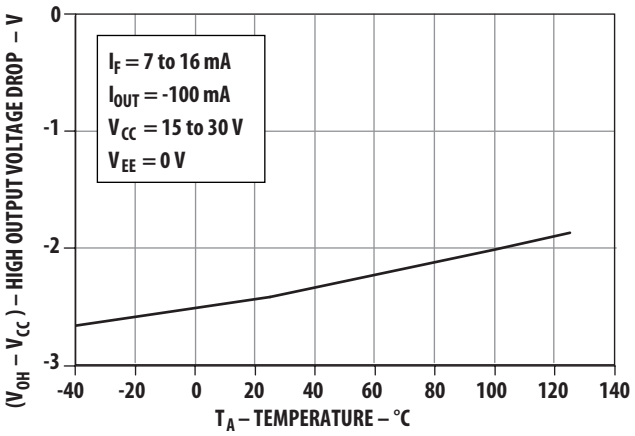


Figure 1. V_{OH} vs. temperature.

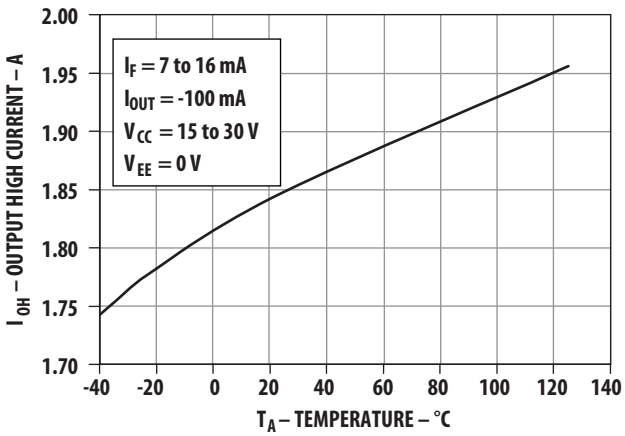


Figure 2. I_{OH} vs. temperature.

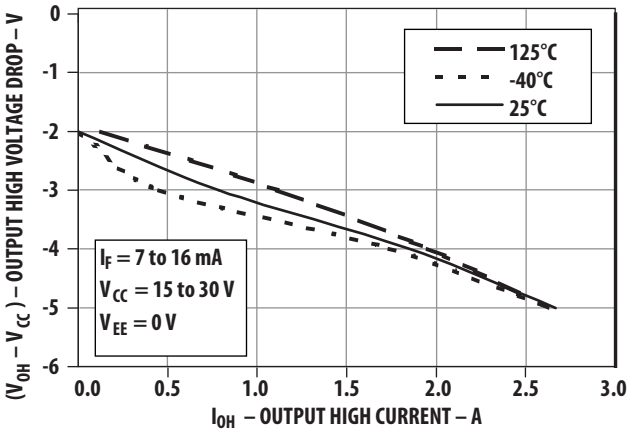


Figure 3. V_{OH} vs. I_{OH}.

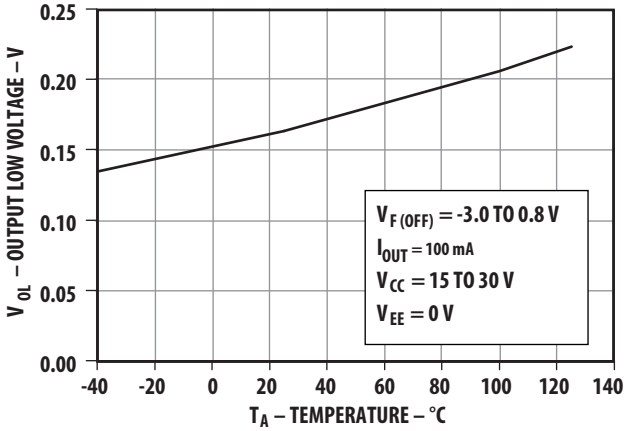


Figure 4. V_{OL} vs. temperature.

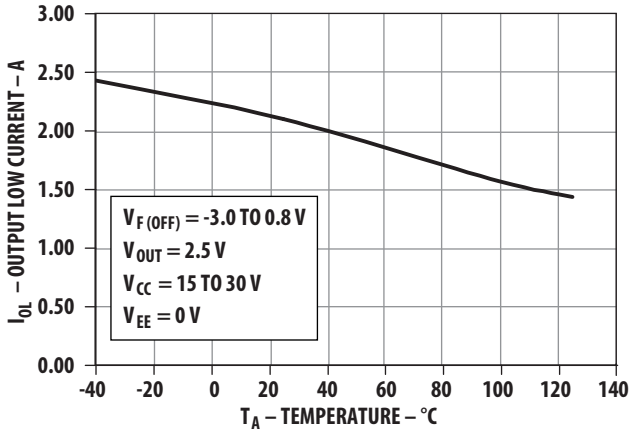


Figure 5. I_{OL} vs. temperature.

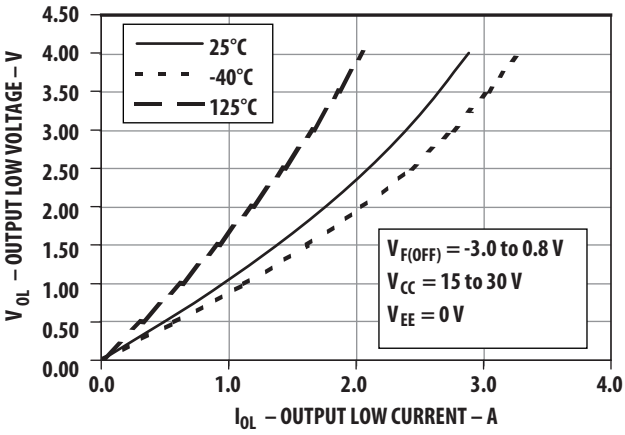


Figure 6. V_{OL} vs. I_{OL}.

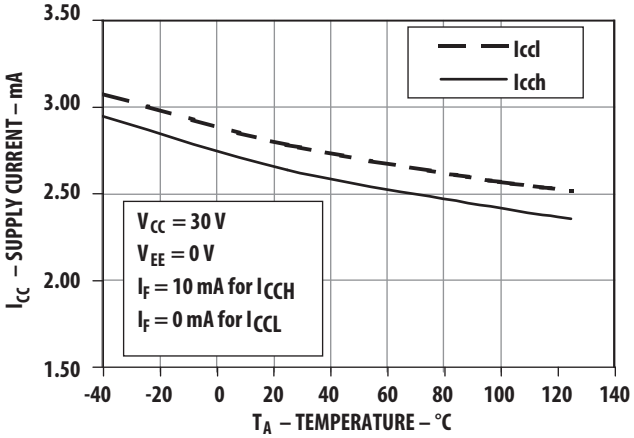


Figure 7. I_{CC} vs. temperature.

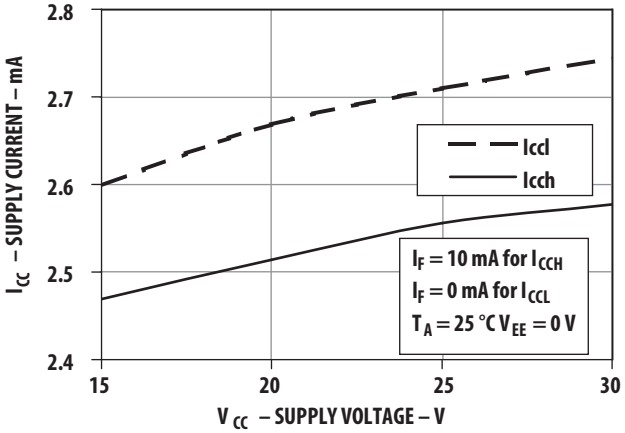


Figure 8. I_{CC} vs. V_{CC}.

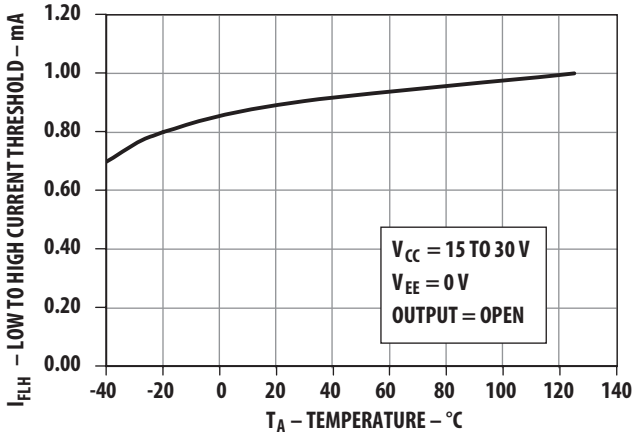


Figure 9. I_{FLH} vs. temperature.

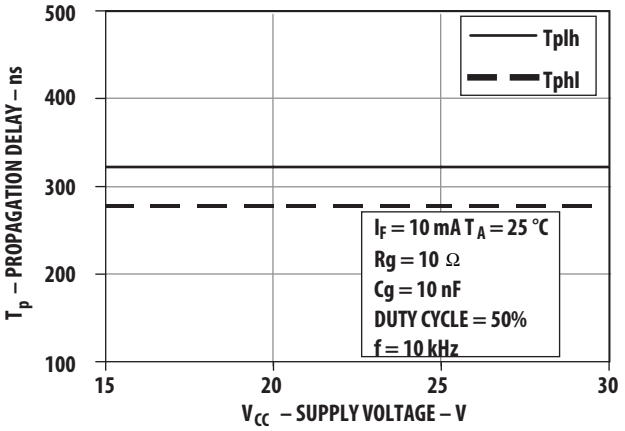


Figure 10. Propagation delay vs. V_{CC}.

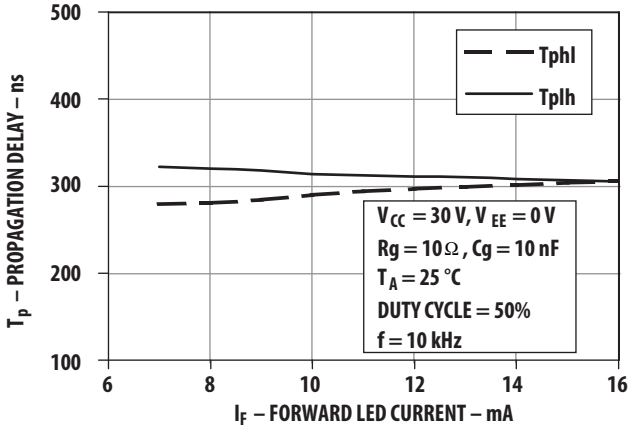


Figure 11. Propagation delay vs. I_F.

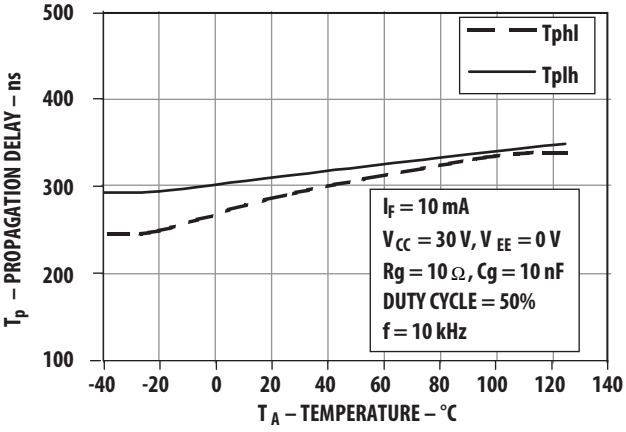


Figure 12. Propagation delay vs. temperature.

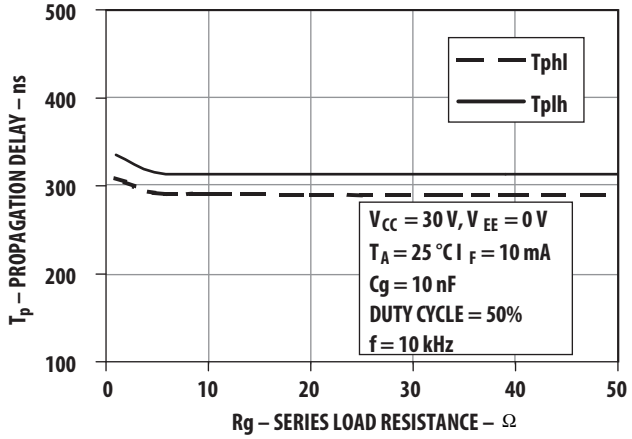


Figure 13. Propagation delay vs. Rg.

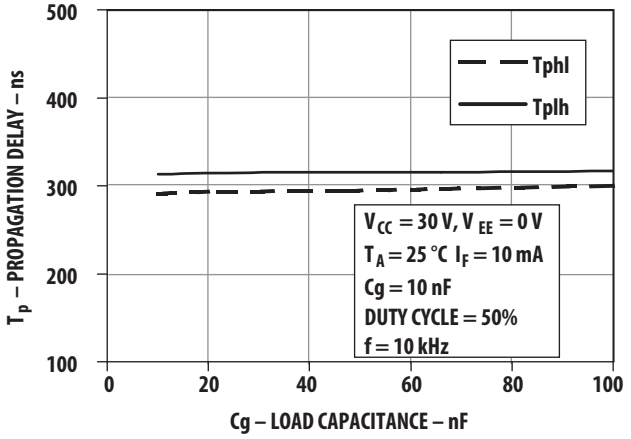


Figure 14. Propagation delay vs. Cg.

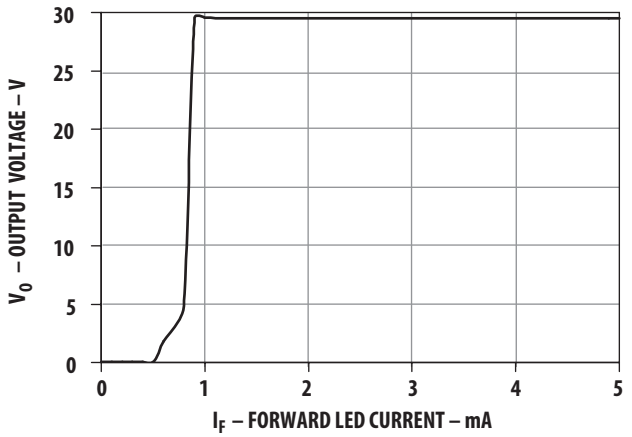


Figure 15. Transfer characteristics.

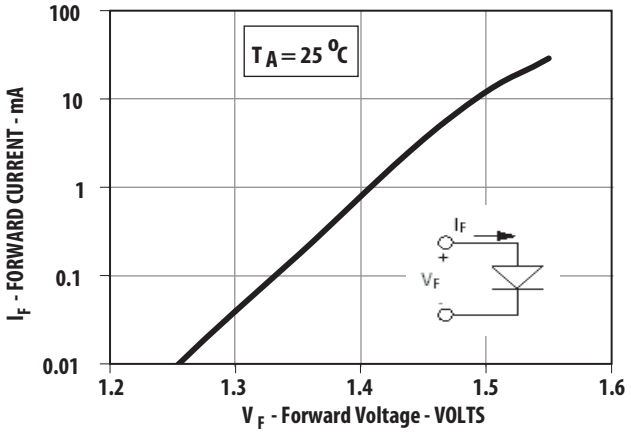


Figure 16. Input current vs. forward voltage.

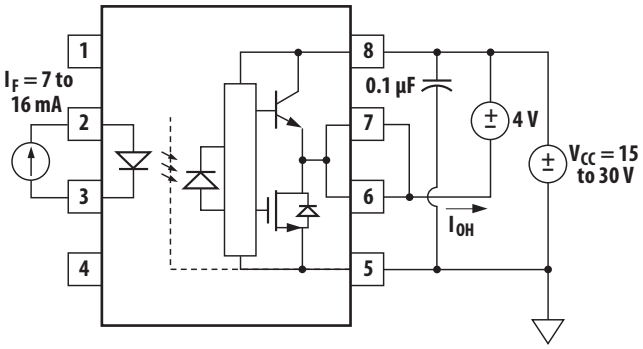


Figure 17. I_{OH} test circuit.

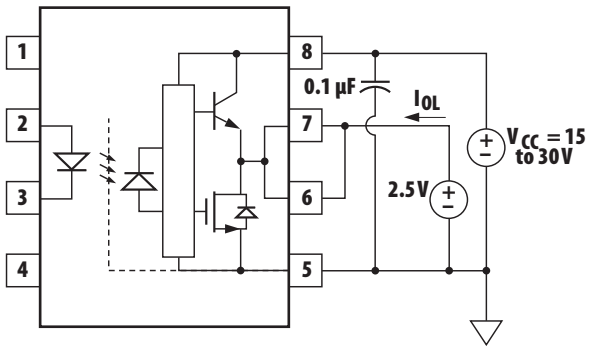


Figure 18. I_{OL} Test circuit.

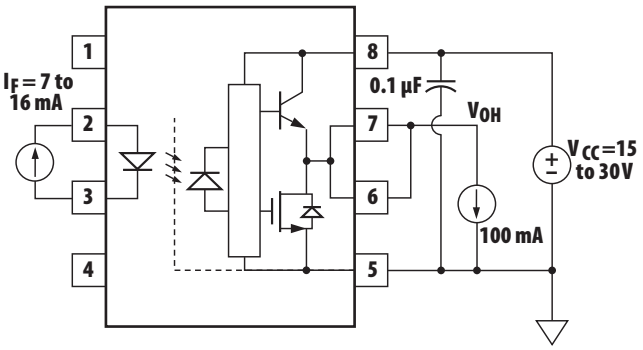


Figure 19. V_{OH} Test circuit.

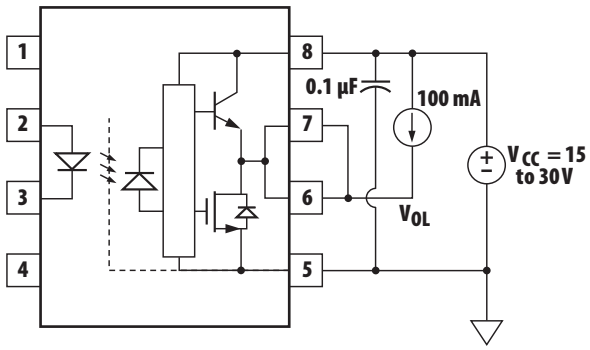


Figure 20. V_{OL} Test circuit.

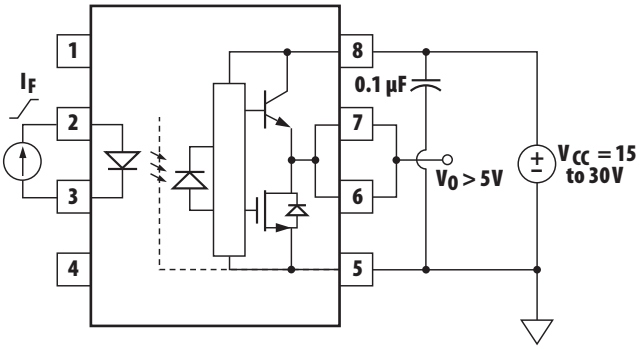


Figure 21. I_{FLH} Test circuit.

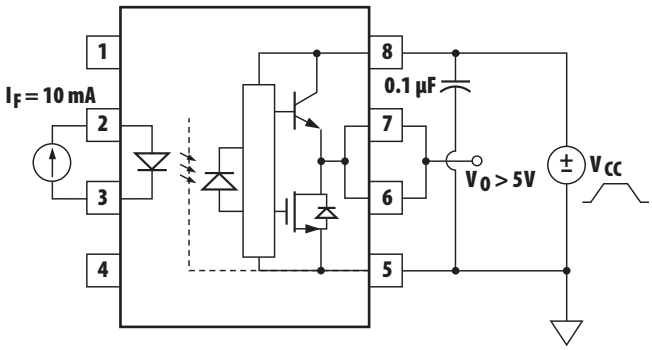


Figure 22. UVLO test circuit.

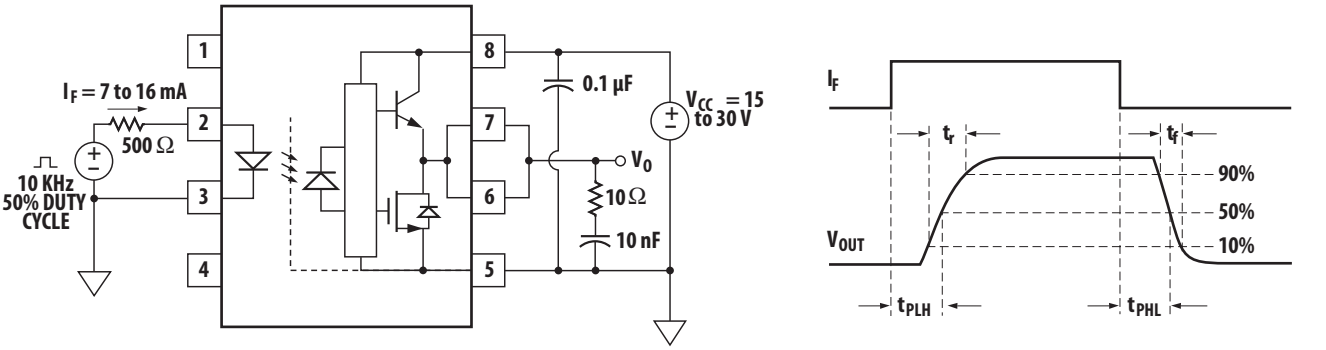


Figure 23. t_{PLH}, t_{PHL}, tr, and tf test circuit and waveforms.

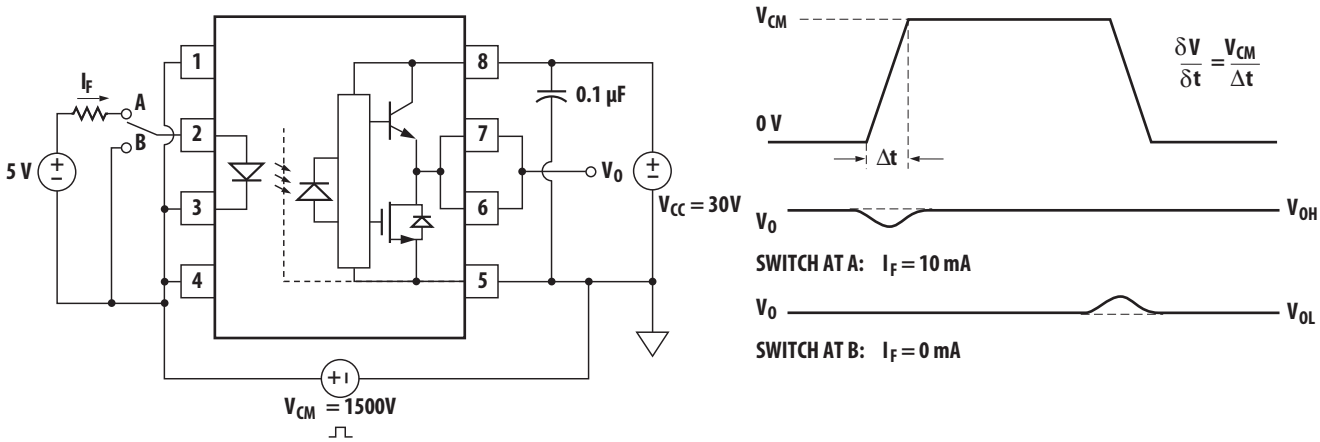


Figure 24. CMR test circuit and waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive ACPL-312T

To keep the IGBT firmly off, the ACPL-312T has a very low maximum V_{OL} specification of 0.5 V. The ACPL-312T realizesthis very low V_{OL} by using a DMOS transistor with 1 Ω (typical) on resistance in its pull down circuit. When the ACPL-312T is in the low state, the IGBT gate is shorted to the emitter by Rg + 1 Ω. Minimizing Rg and the lead inductance from the ACPL-312T to the IGBT gate and emitter (possibly by mounting the ACPL-312T on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the ACPL-312T input as this can result in unwanted coupling of transient signals into the ACPL-312T and degrade performance. (If the IGBT drain must be routed near the ACPL-312T input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the ACPL-312T).

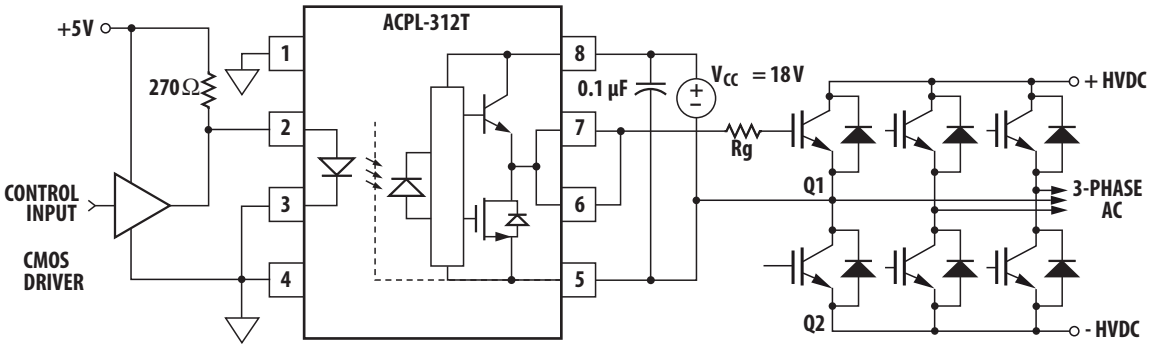


Figure 25. Recommended LED drive and application circuit.

Selecting the Gate Resistor (Rg) to Minimize IGBT Switching Losses.

Step 1: Calculate Rg Minimum from the I_{OL} Peak Specification. The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3120.

$$R_g \geq \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}} = \frac{(V_{CC} - V_{EE} - 2V)}{I_{OLPEAK}}$$

$$= \frac{(15 + 5 - 2)}{2.5A} \quad R_g = 7.2\Omega \cong 8\Omega$$

The V_{OL} value of 2 V in the previous equation is a conservative value of VOL at the peak current of 2.5A (see Figure 6). At lower Rg values the voltage supplied by the ACPL-312T is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used VEE in the previous equation is equal to zero volts.

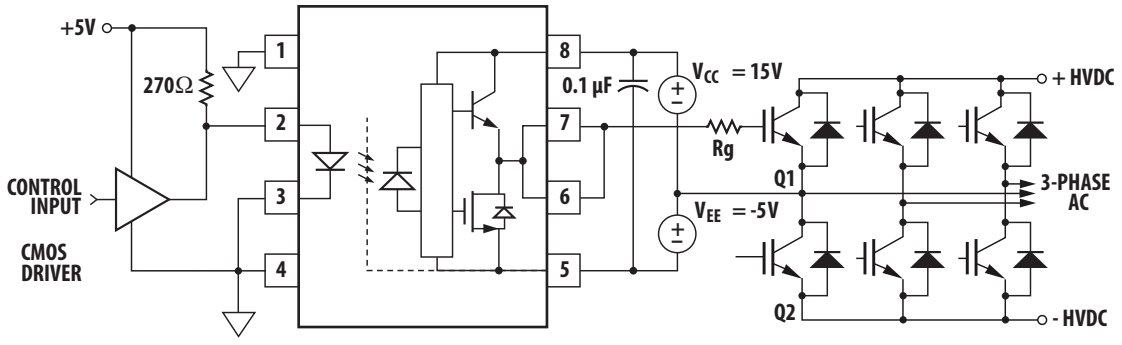


Figure 26. ACPL-312T typical application circuit with negative IGBT gate drive.

Step 2: Check the ACPL-312T Power Dissipation and Increase Rg if Necessary.

The ACPL-312T total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O):

$P_T = P_E + P_O$

$P_E = I_F . V_F .$Duty Cycle

$P_O = P_{O(BIAS)} + P_{O\ (SWITCHING)}$

$= I_{CC}.(V_{CC} - V_{EE}) + E_{SW}(R_G, Q_G).f$

For the circuit in Figure 26 with I_F (worst case) = 16 mA, Rg = 8 Ω, Max Duty Cycle = 80%, Qg = 500 nC, f = 20 kHz and TA max = 85C:

$P_E = 16$ mA.1.8 V.0.8 = 23 mW

$P_O = 4.25$ mA . 20 V + 5.2 µJ . 20 kHz

= 85 mW + 104 mW

= 189 mW

> 178 mW ($P_{O(MAX)}$) @ 85C

= 250 mW-15C*4.8 mW/C)

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at -40°C) to I_{CC} max at 125C (see Figure 7). Since P_O for this case is greater than $P_{O(MAX)}$, R_g must be increased to reduce the ACPL-312T power dissipation.

$P_{O(SWITCHING\ MAX)} = P_{O(MAX)} - P_{O(BIAS)}$

= 178 mW - 85 mW

= 93 mW

$$ESW(MAX) = \frac{PO(SWITCHINGMAX)}{f}$$

$$= \frac{93\,mW}{20\,kHz}$$

$= 4.65\,\mu W$

For Qg = 500 nC, from Figure 27, a value of ESW = 4.65 µW gives a Rg = 10.3 Ω.

P_E Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle

P_0 Parameter	Description
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Energy Dissipated in the ACPL-312T for each IGBT Switching Cycle (See Figure 27)
E_{SW}(Rg,Qg)	
f	Switching Frequency

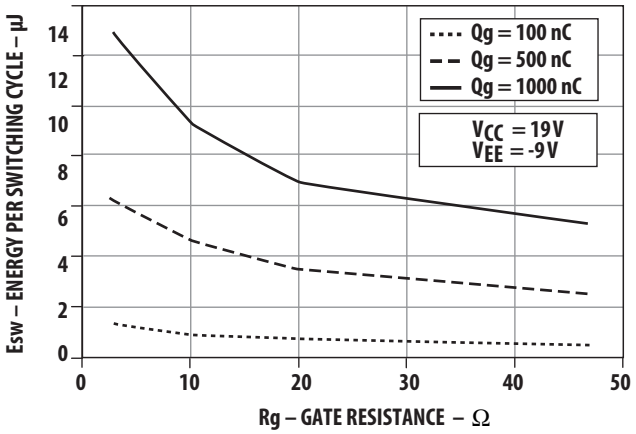


Figure 27. Energy dissipated in the ACPL-312T for each IGBT switching cycle.

Thermal Model

The steady state thermal model for the ACPL-312T is shown in Figure 28. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA} which raises the case temperature TC accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = 83°C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single ACPL-312T soldered into the center of the board and still air. The absolute maximum power dissipation de-rating specifications assume a θ_{CA} value of 83°C/W. From the thermal mode in Figure 28 the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \cdot (\theta_{LD} \,||\, \theta_{DC}) + \theta_{CA})$$
$$+ P_D \cdot \left(\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + T_A$$

$$T_{JD} = P_E \cdot \left(\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right)$$
$$+ P_D \cdot (\theta_{DC} \,||\, \theta_{LD}) + \theta_{LC}) + T_A$$

Inserting the values for θ_{LC} and θ_{DC} shown in Figure 28 gives:

$T_{JE} = P_E.(256°C/W + \theta_{CA}) + P_D.(57°C/W + \theta_{CA}) + T_A$

$T_{JD} = P_E.(57°C/W + \theta_{CA}) + P_D.(111°C/W + \theta_{CA}) + T_A$

For example, given P_E = 30 mW, P_O = 230 mW, T_A = 100°C and θ_{CA} = 83°C/W:

$T_{JE} = P_E.339°C/W + P_D.140°C/W + T_A$

$= 30 mW@339°C/W + 230 mW .140°C/W + 100°C$

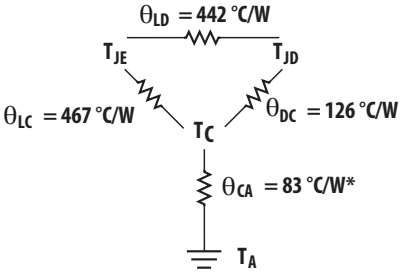
$= 142°C$

$T_{JD} = P_E.140°C/W + P_D.194°C/W + T_A$

$= 30 mW.140°C/W + 230 mW.194°C/W + 100°C$

$= 149°C$

T_{JE} and T_{JD} should be limited to 150°C based on the board layout and part placement (θ_{CA}) specific to the application.



T_{JE}	=	LED junction temperature
T_{JD}	=	detector IC junction temeperature
T_C	=	case temperature measured at the center of the package bottom
θ_{LC}	=	LED-to-case thermal resistance
θ_{LD}	=	LED-to-detector thermal resistance
θ_{DC}	=	detector-to-case thermal resistance
θ_{CA}	=	case-to-ambient thermal resistance
*θ_{CA}		will depend on the board design and the placement of the part.

Figure 28. Thermal model.

LED Drive Circuit Considerations for Ultra High CMR Performance.

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 29. The ACPL-312T improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 30. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 25 kV/µs CMR while minimizing component complexity. Techniques to keep the LED in the proper state are discussed in the next two sections.

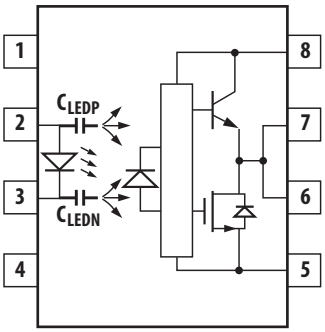


Figure 29. Optocoupler input to output capacitance model for unshielded optocouplers.

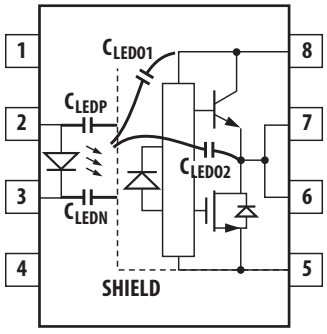


Figure 30. Optocoupler input to output capacitance model for shielded optocouplers.

CMR with the LED On (CMRH).

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum IFLH of 5 mA to achieve 25 kV/µs CMR. CMR with the LED Off (CMRL). A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{cm}/dt$ transient in Figure 31, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur. The open collector drive circuit, shown in Figure 32, cannot keep the LED off during a $+dV_{cm}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMRL performance. Figure 33 is an alternative drive circuit which, like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

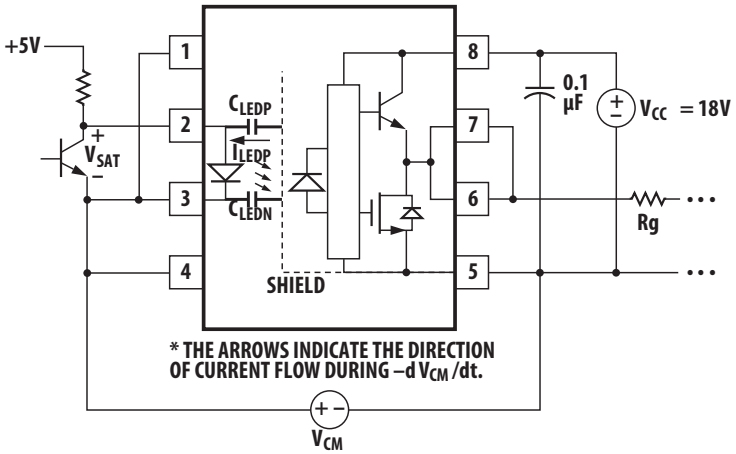


Figure 31. Equivalent circuit for figure 25 during common mode transient.

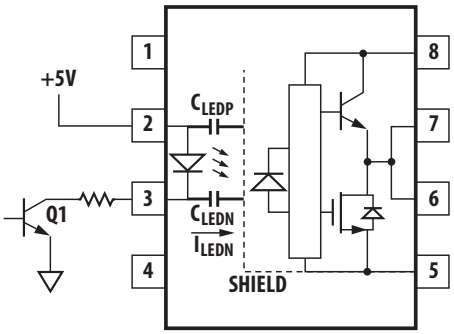


Figure 32. Not recommended open collector drive circuit.

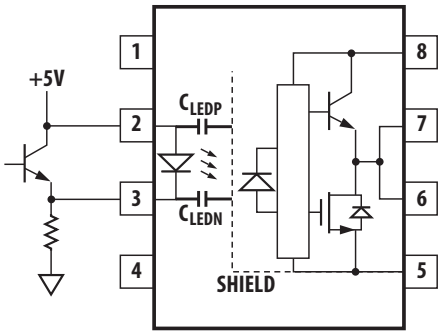


Figure 33. Recommended LED drive circuit for ultra-high CMR.

The ACPL-312T contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the ACPL-312T supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the ACPL-312T output is in the high state and the supply voltage drops below the ACPL-312T V_{UVLO-} threshold ($9.5 < V_{UVLO-} < 12.0$) the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 µs. When the ACPL-312T output is in the low state and the supply voltage rises above the ACPL-312T V_{UVLO+} threshold ($11.0 < V_{UVLO+} < 13.5$) the optocoupler output will go into the high state (assumes LED is "ON") with a typical delay, UVLO Turn On Delay of 0.8 µs.

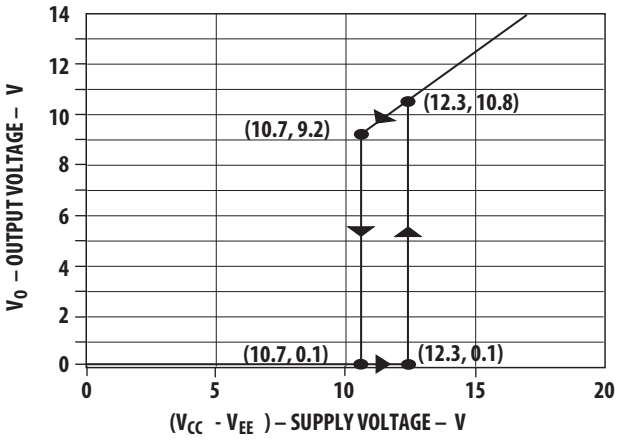
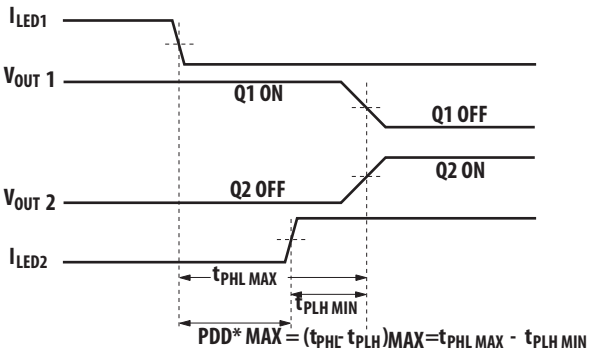


Figure 34. Under voltage lock out.



***PDD = PROPAGATION DELAY DIFFERENCE**
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

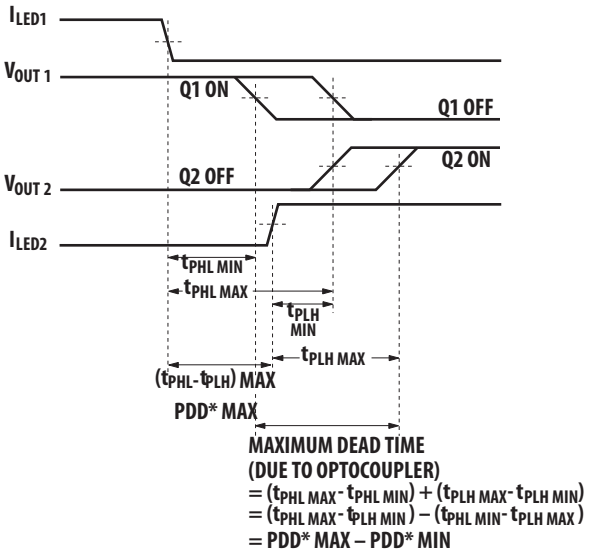
Figure 35. Minimum LED skew for zero dead time.

Dead Time and Propagation Delay Specifications

The ACPL-312T includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 25) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 35. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of -40°C to 125°C. Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 36. The maximum dead time for the ACPL-312T is 700 ns (= 350 ns - (-350 ns)) over an operating temperature range of -40°C to 125°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.



***PDD = PROPAGATION DELAY DIFFERENCE**
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 36. Waveforms for dead time.

Output Power Derating Curve

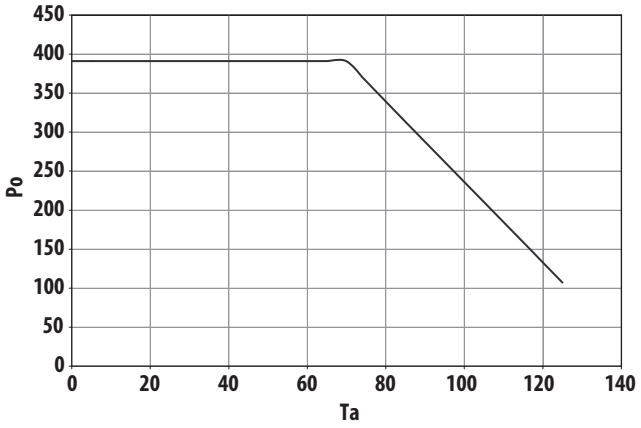


Figure 37. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-2.

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