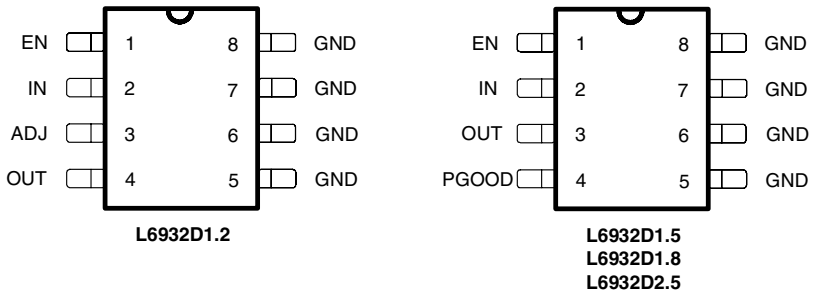
PIN CONNECTIONS



PIN FUNCTION

N°	L6232D 1.2	L6232D 1.5/1.8/ 2.5	Description
1	EN		Enables the device if connected to Vin and disables the device if forced to gnd.
2	IN		Supply voltage. This pin is connected to the drain of the internal N-mos. Connect this pin to a capacitor larger than 10µF.
3	ADJ	–	Connecting this pin to a voltage divider it is possible to programme the output voltage between 1.2V and 5V.
	–	OUT	Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10µF.
4	OUT	–	Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10µF.
	–	PGOOD	Power good output. The pin is open drain and detects the output voltage. It is forced low if the output voltage is lower than 90% of the programmed voltage.
5, 6, 7, 8	GND		Ground pin.

ABSOLUTE MAXIMUM RATINGS

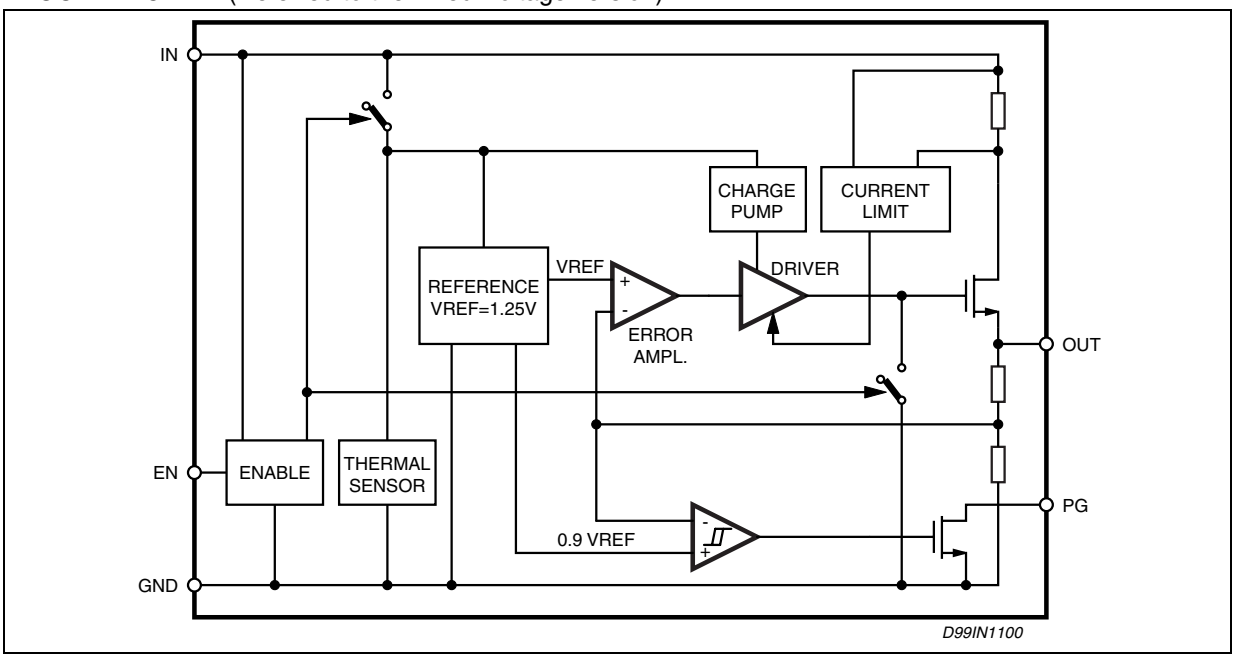
Symbol	Parameter	Value	Unit
V_{in}	VIN and Pgood	14.5	V
	EN, OUT and ADJ	-0.3 to (V_{in} +0.3)	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ J\text{-}amb}$	Thermal Resistance Junction to Ambient	62 (*)	°C/W
T_{max}	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C

(*) Measured on Demoboard with about 4 cm^2 of dissipating area 2 Oz.

BLOCK DIAGRAM (Referred to the Fixed Voltage version)



ELECTRICAL CHARACTERISTCS (T_j = 25°C, V_{IN} = 5V unless otherwise specified)

(*) Specification referred to T_j from -25°C to 125°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{in}	Operating Supply Voltage		2		14	V
V_o	Output voltage L6932D1.2	I_o = 0.1A; V_{in} = 3.3V	1.188	1.2	1.212	V
	Output voltage L6932D1.5	I_o = 0.1A; V_{in} = 3.3V	1.485	1.5	1.515	V
	Output voltage L6932D1.8	I_o = 0.1A; V_{in} = 3.3V	1.782	1.8	1.818	V
	Output voltage L6932D2.5	I_o = 0.1A; V_{in} = 3.3V	2.475	2.5	2.525	V
	L6932D1.2 Line Regulation	V_{in} = 2.5V ±10%; I_o = 10mA			5	mV
		V_{in} = 3.3V ±10%; I_o = 10mA			5	mV
		V_{in} = 5V ±10%; I_o = 10mA			5	mV
	L6932D1.5 Line Regulation	V_{in} = 2.5V ±10%; I_o = 10mA			5	mV
		V_{in} = 3.3V ±10%; I_o = 10mA			5	mV
		V_{in} = 5V ±10%; I_o = 10mA			5	mV
	L6932D1.8 Line Regulation	V_{in} = 2.5V ±10%; I_o = 10mA			5	mV
		V_{in} = 3.3V ±10%; I_o = 10mA			5	mV
		V_{in} = 5V ±10%; I_o = 10mA			5	mV
	L6932D2.5 Line Regulation	V_{in} = 3.3V ±10%; I_o = 10mA			5	mV
		V_{in} = 5V ±10%; I_o = 10mA			5	mV
	L6932D1.2 Load Regulation	V_{in} = 3.3V; 0.1A < I_o < 2A			15	mV
	L6932D1.5 Load Regulation	V_{in} = 3.3V; 0.1A < I_o < 2A			15	mV
	L6932D1.8 Load Regulation	V_{in} = 3.3V; 0.1A < I_o < 2A			15	mV
	L6932D2.5 Load Regulation	V_{in} = 3.3V; 0.1A < I_o < 2A			15	mV
R_{dson}	Drain Source ON resistance				200	mΩ

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{occ}	Current limiting			2.3	2.5	2.7	A
I_q	Quiescent current				0.2	0.4	mA
I_{sh}	Shutdown current	$2V < V_{in} < 14V$	*			25	µA
	Ripple Rejection	f = 120Hz, I_o = 1A V_{in} = 5V, ΔV_{in} = 2Vpp		60	75		dB
V_{en}	EN Input Threshold			0.5	0.65	0.8	V
	Pgood threshold	V_o rise			90		%Vo
	Pgood Hysteresis				10		%Vo
	Pgood saturation	I_{pgood} =1mA			0.2	0.4	V

Figure 1. Output Voltage vs. Junction Temperature (L6932D1.2)

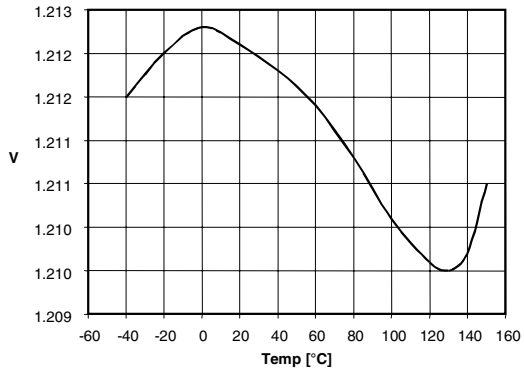


Figure 2. Output Voltage vs. Junction Temperature (L6932D1.8)

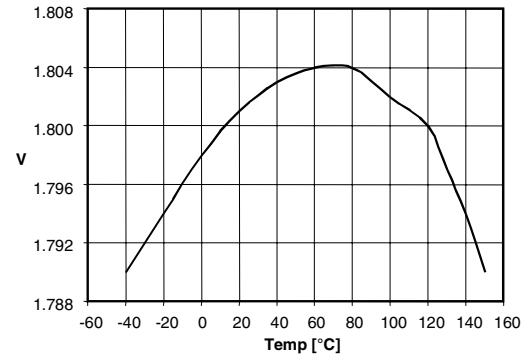


Figure 3. Output Voltage vs. Junction Temperature (L6932D2.5)

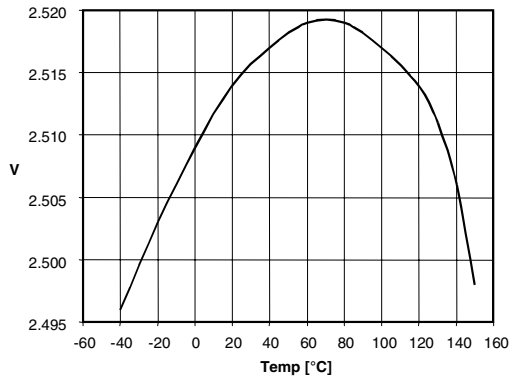


Figure 4. Quiescent Current vs. Junction Temperature

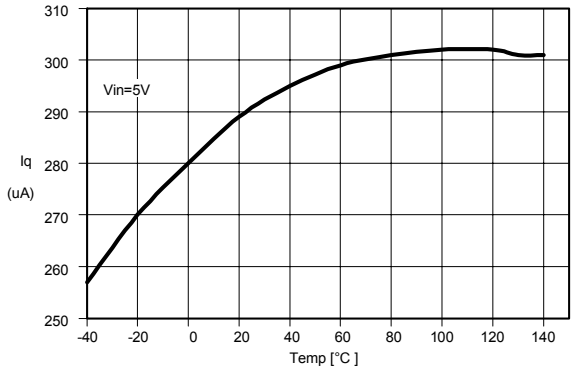
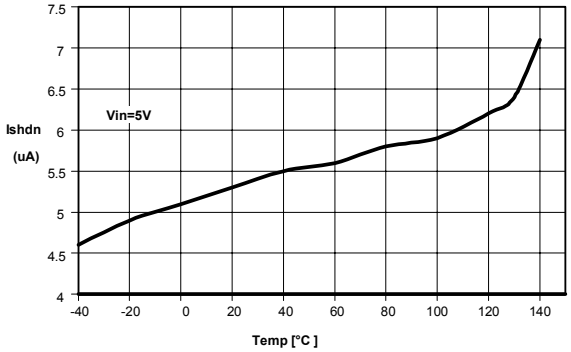


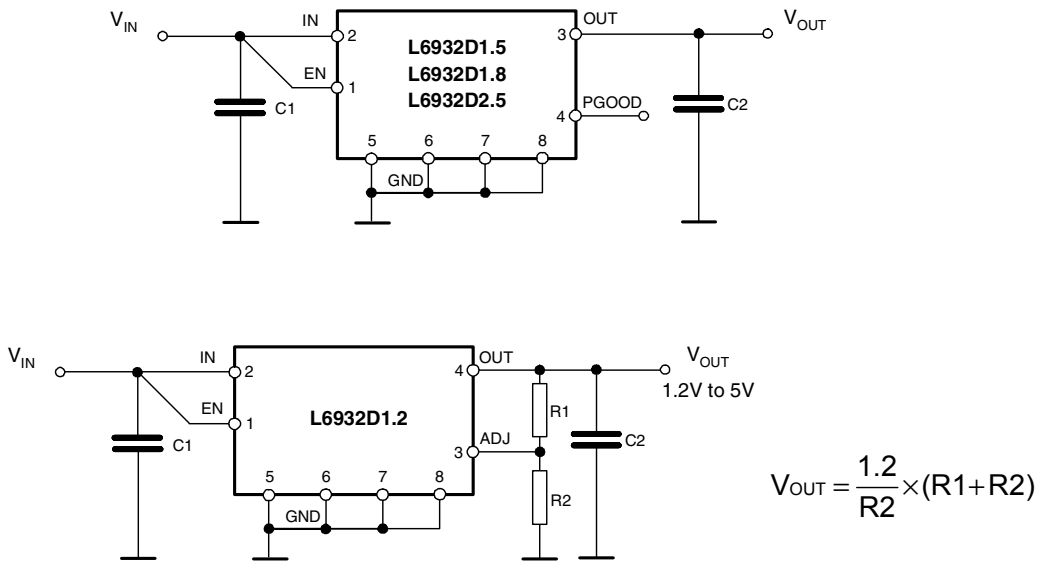
Figure 5. Shutdown Current vs. Junction TemperatureAPPLICATION INFORMATIONS



APPLICATION CIRCUIT

In figure 6 the schematic circuit of the demoboards are shown.

Figure 6. Demoboards Schematic Circuit

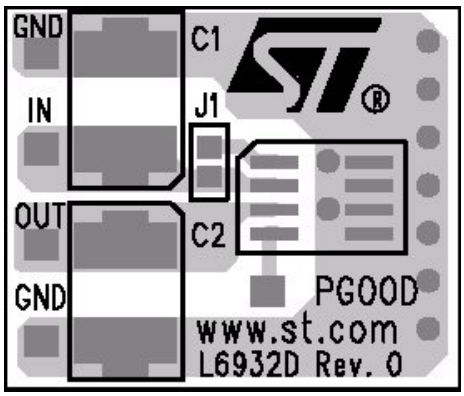


COMPONENT LIST

Fixed version

Reference	Part Number	Description	Manufacturer
C1	C34Y5U1E106Z	10uF, 25V	TOKIN
C2	C34Y5U1E106Z	10uF, 25V	TOKIN

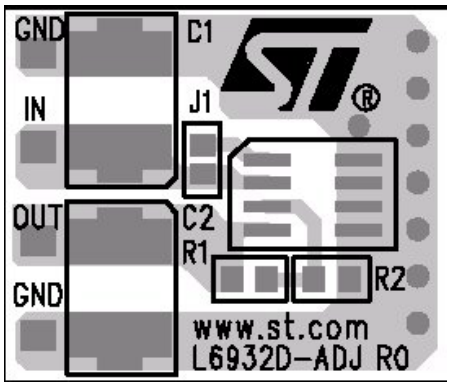
Figure 7. Demoboard Layout (Fixed Version)



Adjustable version

Reference	Part Number	Description	Manufacturer
C1	C34Y5U1E106Z	10uF, 25V	TOKIN
C2	C34Y5U1E106Z	10uF, 25V	TOKIN
R1		5.6K, 1%, 0.25W	Neohm
R2		3.3K, 1%, 0.25W	Neohm

Figure 8. Demoboard Layout (Adjustable Version)



COMPONENTS SELECTION

Input Capacitor

The input capacitor value depends on a lot of factors such as load transient requirements, input source (battery or DC/DC converter) and its distance from the input cap. Usually a 47µF is enough for any application but a much lower value can be sufficient in many cases.

Output Capacitor

The output capacitor choice depends basically on the load transient requirements.

Tantalum, Speciality Polimer, POSCAP and aluminum capacitors are good and offer very low ESR values.

Multilayer ceramic caps have the lowest ESR and can be required for particular applications. Nevertheless in several applications they are ok, the loop stability issue has to be considered (see loop stability section).

Below a list of some suggested capacitor manufacturers.

Manufacturer	Type	Cap Value (μF)	Rated Voltage (V)
PANASONIC	CERAMIC	1 to 47	4 to 16
TAYO YUDEN	CERAMIC	1 to 47	4 to 16
TDK	CERAMIC	1 to 47	4 to 16
TOKIN	CERAMIC	1 to 47	4 to 16
SANYO	POSCAP	1 to 47	4 to 16
PANASONIC	SP	1 to 47	4 to 16
KEMET	TANTALUM	1 to 47	4 to 16

Loop Stability

The stability of the loop is affected by the zero introduced by the output capacitor.

The time constant of the zero is given by:

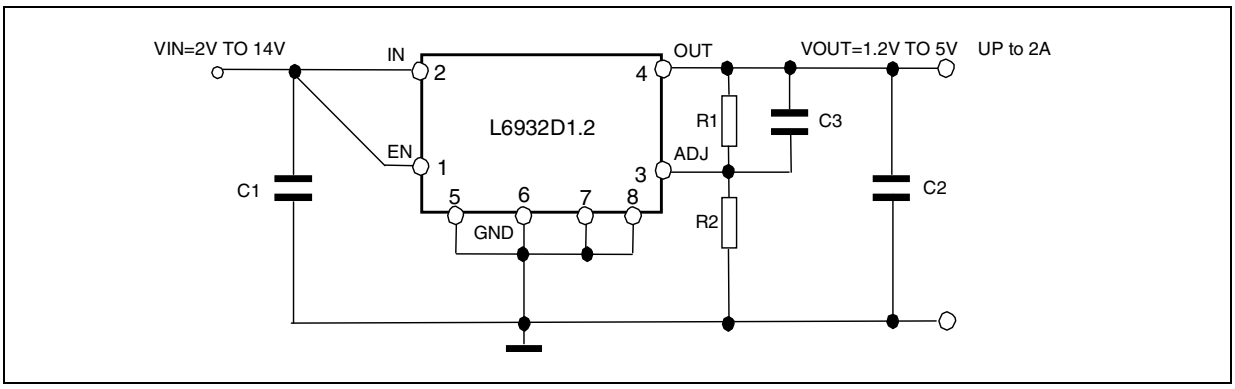
$$T = ESR \cdot C_{OUT} \qquad F_{ZERO} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

This zero helps to increase the phase margin of the loop until the time constant is higher than some hundreds of nsec, depending also on the output voltage and current.

So, using very low ESR ceramic capacitors could produce oscillations at the output, in particular when regulating high output voltages (adjustable version).

To solve this issue is sufficient to add a small capacitor (e.g. 1nF to 10nF) in parallel to the high side resistor of the external divider, as shown in figure 9.

Figure 9. Compensation Network



Thermal Considerations

Since the device is housed in a small SO(4+2+2) package the thermal issue can be the bottleneck of many applications. The power dissipated by the device is given by:

$$P_{DISS} = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

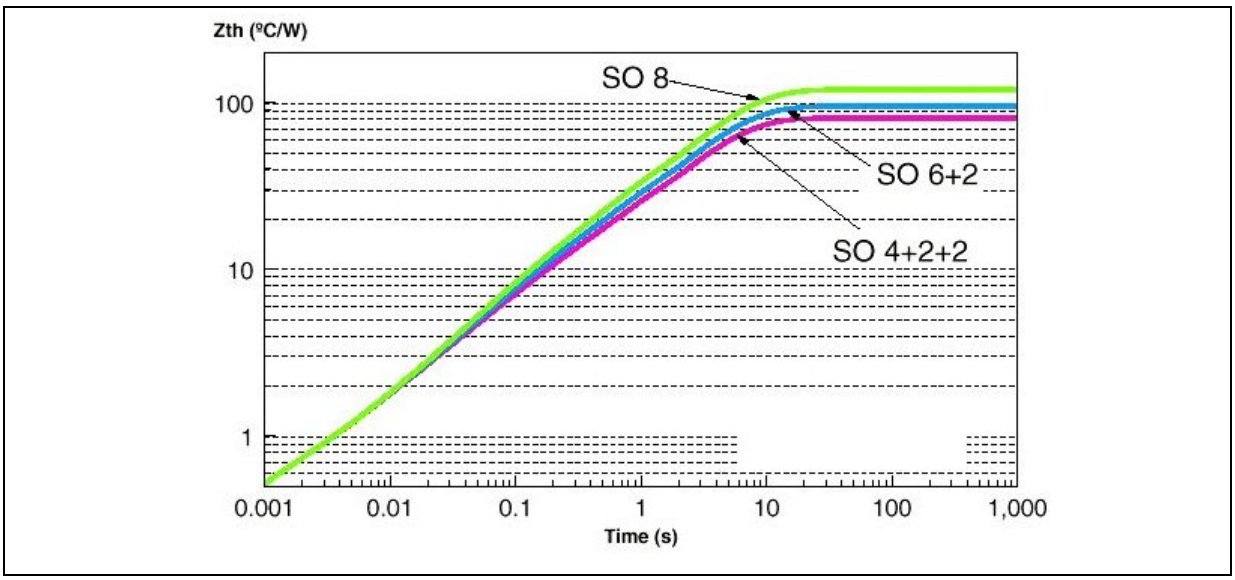
The thermal resistance junction to ambient of the demoboard is approximately 62°C/W. This mean that, considering an ambient temperature of 60°C and a maximum junction temperature of 150°C, the maximum power that the device can handle is 1.5W.

This means that the device is able to deliver a DC output current of 2A only with a very low dropout.

In many applications, high output current pulses are required. If their duration is shorter than the thermal constant time of the board, the thermal impedance (not the thermal resistance) has to be considered.

In figure 10 the thermal impedance versus the duration of the current pulse for the SO(4+2+2) mounted on board is shown.

Figure 10. Thermal Impedance



Considering a pulse duration of 1sec, the thermal impedance is close to 20°C/W, allowing much bigger power dissipated.

Example:

Vin = 3.3V

Vout = 1.8V

Iout = 2A

Pulse Duration = 1sec

The power dissipated by the device is:

$$P_{DISS} = (V_{IN} - V_{OUT}) \cdot I_{OUT} = 1.5 \cdot 2\ 3W$$

Considering a thermal impedance of 20°C/W, the maximum junction temperature will be:

$$T_J = T_A + Z_{THJA} \cdot P_{DISS} = 60 + 60 = 120°C$$

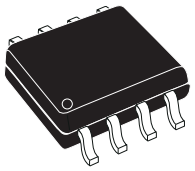
Obviously, with pulse durations longer than approximately 10sec the thermal impedance is very close to the thermal resistance (60°C/W to 70°C/W).

Figure 11. SO-8 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.
Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

OUTLINE AND MECHANICAL DATA



SO-8

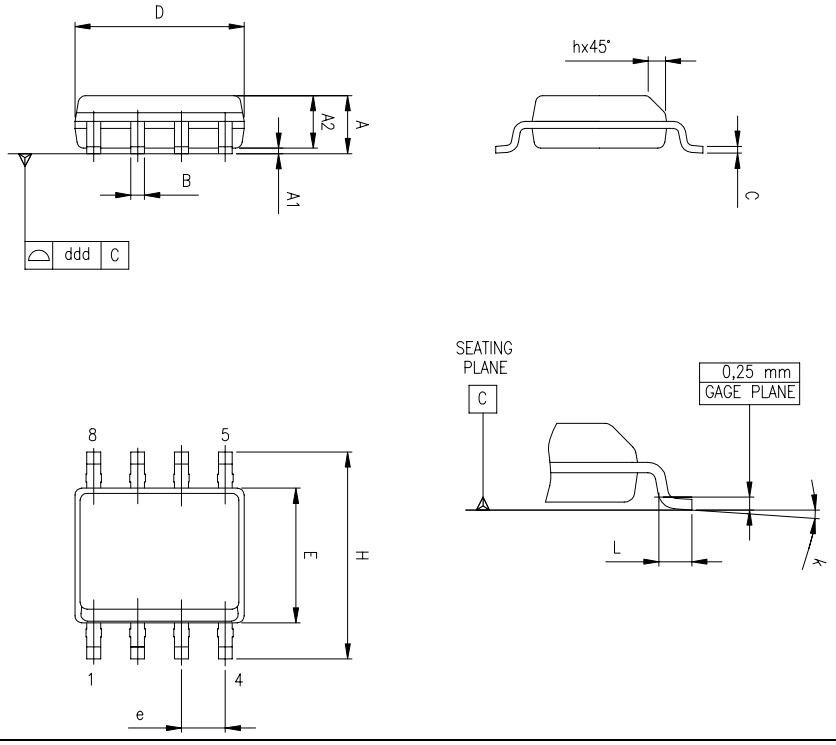


Table 1. Revision History

Date	Revision	Description of Changes
February 2003	8	First Issue
December 2005	9	Added new Ordering Numbers: L6932D1.5 & L6932D1.5TR.

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