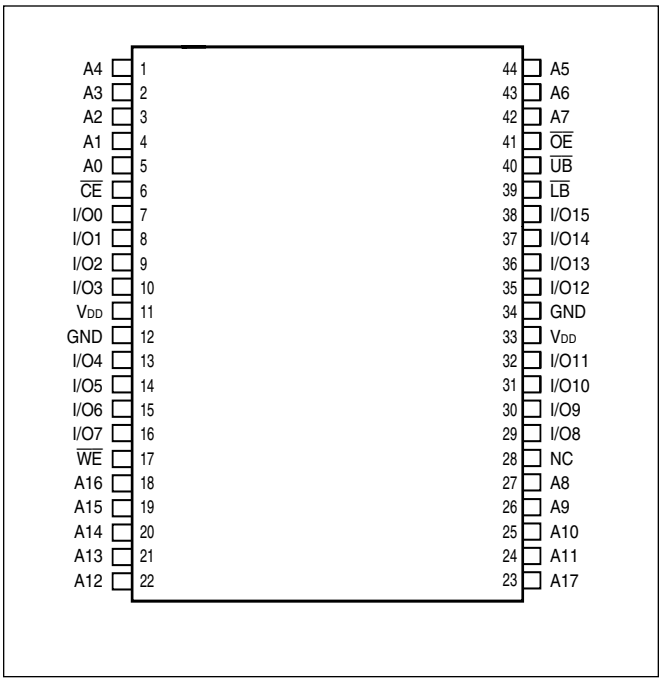
## PIN CONFIGURATIONS*

### 44-Pin TSOP (Type II)




*Please contact ISSI at SRAM@issi.com for availability of 48-pin BGA and 44-pin SOJ packages.

## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A17 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |

| | |
|---|---|
| $\overline{LB}$ | Lower-byte Control (I/O0-I/O7) |
| $\overline{UB}$ | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| $V_{DD}$ | Power |
| GND | Ground |

## TRUTH TABLE

| Mode | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O PIN I/O0-I/O7 | I/O PIN I/O8-I/O15 | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| Not Selected | X | H | X | X | X | High-Z | High-Z | $I_{SB1}$, $I_{SB2}$ |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | $I_{CC1}$, $I_{CC2}$ |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | $D_{OUT}$ | High-Z | $I_{CC1}$, $I_{CC2}$ |
| | H | L | L | H | L | High-Z | $D_{OUT}$ | |
| | H | L | L | L | L | $D_{OUT}$ | $D_{OUT}$ | |
| Write | L | L | X | L | H | $D_{IN}$ | High-Z | $I_{CC1}$, $I_{CC2}$ |
| | L | L | X | H | L | High-Z | $D_{IN}$ | |
| | L | L | X | L | L | $D_{IN}$ | $D_{IN}$ | |

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.5 | W |
| $I_{OUT}$ | DC Output Current (LOW) | 20 | mA |

**Notes:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 5.0V.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –1.0 mA | | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 2.1 mA | | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage(1) | | | 2.2 | $V_{DD}$ + 0.5 | V |
| $V_{IL}$ | Input LOW Voltage(1) | | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | Com. | –1 | 1 | µA |
| | | | Ind. | –2 | 2 | |
| | | | Auto. | –5 | 5 | |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$ | Com. | –1 | 1 | µA |
| | | Outputs Disabled | Ind. | –2 | 2 | |
| | | | Auto. | –5 | 5 | |

**Note:**
1. $V_{ILL}$ (min) = -2.0V AC (pulse width <10 ns). Not 100% tested.
   $V_{IHH}$ (max) = $V_{DD}$ + 2.0V AC (pulse width <10 ns). Not 100% tested.

## OPERATING RANGE

| Range | Ambient Temperature | $V_{DD}$ | Speed (ns) |
|---|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% | 45 |
| Industrial | -40°C to +85°C | 5V ± 10% | 45 |
| Automotive | -40°C to +125°C | 5V ± 10% | 45 |

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -45 ns Min. | -45 ns Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Average operating Current | $\overline{CE}$ = $V_{IL}$, $V_{DD}$ = Max., $I_{OUT}$= 0 mA, f = 0 | Com. | — | 10 | mA |
| | | | Ind. | — | 10 | |
| | | | Auto. | — | 10 | |
| $I_{CC1}$ | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}$ = Max., $\overline{CE}$ = $V_{IL}$ $I_{OUT}$ = 0 mA, f = $f_{MAX}$ $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | Com. | — | 15 | mA |
| | | | Ind. | — | 20 | |
| | | | Auto. | — | 25 | |
| | | | typ.[2] | 10 | | |
| $I_{SB1}$ | TTL Standby Current (TTL Inputs) | $V_{DD}$ = Max., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\overline{CE}$ ≥ $V_{IH}$, f = 0 | Com. | — | 1 | mA |
| | | | Ind. | — | 1.5 | |
| | | | Auto. | — | 2 | |
| $I_{SB2}$ | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = Max., $\overline{CE}$ ≥ $V_{DD}$ – 0.2V, $V_{IN}$ ≥ $V_{DD}$ – 0.2V, or $V_{IN}$ ≤ $V_{SS}$ + 0.2V, f = 0 | Com. | — | 10 | µA |
| | | | Ind. | — | 15 | |
| | | | Auto. | — | 35 | |
| | | | typ.[2] | 4 | | |

**Note:**
1. At f = $f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at $V_{DD}$ = 5V, $T_A$ = 25°C and not 100% tested.

## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| | | -45 | | |
|---|---|---|---|---|
| Symbol | Parameter | Min. | Max. | Unit |
| $t_{RC}$ | Read Cycle Time | 45 | — | ns |
| $t_{AA}$ | Address Access Time | — | 45 | ns |
| $t_{OHA}$ | Output Hold Time | 3 | — | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | — | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | — | 20 | ns |
| $t_{HZOE}$[2] | $\overline{OE}$ to High-Z Output | 0 | 15 | ns |
| $t_{LZOE}$[2] | $\overline{OE}$ to Low-Z Output | 5 | — | ns |
| $t_{HZCE}$[2] | $\overline{CE}$ to High-Z Output | 0 | 15 | ns |
| $t_{LZCE}$[2] | $\overline{CE}$ to Low-Z Output | 5 | — | ns |
| $t_{BA}$ | $\overline{LB}$, $\overline{UB}$ Access Time | — | 45 | ns |
| $t_{HZB}$ | $\overline{LB}$, $\overline{UB}$ to High-Z Output | 0 | 15 | ns |
| $t_{LZB}$ | $\overline{LB}$, $\overline{UB}$ to Low-Z Output | 0 | — | ns |

**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

## AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

## AC TEST LOADS

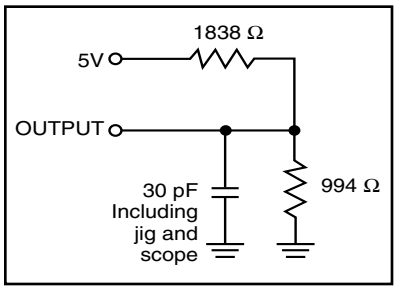



Figure 1

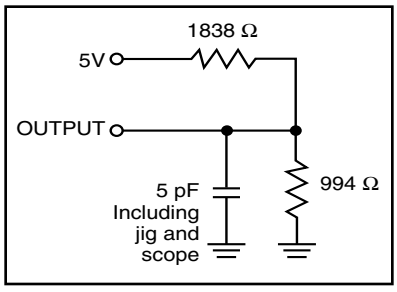
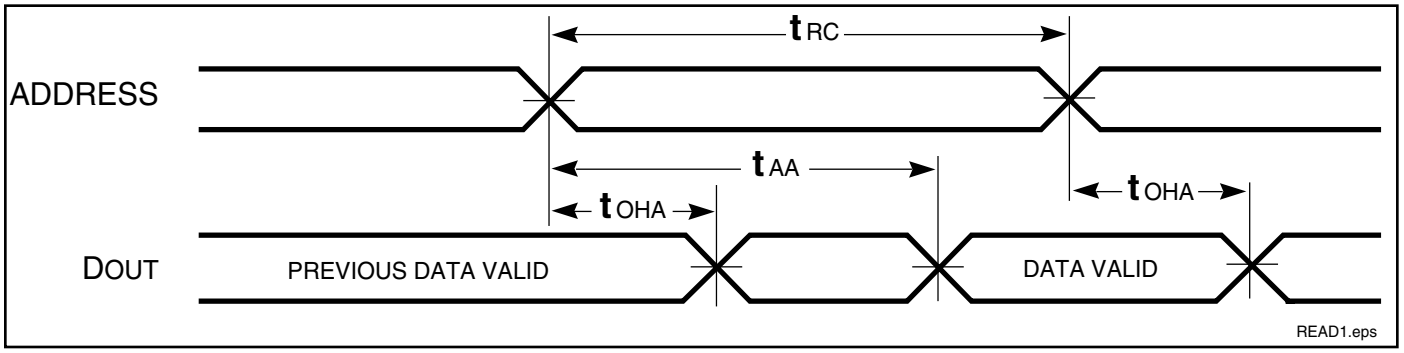


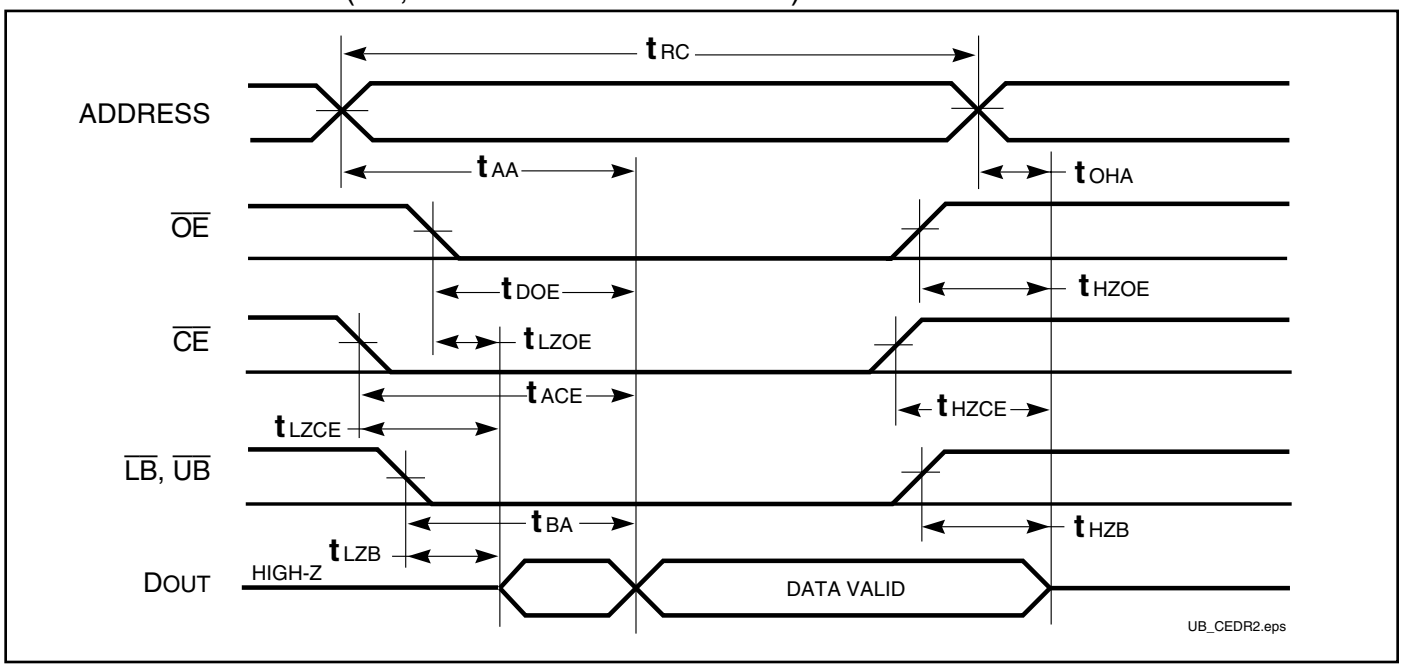

Figure 2

## AC WAVEFORMS

### READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{UB}$ or $\overline{LB}$ = $V_{IL}$)




### READ CYCLE NO. 2[1,3] ($\overline{CE}$, $\overline{OE}$ and $\overline{UB}$/$\overline{LB}$ Controlled)




**Notes:**
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = $V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

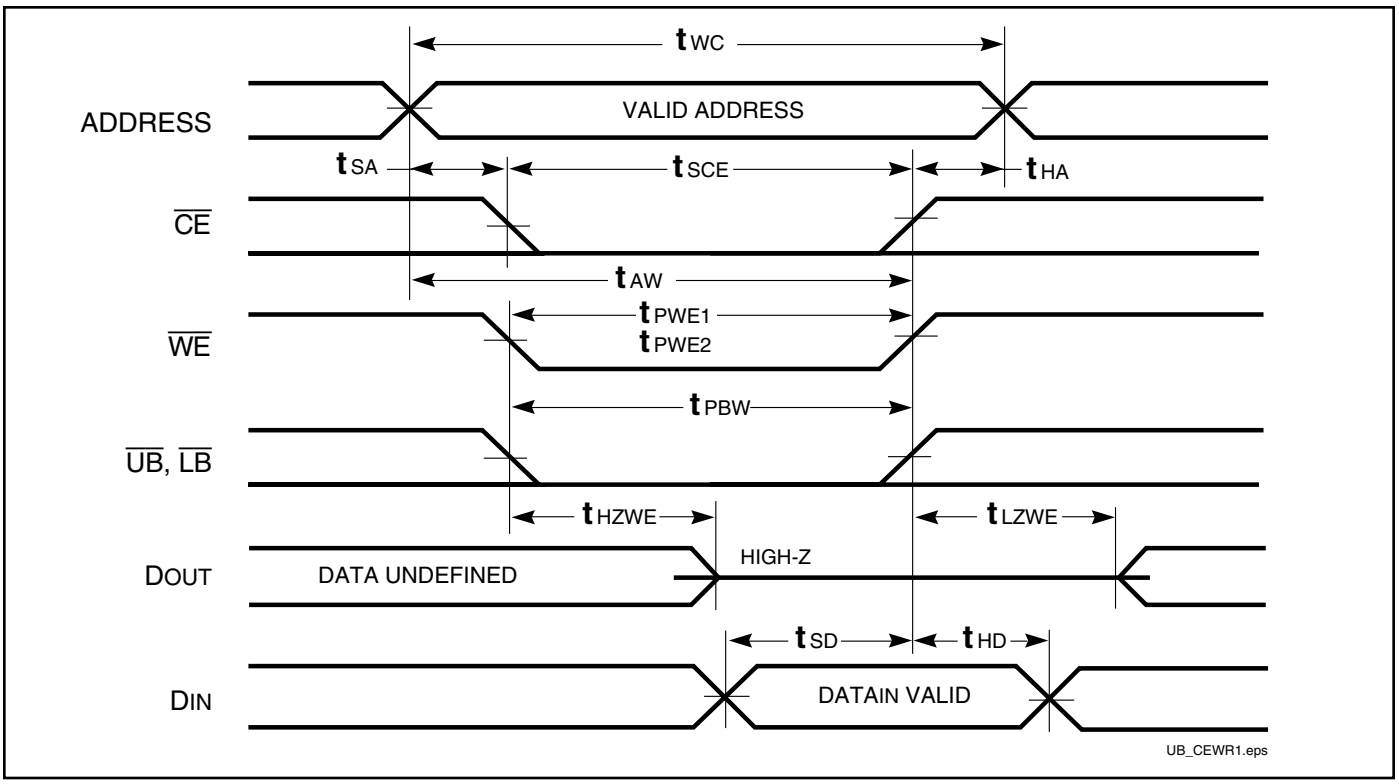
## WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

| | | -45 | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Unit** |
| $t_{WC}$ | Write Cycle Time | 45 | — | ns |
| $t_{SCE}$ | $\overline{CE}$ to Write End | 35 | — | ns |
| $t_{AW}$ | Address Setup Time to Write End | 35 | — | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | — | ns |
| $t_{SA}$ | Address Setup Time | 0 | — | ns |
| $t_{PWB}$ | $\overline{LB}$, $\overline{UB}$ Valid to End of Write | 35 | — | ns |
| $t_{PWE1}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$ =High) | 35 | — | ns |
| $t_{PWE2}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$=Low) | 35 | — | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | ns |
| $t_{HZWE}$[2] | $\overline{WE}$ LOW to High-Z Output | — | 20 | ns |
| $t_{LZWE}$[2] | $\overline{WE}$ HIGH to Low-Z Output | 5 | — | ns |

**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

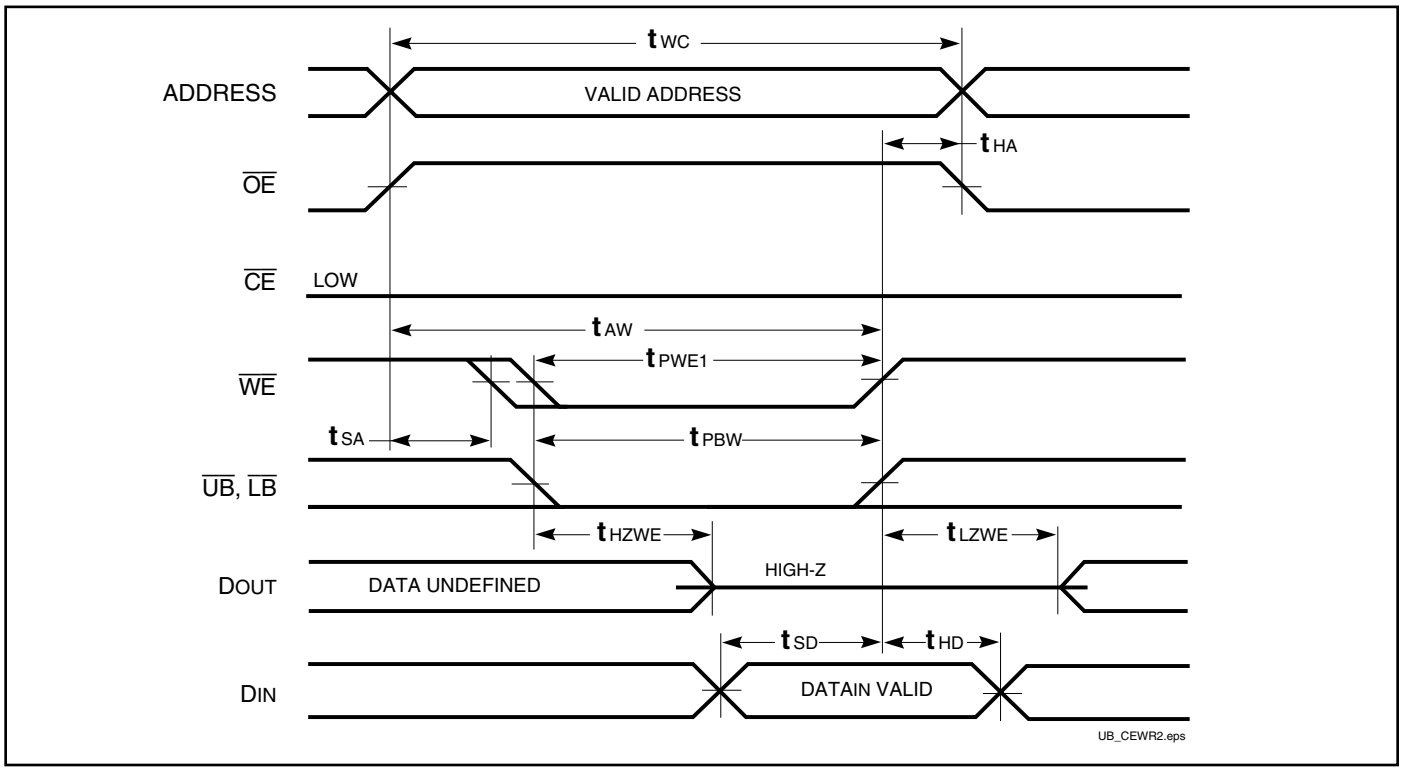
## AC WAVEFORMS

### WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]

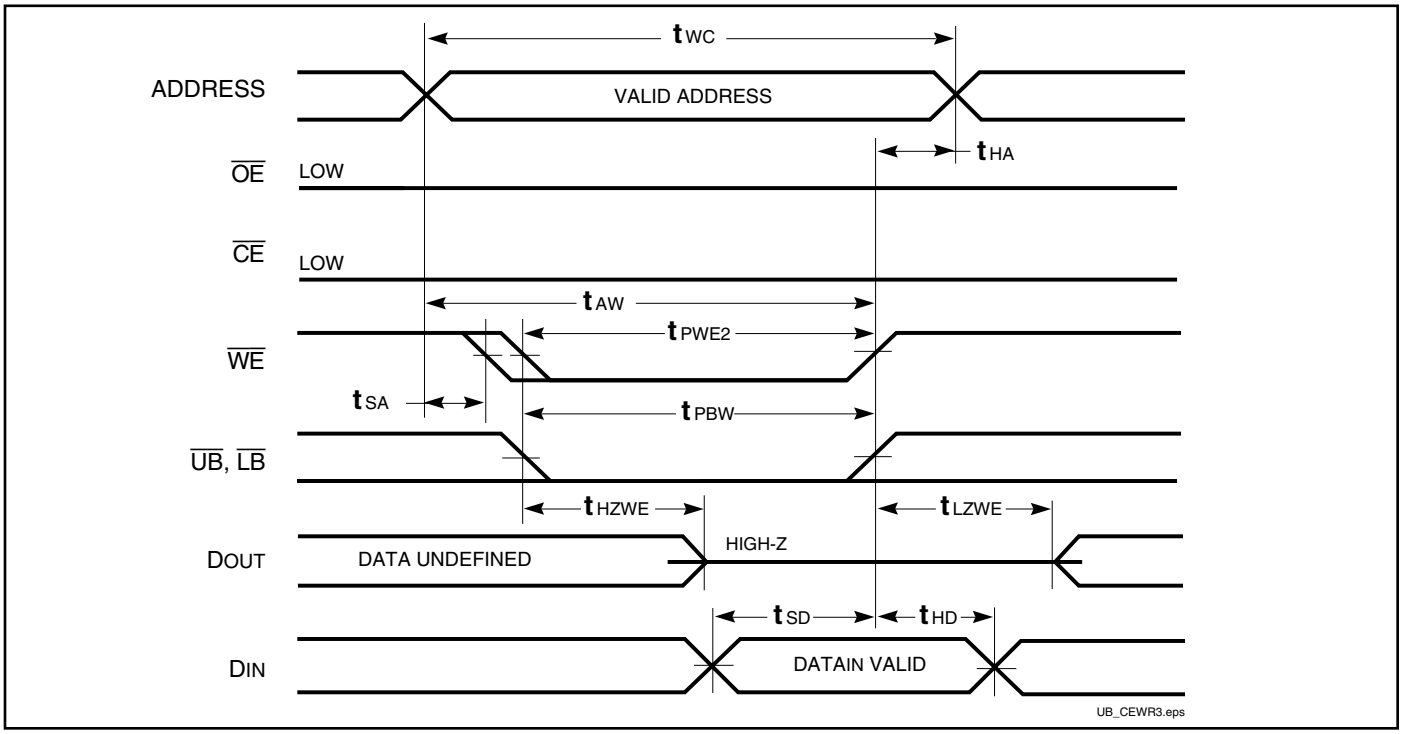



**Notes:**
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [ ($\overline{LB}$) = ($\overline{UB}$) ] ($\overline{WE}$).

## WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



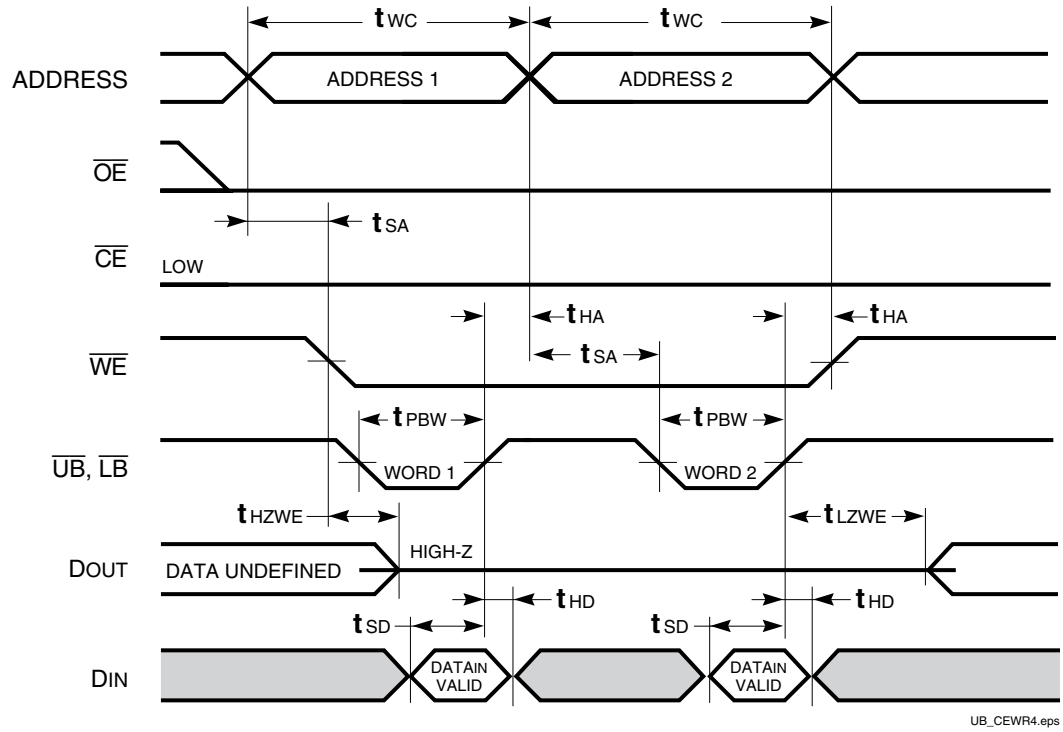

## WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]




**Notes:**

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

## WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Back to Back Write)



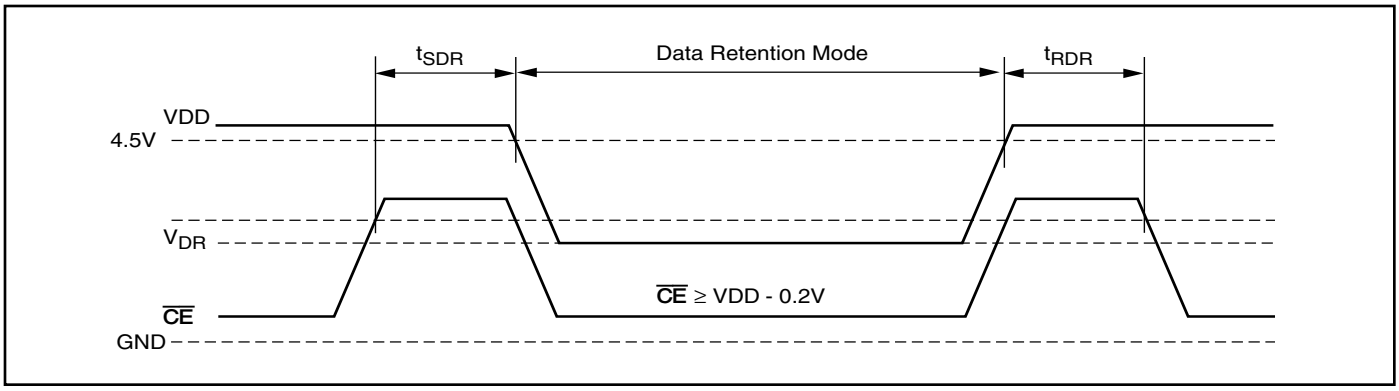
## DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 2.0 | 5.5 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$ = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. | — | 10 | µA |
| | | $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$ | Ind. | — | 15 | |
| | | | Auto. | — | 35 | |
| | | | typ. [1] | 2 | | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | $t_{RC}$ | — | ns |

**Note:**

1. Typical Values are measured at $V_{DD}$ = 5V, $T_A$ = 25ºC and not 100% tested.

## DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



## ORDERING INFORMATION: IS62C25616BL

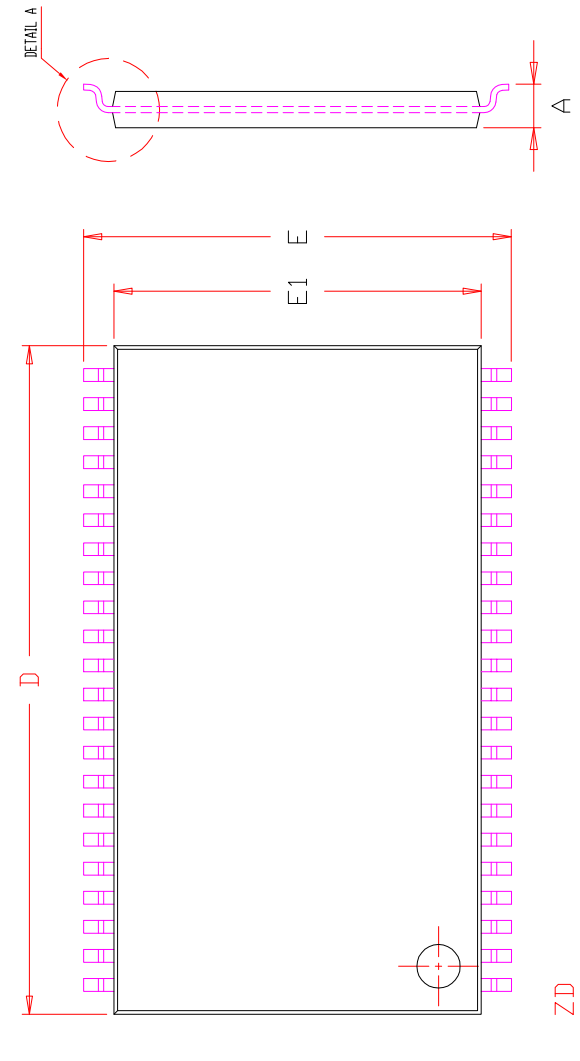
### Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 45 | IS62C25616BL-45TI | 44-pin TSOP-II |
| | IS62C25616BL-45TLI | 44-pin TSOP-II, Lead-free |

### Automotive Range: –40°C to +125°C

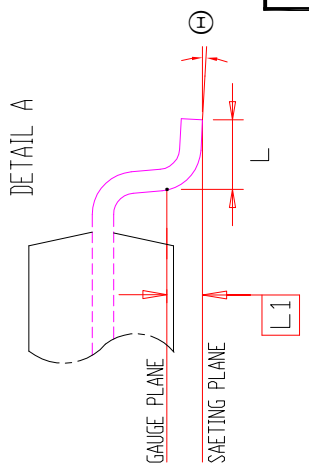
| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 45 | IS65C25616BL-45CTLA3 | 44-pin TSOP-II, Lead-free, Copper Leadframe |

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | — | 1.20 | 0.039 | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | — | 0.45 | 0.012 | — | 0.018 |
| D | 18.28 | 18.41 | 18.54 | 0.720 | 0.725 | 0.730 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 0.80 BSC, | | | 0.031 BSC, | | |
| L | 0.40 | — | 0.69 | 0.016 | — | 0.027 |
| L1 | 0.25 BSC, | | | 0.010 BSC, | | |
| ZD | 0.805 REF, | | | 0.032 REF, | | |
| Θ | 0 | — | 8° | 0 | — | 8° |




NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.




| | TITLE | REV. | DATE |
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