

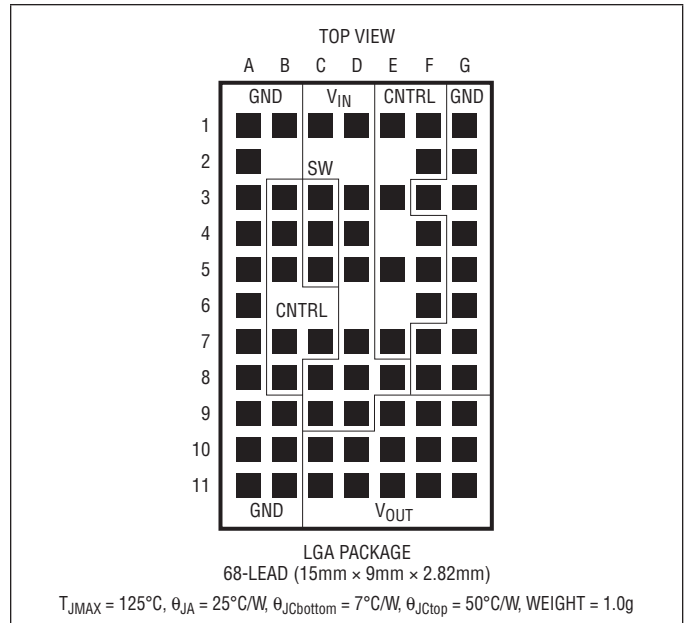
LTM4608

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} , SV_{IN}	-0.3V to 6V
CLKOUT	-0.3V to 2V
PGOOD, PLLLPF, CLKIN, PHMODE, MODE..	-0.3V to V_{IN}
I_{TH} , I_{THM} , RUN, FB, TRACK, MGN, BSEL.....	-0.3V to V_{IN}
V_{OUT} , V_{SW}	-0.3V to ($V_{IN} + 0.3V$)
Operating Temperature Range (Note 2)....	-40°C to 85°C
Junction Temperature	125°C
Storage Temperature Range	-55°C to 125°C

PIN CONFIGURATION



For easier board layout and PCB assembly due to increased spacing between land grid pads, please refer to the LTM4608A.

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (NOTE 2)
LTM4608EV#PBF	LTM4608V	68-Lead (15mm × 9mm × 2.82mm) LGA	-40°C to 85°C
LTM4608IV#PBF	LTM4608V	68-Lead (15mm × 9mm × 2.82mm) LGA	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at $T_A = 25^{\circ}C$. $V_{IN} = 5V$ unless otherwise noted. See Figure 1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{IN(DC)}$	Input DC Voltage		● 2.7		5.5	V	
$V_{OUT(DC)}$	Output Voltage	$C_{IN} = 10\mu F \times 1$, $C_{OUT} = 100\mu F$ Ceramic, 100 μF POSCAP, $R_{FB} = 6.65k$, MODE = 0V $V_{IN} = 2.7V$ to 5.5V, $V_{OUT} = 1.5V$, $I_{OUT} = 0A$		1.475	1.49	1.505	V
			● 1.468	1.49	1.512	V	
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	SV_{IN} Rising SV_{IN} Falling	2.05	2.2	2.35	V	
			1.85	2.0	2.15	V	

4608fd

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 5\text{V}$ unless otherwise noted. See Figure 1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{Q(VIN)}$	Input Supply Bias Current	$V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.5\text{V}$, No Switching, MODE = V_{IN}		400		μA
		$V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.5\text{V}$, No Switching, MODE = 0V		1.15		mA
		$V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.5\text{V}$, Switching Continuous		55		mA
		$V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, No Switching, MODE = V_{IN}		450		μA
$I_{S(VIN)}$	Input Supply Current	$V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, No Switching, MODE = 0V		1.3		mA
		$V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, Switching Continuous		75		mA
		Shutdown, RUN = 0, $V_{IN} = 5\text{V}$		1		μA
$I_{S(VIN)}$	Input Supply Current	$V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 8\text{A}$		4.5		A
		$V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 8\text{A}$		2.93		A

Output Specifications

$I_{OUT(DC)}$	Output Continuous Current Range (See Output Current Derating Curves for Different V_{IN} , V_{OUT} and T_A)	$V_{OUT} = 1.5\text{V}$		0		8	A
		$V_{IN} = 3.3\text{V}$, 5.5V		0		5	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	$V_{OUT} = 1.5\text{V}$, V_{IN} from 2.7V to 5.5V, $I_{OUT} = 0\text{A}$	●		0.1	0.2	%/V
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	$V_{OUT} = 1.5\text{V}$ $V_{IN} = 3.3\text{V}$, 5.5V, $I_{LOAD} = 0\text{A}$ to 8A $V_{IN} = 2.7\text{V}$, $I_{LOAD} = 0\text{A}$ to 5A	●		0.3	0.75	%
			●		0.3	0.75	%
$V_{OUT(AC)}$	Output Ripple Voltage	$I_{OUT} = 0\text{A}$, $C_{OUT} = 100\mu\text{F}/\text{X5R}/\text{Ceramic}$, $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$			10		mV _{p-p}
f_S	Switching Frequency	$I_{OUT} = 8\text{A}$, $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$		1.3	1.5	1.7	MHz
f_{SYNC}	SYNC Capture Range			0.75		2.25	MHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	$C_{OUT} = 100\mu\text{F}$, $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 0\text{A}$ $V_{IN} = 3.3\text{V}$ $V_{IN} = 5\text{V}$			10		mV
					10		mV
t_{START}	Turn-On Time	$C_{OUT} = 100\mu\text{F}$, $V_{OUT} = 1.5\text{V}$, $V_{IN} = 5\text{V}$ $I_{OUT} = 1\text{A}$ Resistive Load, Track = V_{IN}			100		μs
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 100\mu\text{F}$ Ceramic, 100 μF POSCAP, $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$			15		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, $C_{OUT} = 100\mu\text{F}$			10		μs
$I_{OUT(PK)}$	Output Current Limit	$C_{OUT} = 100\mu\text{F}$ $V_{IN} = 2.7\text{V}$, $V_{OUT} = 1.5\text{V}$ $V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.5\text{V}$ $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$			8		A
					11		A
					13		A

Control Section

V_{FB}	Voltage at FB Pin	$I_{OUT} = 0\text{A}$, $V_{OUT} = 1.5\text{V}$, $V_{IN} = 2.7\text{V}$ to 5.5V	●	0.592	0.596	0.600	V
				0.589	0.596	0.603	V
SS Delay	Internal Soft-Start Delay			90		μs	
I_{FB}				0.2		μA	
V_{RUN}	RUN Pin On/Off Threshold	RUN Rising		1.4	1.55	1.7	V
		RUN Falling		1.3	1.4	1.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 5\text{V}$ unless otherwise noted. See Figure 1.

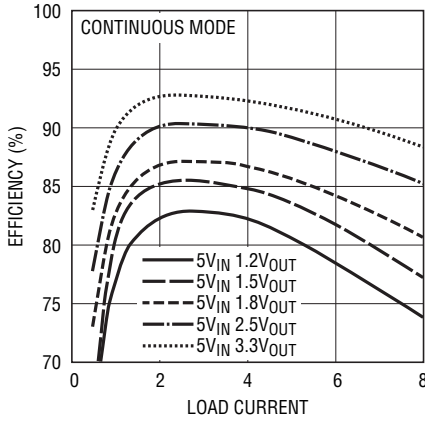
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRACK	Tracking Threshold (Rising)	$\text{RUN} = V_{IN}$		0.57		V
	Tracking Threshold (Falling)	$\text{RUN} = 0\text{V}$		0.18		V
	Tracking Disable Threshold			$V_{IN} - 0.5$		V
R_{FBHI}	Resistor Between V_{OUT} and FB Pins		9.95	10	10.05	$k\Omega$
ΔV_{PGOOD}	PGOOD Range			± 10		%
%Margining	Output Voltage Margining Percentage	$\text{MGN} = V_{IN}$, $\text{BSEL} = 0\text{V}$	4	5	6	%
		$\text{MGN} = V_{IN}$, $\text{BSEL} = V_{IN}$	9	10	11	%
		$\text{MGN} = V_{IN}$, $\text{BSEL} = \text{Float}$	14	15	16	%
		$\text{MGN} = 0\text{V}$, $\text{BSEL} = 0\text{V}$	-4	-5	-6	%
		$\text{MGN} = 0\text{V}$, $\text{BSEL} = V_{IN}$	-9	-10	-11	%
		$\text{MGN} = 0\text{V}$, $\text{BSEL} = \text{Float}$	-14	-15	-16	%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

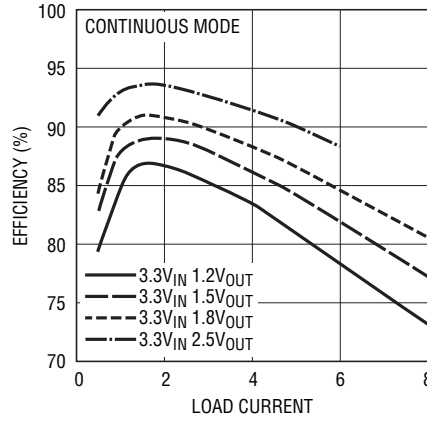
Note 2: The LTM4608E is guaranteed to meet performance specifications from 0°C to 85°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4608I is guaranteed over the -40°C to 85°C temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

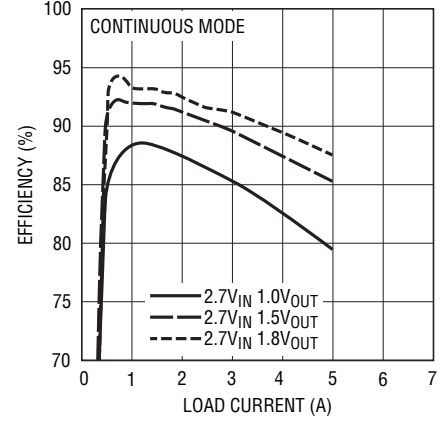
Efficiency vs Load Current



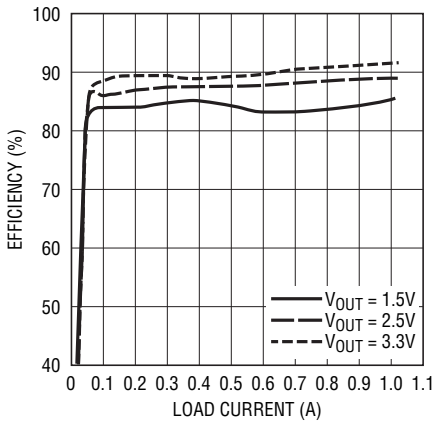
Efficiency vs Load Current



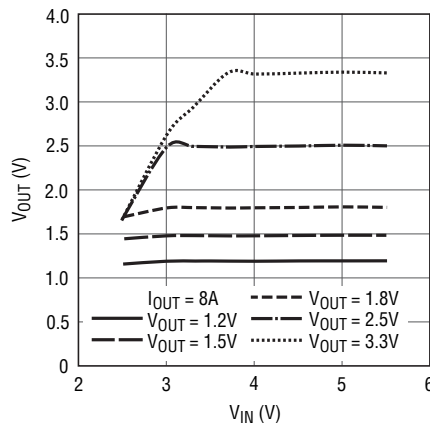
Efficiency vs Load Current



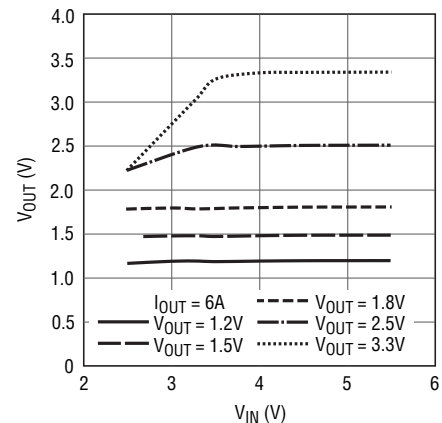
Burst Mode Efficiency with 5V Input



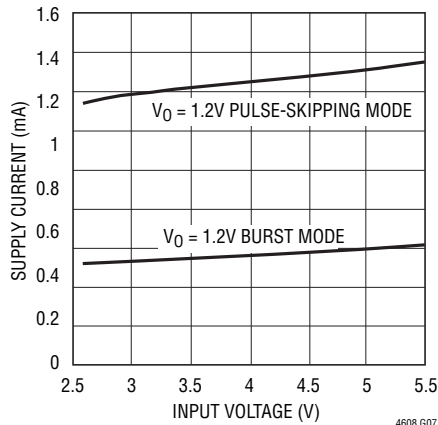
V_{IN} to V_{OUT} Step-Down Ratio



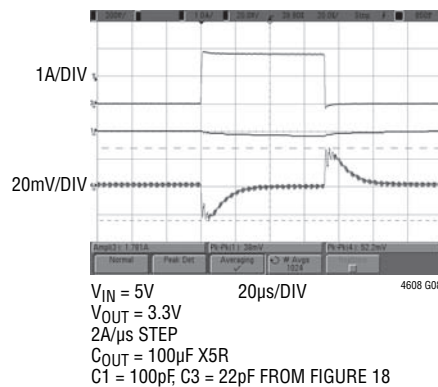
V_{IN} to V_{OUT} Step-Down Ratio



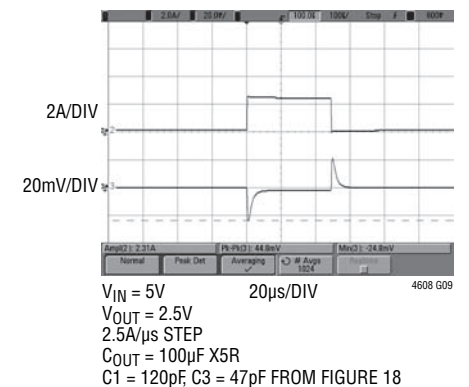
Supply Current vs V_{IN}



Load Transient Response

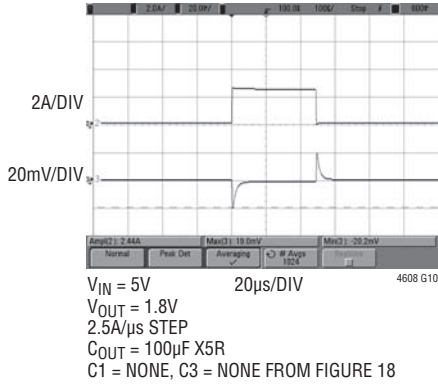


Load Transient Response

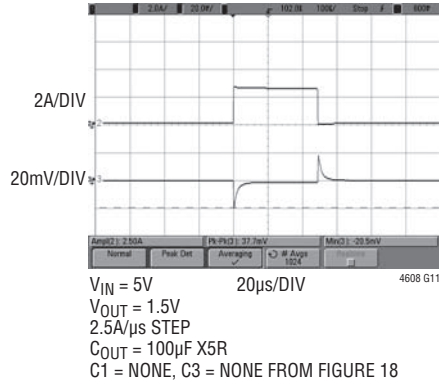


TYPICAL PERFORMANCE CHARACTERISTICS

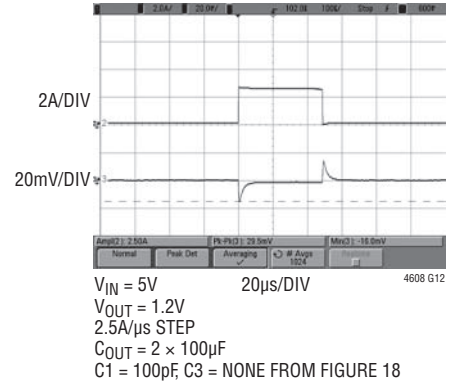
Load Transient Response



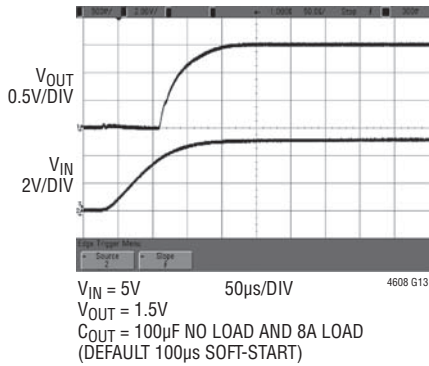
Load Transient Response



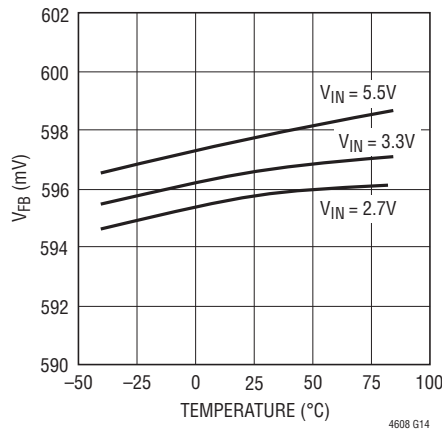
Load Transient Response



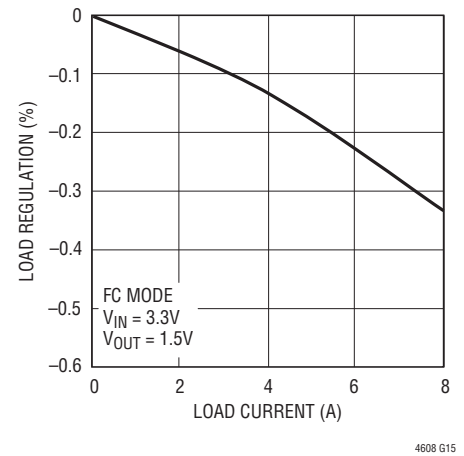
Start-Up



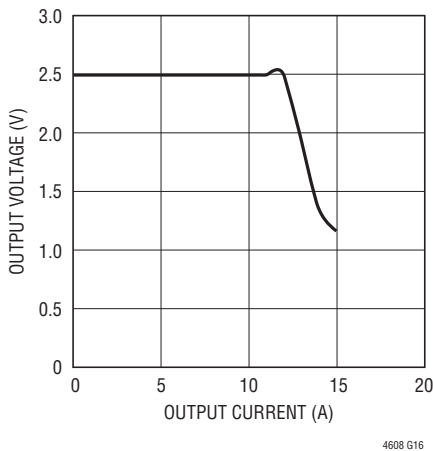
V_{FB} vs Temperature



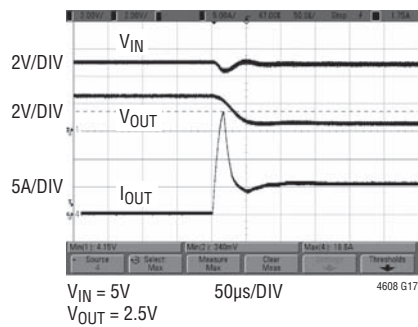
Load Regulation vs Current



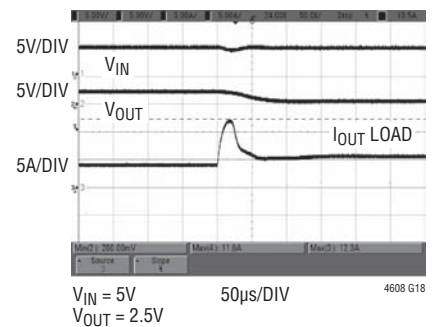
2.5V Output Current



Short-Circuit Protection (2.5V Short, No Load)



Short-Circuit Protection (2.5V Short, 4A Load)



PIN FUNCTIONS

V_{IN} (C1, C8, C9, D1, D3-D5, D7-D9 and E8): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT} (C10-C11, D10-D11, E9-E11, F9-F11, G9-G11): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 1.

GND (A1-A11, B1, B9-B11, F3, F7-F8, G1-G8): Power Ground Pins for Both Input and Output Returns.

SV_{IN} (F4): Signal Input Voltage. This pin is internally connected to V_{IN} through a lowpass filter.

SGND (E1): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to GND in the application.

MODE (B5): Mode Select Input. Tying this pin high enables Burst Mode[®] operation. Tying this pin low enables forced continuous operation. Floating this pin or tying it to V_{IN}/2 enables pulse-skipping operation.

CLKIN (B3): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with a 50k resistor. The phase-locked loop will force the internal top power PMOS turn on to be synchronized with the rising edge of the CLKIN signal. Connect this pin to SV_{IN} to enable spread spectrum modulation. During external synchronization, make sure the PLLPF pin is not tied to V_{IN} or GND.

PLLLPF (E3): Phase-Locked Loop Lowpass Filter. An internal lowpass filter is tied to this pin. In spread spectrum mode, placing a capacitor here to SGND controls the slew rate from one frequency to the next. Alternatively, floating this pin allows normal running frequency at 1.5MHz, tying this pin to SV_{IN} forces the part to run at 1.33 times its normal frequency (2MHz), tying it to ground forces the frequency to run at 0.67 times its normal frequency (1MHz).

PHMODE (B4): Phase Selector Input. This pin determines the phase relationship between the internal oscillator and CLKOUT. Tie it high for 2-phase operation, tie it low for 3-phase operation, and float or tie it to V_{IN}/2 for 4-phase operation.

MGN (B8): Margining Pin. Increases or decreases the output voltage by the amount specified by the BSEL pin. To disable margining, tie the MGN pin to a voltage divider with 50k resistors from V_{IN} to ground. See the Applications Information section and Figure 20.

BSEL (B7): Margining Bit Select Pin. Tying BSEL low selects ±5%, tying it high selects ±10%. Floating it or tying it to V_{IN}/2 selects ±15%.

TRACK (E5): Output Voltage Tracking Pin. Voltage tracking is enabled when the TRACK voltage is below 0.57V. If tracking is not desired, then connect the TRACK pin to SV_{IN}. If TRACK is not tied to SV_{IN}, then the TRACK pin's voltage needs to be below 0.18V before the chip shuts down even though RUN is already low. Do not float this pin. A resistor divider and capacitor can be applied to the TRACK pin to increase the soft-start time of the regulator. See the Applications Information section. Can tie together for parallel operation and tracking. Load current needs to be present during track down.

PIN FUNCTIONS

FB (E7): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 10k precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase® operation, tie FB pins together for parallel operation. See the Applications Information section for details.

I_{TH} (F6): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Tie together in parallel operation.

I_{THM} (F5): Negative Input to the Internal I_{TH} Differential Amplifier. Tie this pin to SGND for single phase operation. For PolyPhase operation, tie the master's I_{THM} to SGND while connecting all of the I_{THM} pins together.

PGOOD (C7): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within $\pm 10\%$ of the regulation point. Disabled during margining.

RUN (F1): Run Control Pin. A voltage above 1.5V will turn on the module.

SW (C3-C5): Switching Node of the Circuit is Used for Testing Purposes. This can be connected to an electrically open circuit copper pad on the board for improved thermal performance.

CLKOUT (F2): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT is determined by the state of the PHMODE pin.

SIMPLIFIED BLOCK DIAGRAM

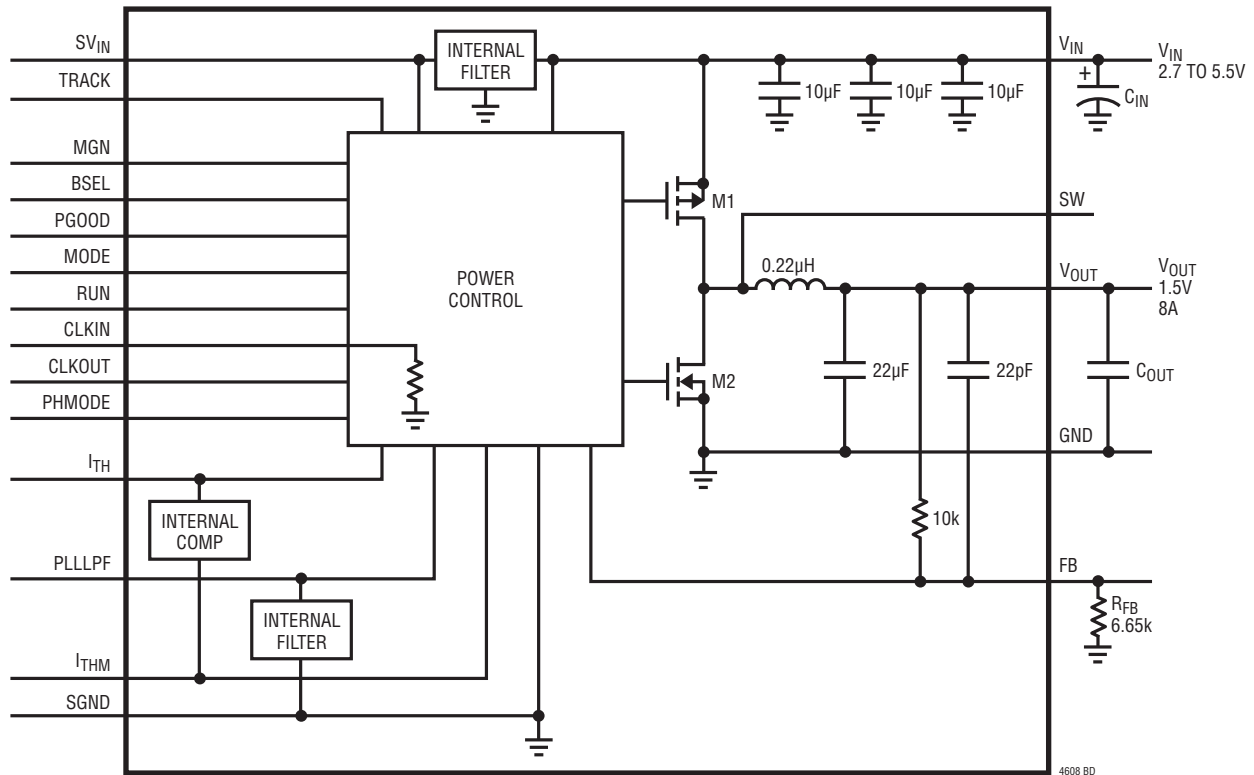


Figure 1. Simplified LTM4608 Block Diagram

Table 1. Decoupling Requirements. $T_A = 25^\circ\text{C}$, Block Diagram Configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement ($V_{IN} = 2.7\text{V to } 5.5\text{V}$, $V_{OUT} = 1.5\text{V}$)	$I_{OUT} = 8\text{A}$	10			μF
C_{OUT}	External Output Capacitor Requirement ($V_{IN} = 2.7\text{V to } 5.5\text{V}$, $V_{OUT} = 1.5\text{V}$)	$I_{OUT} = 8\text{A}$		100		μF

OPERATION

The LTM4608 is a standalone nonisolated switch mode DC/DC power supply. It can deliver up to 8A of DC output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via one external resistor from 0.6V DC to 5.0V DC over a 2.7V to 5.5V input voltage. The typical application schematic is shown in Figure 18.

The LTM4608 has an integrated constant frequency current mode regulator and built-in power MOSFET devices with fast switching speed. The typical switching frequency is

1.5MHz. For switching noise sensitive applications, it can be externally synchronized from 0.75MHz to 2.25MHz. Even spread spectrum switching can be implemented in the design to reduce noise.

With current mode control and internal feedback loop compensation, the LTM4608 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

OPERATION

Current mode control provides cycle-by-cycle fast current limit and thermal shutdown in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a $\pm 10\%$ window around the regulation point.

Pulling the RUN pin below 1.3V forces the controller into its shutdown state, by turning off both M1 and M2 at low load current. The TRACK pin is used for programming the output voltage ramp and voltage tracking during start-up. See Applications Information.

The LTM4608 is internally compensated to be stable over all operating conditions. Table 3 provides a guideline for input and output capacitances for several operating conditions. The Linear Technology μ Module Power Design Tool is provided for transient and stability analysis.

The FB pin is used to program the output voltage with a single external resistor to ground.

Multiphase operation can be easily employed with the synchronization and phase mode controls. Up to 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin to different levels. The LTM4608 has clock in and clock out for polyphasing multiple devices or frequency synchronization.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics.

Output voltage margining is supported, and can be programmed from $\pm 5\%$ to $\pm 15\%$ using the MGN and BSEL pins. The PGOOD pin is disabled during margining.

APPLICATIONS INFORMATION

The typical LTM4608 application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 3 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. The LTM4608 is 100% duty cycle, but the V_{IN} to V_{OUT} minimum dropout is a function of its load current. Please refer to the curves in the Typical Performance Characteristics section of this data sheet for more information.

Output Voltage Programming

The PWM controller has an internal 0.596V reference voltage. As shown in the Block Diagram, a 10k/0.5% internal feedback resistor connects V_{OUT} and FB pins together. The output voltage will default to 0.596V with no feedback resistor. Adding a resistor R_{FB} from FB pin to GND programs the output voltage:

$$V_{OUT} = 0.596V \cdot \frac{10k + R_{FB}}{R_{FB}}$$

Table 2. R_{FB} Resistor vs Output Voltage

V_{OUT}	0.596V	1.2V	1.5V	1.8V	2.5V	3.3V
R_{FB}	Open	10k	6.65k	4.87k	3.09k	2.21k

Input Capacitors

The LTM4608 module should be connected to a low AC impedance DC source. Three 10 μ F ceramic capacitors are included inside the module. Additional input capacitors are only needed if a large load step is required up to the 4A level. A 47 μ F to 100 μ F surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this 47 μ F capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

APPLICATIONS INFORMATION

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{\text{CIN(RMS)}} = \frac{I_{\text{OUT(MAX)}}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, polymer capacitor for bulk input capacitance due to high inductance traces or leads. If a low inductance plane is used to power the device, then only one 10 μ F ceramic is required. The three internal 10 μ F ceramics are typically rated for 2A of RMS ripple current, so the ripple current at the worse case for 8A maximum current is 4A or less.

Output Capacitors

The LTM4608 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range is from 47 μ F to 220 μ F. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is desired. Table 3 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 3A/ μ s transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 3 matrix, and the Linear Technology LTpowerCAD™ Design Tool is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Linear Technology LTpowerCAD Design Tool will calculate the output ripple reduction as the number phases implemented increases by N times.

Burst Mode Operation

The LTM4608 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply tie the MODE pin to V_{IN} . During this operation, the peak current of the inductor is set to approximately 20% of the maximum peak current value in normal operation even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below 0.2V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 450 μ A. The load current is now being supplied from the output capacitor. When the output voltage drops, causing I_{TH} to rise above 0.25V, the internal sleep line goes low, and the LTM4608 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4608 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Floating the MODE pin or tying it to $V_{\text{IN}}/2$ enables pulse-skipping operation. This allows discontinuous conduction mode (DCM) operation down to near the limit defined by the chip's minimum on-time (about 100ns). Below this output current level, the converter will begin to skip cycles in order to maintain output regulation. Increasing the output load current slightly, above the minimum required for discontinuous conduction mode, allows constant frequency PWM.

APPLICATIONS INFORMATION

Table 3. Output Voltage Response Versus Component Matrix (Refer to Figure 18) 0A to 3A Load Step

TYPICAL MEASURED VALUES													
C _{OUT1} VENDORS		VALUE	PART NUMBER		C _{OUT2} VENDORS		VALUE	PART NUMBER					
TDK		22μF, 6.3V	C3216X7S0J226M		Sanyo POSCAP		150μF, 10V	10TPD150M					
Murata		22μF, 16V	GRM31CR61C226KE15L		C _{IN} (BULK) VENDORS		VALUE	PART NUMBER					
TDK		100μF, 6.3V	C4532X5R0J107MZ		Sanyo		100μF, 10V	10CE100FH					
Murata		100μF, 6.3V	GRM32ER60J107M										

V _{OUT} (V)	C _{IN} (CERAMIC)	C _{IN} (BULK)*	C _{OUT1} (CERAMIC)	C _{OUT2} (BULK)	I _{TH}	C1	C3	V _{IN} (V)	DROOP (mV)	PEAK-TO-PEAK DEVIATION (mV)	RECOVERY TIME (μs)	LOAD STEP (A/μs)	R _{FB} (kΩ)
1.0	10μF	100μF	100μF × 2		None	68pF	None	5	13	26	7	3	14.7
1.0	10μF	100μF	22μF × 1	150μF × 2	None	None	100pF	5	17	34	8	3	14.7
1.0	10μF	100μF	100μF × 2		None	68pF	None	3.3	13	26	7	3	14.7
1.0	10μF	100μF	22μF × 1	150μF × 2	None	None	100pF	3.3	17	34	10	3	14.7
1.0	10μF	100μF	100μF × 2		None	68pF	None	2.7	13	26	7	3	14.7
1.0	10μF	100μF	22μF × 1	150μF × 2	None	None	100pF	2.7	17	34	8	3	14.7
1.2	10μF	100μF	100μF × 2		None	100pF	None	5	16	32	8	3	10
1.2	10μF	100μF	22μF × 1	150μF × 2	None	None	100pF	5	20	41	10	3	10
1.2	10μF	100μF	100μF × 2		None	100pF	None	3.3	16	32	8	3	10
1.2	10μF	100μF	22μF × 1	150μF × 2	None	None	100pF	3.3	20	41	10	3	10
1.2	10μF	100μF	100μF × 2		None	100pF	None	2.7	16	32	10	3	10
1.2	10μF	100μF	22μF × 1	150μF × 2	None	47pF	None	2.7	16	32	8	3	10
1.5	10μF	100μF	100μF × 2		None	100pF	None	5	18	36	8	3	6.65
1.5	10μF	100μF	22μF × 1	150μF × 2	None	None	47pF	5	20	41	12	3	6.65
1.5	10μF	100μF	100μF × 2		None	100pF	None	3.3	16	32	10	3	6.65
1.5	10μF	100μF	22μF × 1	150μF × 2	None	None	47pF	3.3	20	41	12	3	6.65
1.5	10μF	100μF	100μF × 2		None	100pF	None	2.7	18	36	10	3	6.65
1.5	10μF	100μF	22μF × 1	150μF × 2	None	None	None	2.7	20	41	12	3	6.65
1.8	10μF	100μF	100μF × 1		None	47pF	None	5	22	42	8	3	4.87
1.8	10μF	100μF	22μF × 1	150μF × 2	None	None	47pF	5	21	42	12	3	4.87
1.8	10μF	100μF	100μF × 2		None	120pF	None	3.3	21	43	12	3	4.87
1.8	10μF	100μF	22μF × 1	150μF × 2	None	None	47pF	3.3	21	41	12	3	4.87
1.8	10μF	100μF	100μF × 2		None	120pF	None	2.7	22	44	12	3	4.87
1.8	10μF	100μF	22μF × 1	150μF × 2	None	None	None	2.7	21	42	14	3	4.87
2.5	10μF	100μF	100μF × 1		None	100pF	None	5	28	42	10	3	3.09
2.5	10μF	100μF	22μF × 1	150μF × 1	None	22pF	None	5	33	60	10	3	3.09
2.5	10μF	100μF	100μF × 1		None	100pF	None	3.3	30	60	10	3	3.09
2.5	10μF	100μF	22μF × 1	150μF × 1	None	22pF	None	3.3	21	41	10	3	3.09
3.3	10μF	100μF	100μF × 1		100pF	22pF	None	5	38	74	10	3	2.21
3.3	10μF	100μF	22μF × 1	150μF × 1	None	None	None	5	39	75	12	3	2.21

*Bulk capacitance is optional if V_{IN} has very low input impedance.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the I_{TH} voltage is in control of the current comparator threshold

throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4608's output voltage is in regulation.

Multiphase Operation

For output loads that demand more than 8A of current, multiple LTM4608s can be cascaded to run out of phase to

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provide more output current without increasing input and output voltage ripple. The CLKIN pin allows the LTC4608 to synchronize to an external clock (between 0.75MHz and 2.25MHz) and the internal phase-locked loop allows the LTM4608 to lock onto CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following LTM4608 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to S_{VIN} , SGND or $S_{VIN}/2$ (floating) generates a phase difference (between CLKIN and CLKOUT) of 180°, 120° or 90° respectively, which corresponds to a 2-phase, 3-phase or 4-phase operation. A total of 6 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin of each LTM4608 to different levels. For a 6-phase example in Figure 2, the 2nd stage that is 120° out of phase from the 1st stage can generate a 240° (PHMODE = 0) CLKOUT signal for the 3rd stage,

which then can generate a CLKOUT signal that's 420°, or 60° (PHMODE = S_{VIN}) for the 4th stage. With the 60° CLKIN input, the next two stages can shift 120° (PHMODE = 0) for each to generate a 300° signal for the 6th stage. Finally, the signal with a 60° phase shift on the 6th stage (PHMODE is floating) goes back to the 1st stage. Figure 3 shows the configuration for a 12 phase configuration

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used.

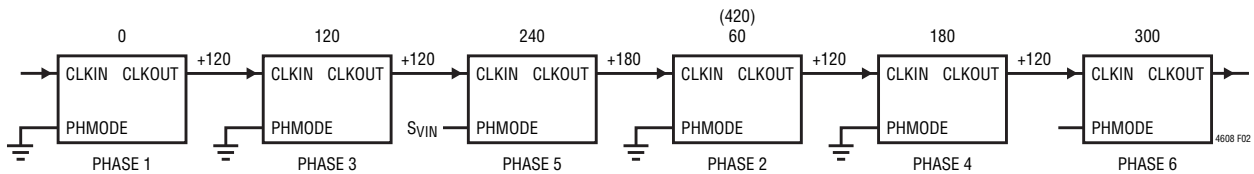


Figure 2. 6-Phase Operation

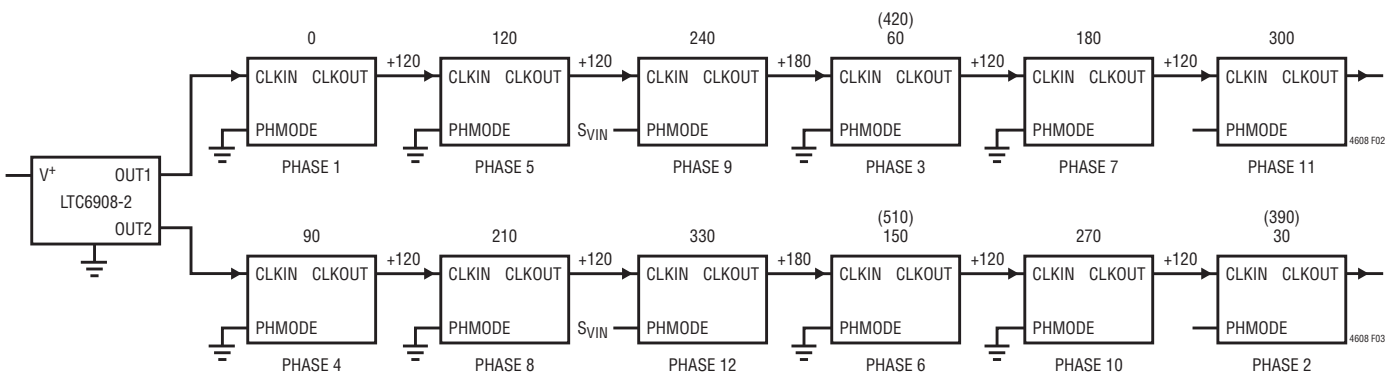


Figure 3. 12-Phase Operation

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The LTM4608 device is an inherently current mode controlled device. Parallel modules will have very good current sharing. This will balance the thermals on the design. Tie the I_{TH} pins of each LTM4608 together to share the current evenly. To reduce ground potential noise, tie the I_{THM} pins of all LTM4608s together and then connect to the SGND at only one point. Figure 19 shows a schematic of the parallel design. The FB pins of the parallel module are tied together. With parallel operation, input and output capacitors may be reduced in part according to the operating duty cycle.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

Spread Spectrum Operation

Switching regulators can be particularly troublesome where electromagnetic interference (EMI) is concerned.

Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is fixed based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

To reduce this noise, the LTM4608 can run in spread spectrum operation by tying the CLKIN pin to SV_{IN} . In spread spectrum operation, the LTM4608's internal oscillator is designed to produce a clock pulse whose period is random on a cycle-by-cycle basis but fixed between 70% and 130% of the nominal frequency. This has the benefit of spreading the switching noise over a range of frequencies, thus significantly reducing the

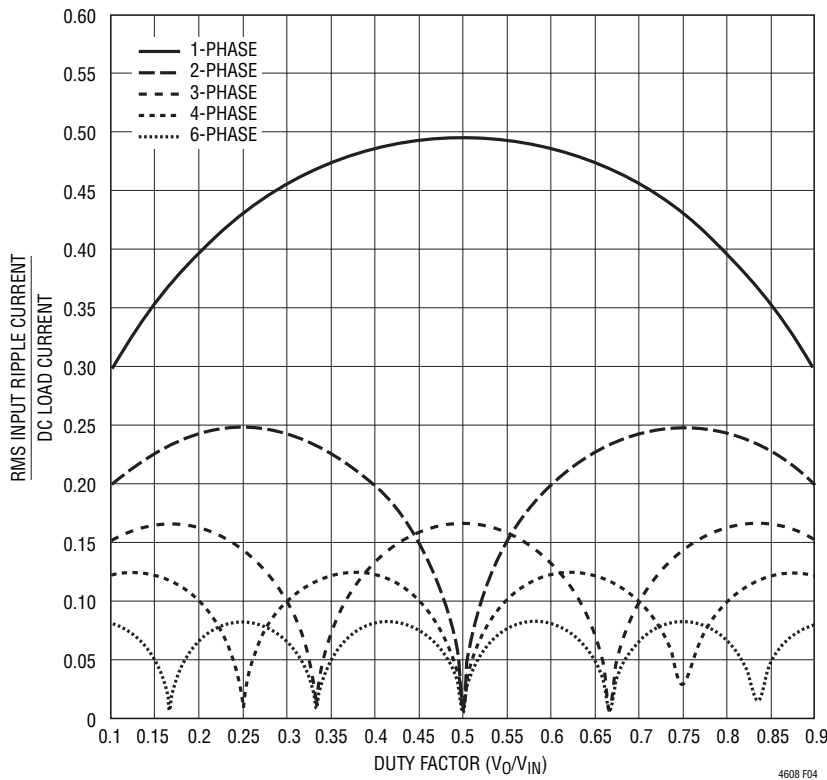


Figure 4. Normalized Input RMS Ripple Current vs Duty Factor for One to Six Modules (Phases)

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peak noise. Spread spectrum operation is disabled if CLKIN is tied to ground or if it's driven by an external frequency synchronization signal. A capacitor value of 0.01μF must be placed from the PLLPF pin to ground to control the slew rate of the spread spectrum frequency change. Add a control ramp on the TRACK pin with R_{SR} and C_{SR} referenced to V_{IN} . Figure 21 shows an example for spread spectrum operation.

$$R_{SR} \geq \frac{1}{-\ln\left(1 - \frac{0.592}{V_{IN}}\right) \cdot 500 \cdot C_{SR}}$$

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the

same as the slave regulator's feedback divider to implement coincident tracking. The LTM4608 uses an accurate 10k resistor internally for the top feedback resistor. Figure 5 shows an example of coincident tracking:

$$\text{Slave} = \left(1 + \frac{10k}{R_{FB4}}\right) \cdot V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.596V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, this resistor divider is connected to the slave's track pin. The slave will then coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.596V. R_{FB4} in Figure 5 will be equal to R_{FB2} for coincident tracking.

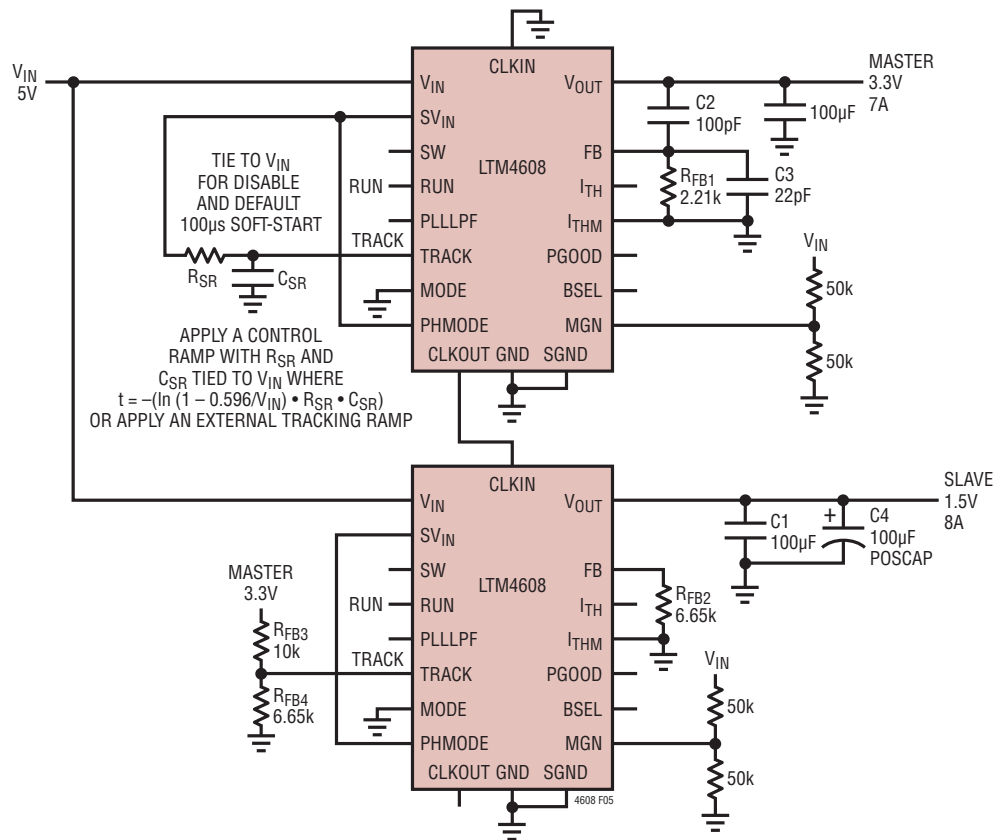


Figure 5. Dual Outputs (3.3V and 1.5V) with Tracking

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The track pin of the master can be controlled by an external ramp or by R_{SR} and C_{SR} in Figure 5 referenced to V_{IN} . The RC ramp time can be programmed using equation:

$$t = - \left(\ln \left(1 - \frac{0.596V}{V_{IN}} \right) \cdot R_{SR} \cdot C_{SR} \right)$$

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's track pin. As mentioned above, the TRACK pin has a control range from 0V to 0.596V. The master's TRACK pin slew rate is directly equal to the master's output slew rate in Volts/Time:

$$\frac{MR}{SR} \cdot 10k = R_{FB3}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{FB3} is equal the 10k. R_{FB4} is derived from equation:

$$R_{FB4} = \frac{0.596V}{\frac{V_{FB}}{10k} + \frac{V_{FB}}{R_{FB2}} - \frac{V_{TRACK}}{R_{FB3}}}$$

where V_{FB} is the feedback voltage reference of the regulator and V_{TRACK} is 0.596V. Since R_{FB3} is equal to the 10k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{FB4} is equal to R_{FB2} with $V_{FB} = V_{TRACK}$. Therefore $R_{FB3} = 10k$ and $R_{FB4} = 6.65k$ in Figure 5.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{FB3} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

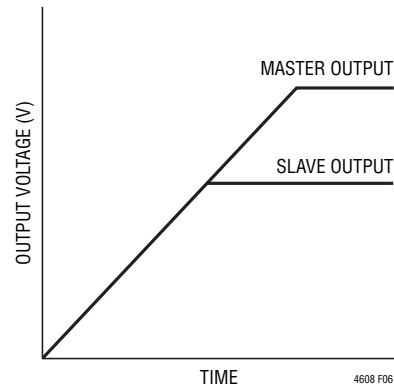


Figure 6. Output Voltage Coincident Tracking

For example: $MR = 3.3V/ms$ and $SR = 1.5V/ms$. Then $R_{FB3} = 22.1k$. Solve for R_{FB4} to equal to 4.87k.

For applications that do not require tracking or sequencing, simply tie the TRACK pin to SV_{IN} to let RUN control the turn on/off. Connecting TRACK to SV_{IN} also enables the $\sim 100\mu s$ of internal soft-start during start-up. Load current needs to be present during track down.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a $\pm 10\%$ window around the regulation point. As shown in Figure 20, the sequencing function can be realized in a dual output application by controlling the RUN pins and the PGOOD signals from each other. The 1.5V output begins its soft starting after the PGOOD signal of 3.3V output becomes high, and 3.3V output starts its shutdown after the PGOOD signal of 1.5V output becomes low. This can be applied to systems that require voltage sequencing between the core and sub-power supplies.

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Slope Compensation

The module has already been internally compensated for all output voltages. Table 3 is provided for most application requirements. A spice model will be provided for other control loop optimization. For single module operation, connect I_{THM} pin to SGND. For parallel operation, tie I_{THM} pins together and then connect to SGND at one point. Tie I_{TH} pins together to share currents evenly for all phases.

Output Margining

For a convenient system stress test on the LTM4608's output, the user can program the LTM4608's output to $\pm 5\%$, $\pm 10\%$ or $\pm 15\%$ of its normal operational voltage. The margin pin with a voltage divider is driven with a small three-state gate as shown in Figure 18, for the three margin states (high, low, no margin). When the MGN pin is $< 0.3V$, it forces negative margining in which the output voltage is below the regulation point. When MGN is $> V_{IN} - 0.3V$, the output voltage is forced above the regulation point. The amount of output voltage margining is

determined by the BSEL pin. When BSEL is low, it is 5%. When BSEL is high, it is 10%. When BSEL is floating, it is 15%. When margining is active, the internal output overvoltage and undervoltage comparators are disabled and PGOOD remains high. Margining is disabled by tying the MGN pin to a voltage divider as shown in Figure 20.

Thermal Considerations and Output Current Derating

The power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 16 for calculating an approximate θ_{JA} for the module with various heat sinking methods. Thermal models are derived from several temperature measurements at the bench, and thermal modeling analysis. Thermal Application Note 103 provides a detailed explanation of the analysis for the thermal models and the derating curves. Tables 4 and 5 provide a summary of the equivalent θ_{JA} for the noted conditions. These equivalent θ_{JA} parameters are correlated to the measured values and improve with air flow. The junction temperature is maintained at $125^{\circ}C$ or below for the derating curves.

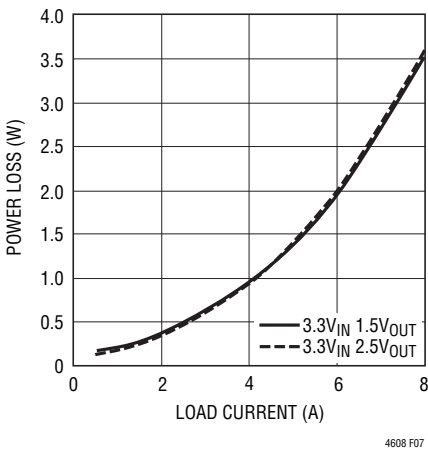


Figure 7. 3.3V_{IN}, 2.5V and 1.5V_{OUT} Power Loss

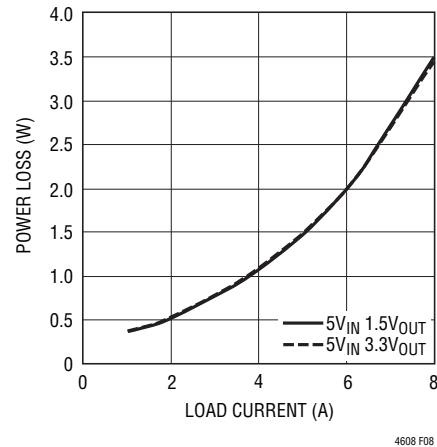


Figure 8. 5V_{IN}, 3.3V and 1.5V_{OUT} Power Loss

APPLICATIONS INFORMATION

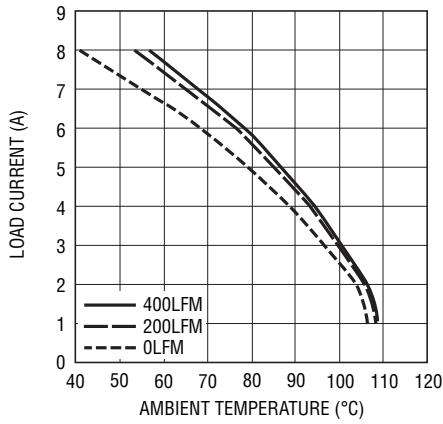


Figure 9. No Heat Sink with 3.3V_{IN} to 1.5V_{OUT}

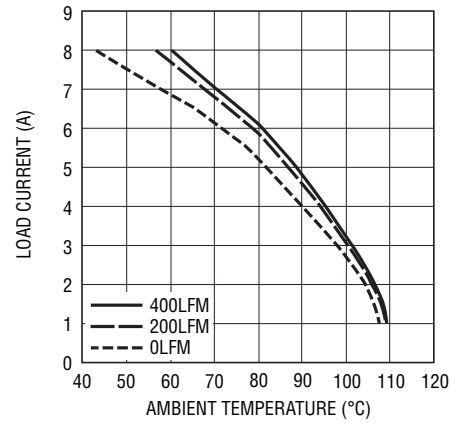


Figure 10. BGA Heat Sink with 3.3V_{IN} to 1.5V_{OUT}

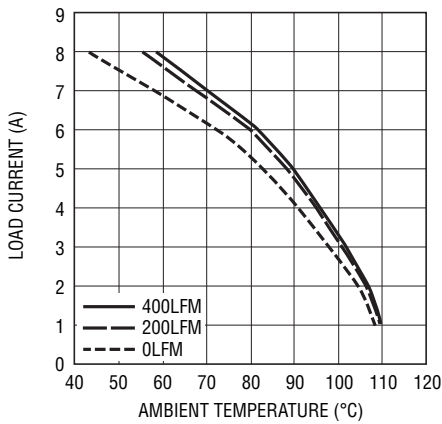


Figure 11. No Heat Sink with 5V_{IN} to 1.5V_{OUT}

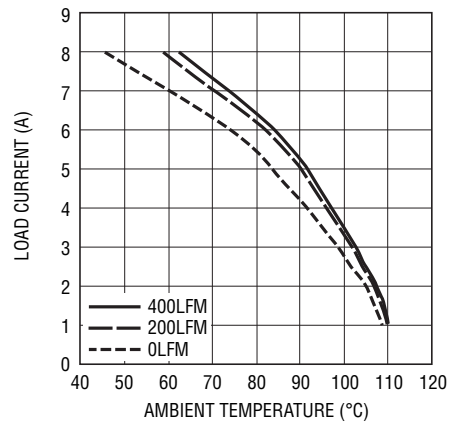


Figure 12. BGA Heat Sink with 5V_{IN} to 1.5V_{OUT}

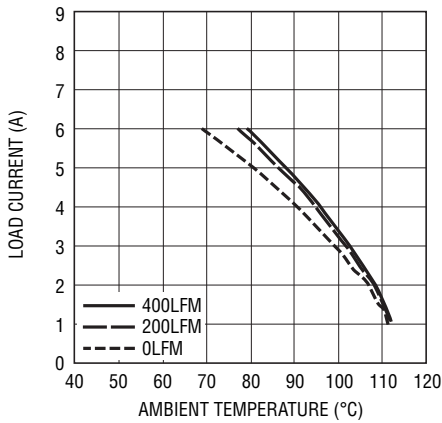


Figure 13. No Heat Sink with 3.3V_{IN} to 2.5V_{OUT}

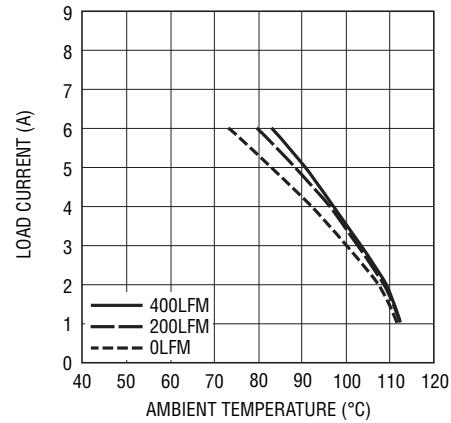


Figure 14. BGA Heat Sink with 3.3V_{IN} to 2.5V_{OUT}

APPLICATIONS INFORMATION

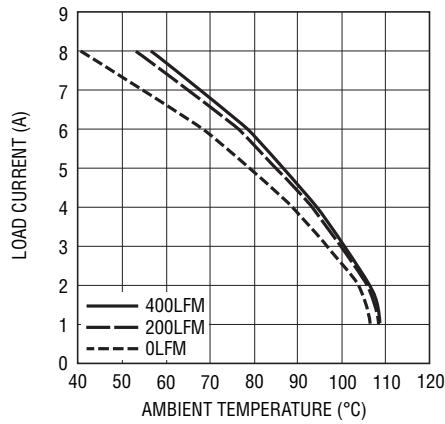


Figure 15. No Heat Sink with $5V_{IN}$ to $3.3V_{OUT}$

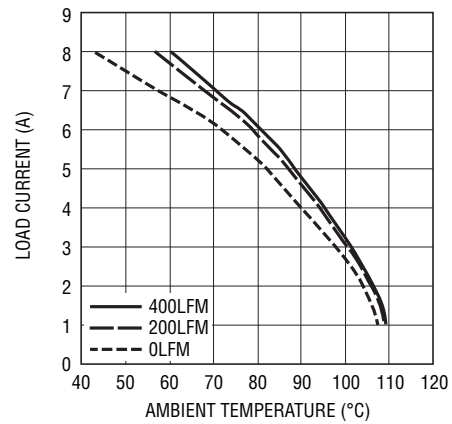


Figure 16. BGA Heat Sink with $5V_{IN}$ to $3.3V_{OUT}$

Table 4. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 9, 11	3.3, 5	Figures 7, 8	0	None	25
Figures 9, 11	3.3, 5	Figures 7, 8	200	None	21
Figures 9, 11	3.3, 5	Figures 7, 8	400	None	20
Figures 10, 12	3.3, 5	Figures 7, 8	0	BGA Heat Sink	23.5
Figures 10, 12	3.3, 5	Figures 7, 8	200	BGA Heat Sink	22
Figures 10, 12	3.3, 5	Figures 7, 8	400	BGA Heat Sink	22

Table 5. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 15	5	Figure 8	0	None	25
Figure 15	5	Figure 8	200	None	21
Figure 15	5	Figure 8	400	None	20
Figure 16	5	Figure 8	0	BGA Heat Sink	23.5
Figure 16	5	Figure 8	200	BGA Heat Sink	22
Figure 16	5	Figure 8	400	BGA Heat Sink	22

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Safety Considerations

The LTM4608 modules do not provide isolation from V_{IN} to V_{OUT} . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4608 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN} , GND and V_{OUT} . It helps to minimize the PCB conduction loss and thermal stress.

- Place high frequency ceramic input and output capacitors next to the V_{IN} , GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pads, unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.

Figure 17 gives a good example of the recommended layout.

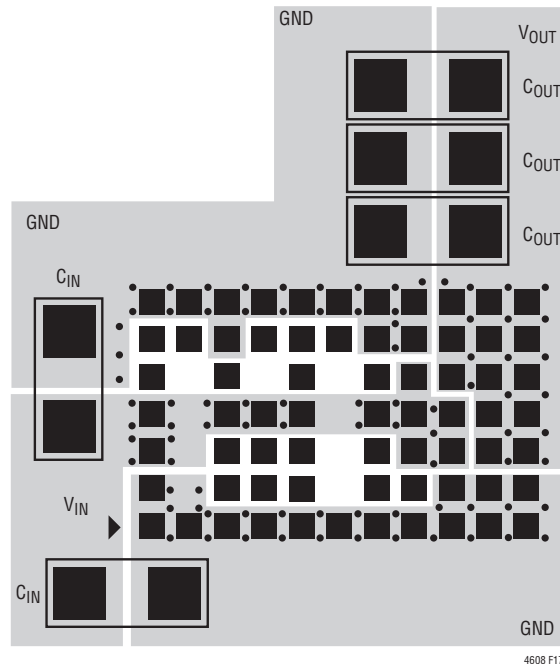


Figure 17. Recommended PCB Layout

For easier board layout and PCB assembly due to increased spacing between land grid pads, please refer to the LTM4608A.

TYPICAL APPLICATIONS

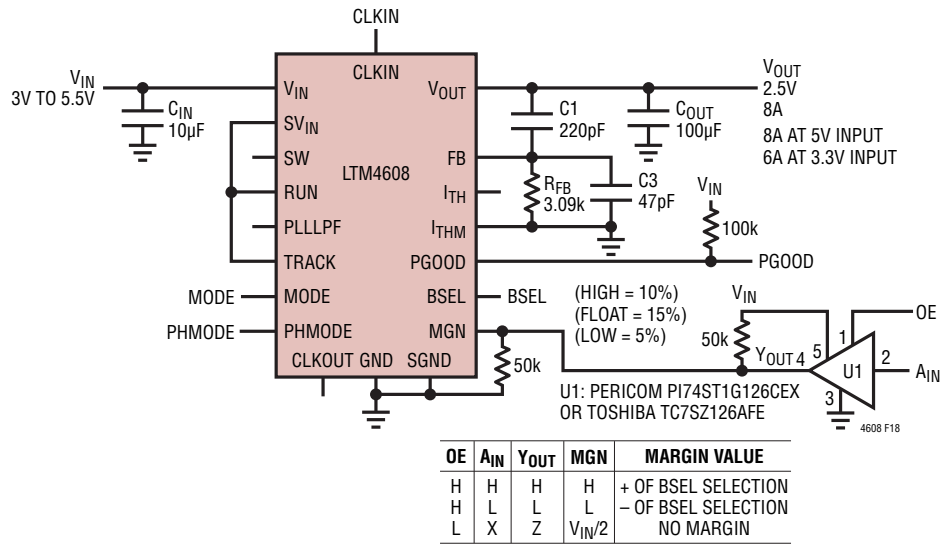


Figure 18. Typical 3V to 5.5V_{IN}, 2.5V at 8A Design

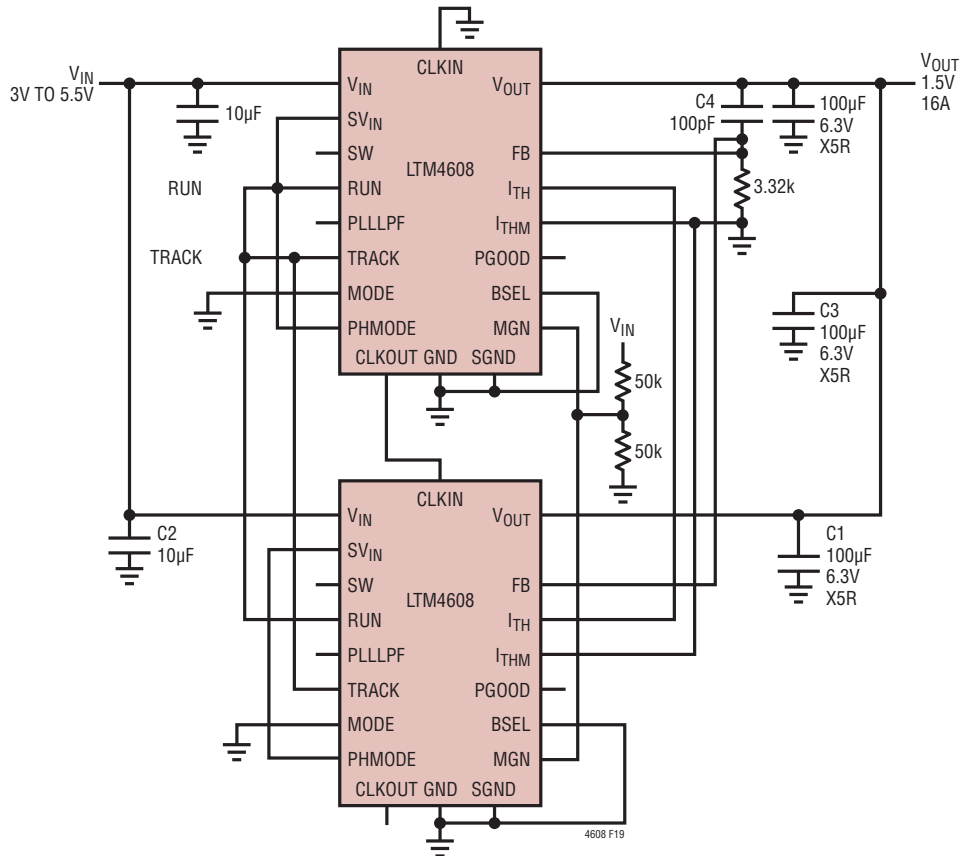


Figure 19. Two LTM4608s in Parallel, 1.5V at 16A Design.
See Also Dual 8A per Channel LTM4616

TYPICAL APPLICATIONS

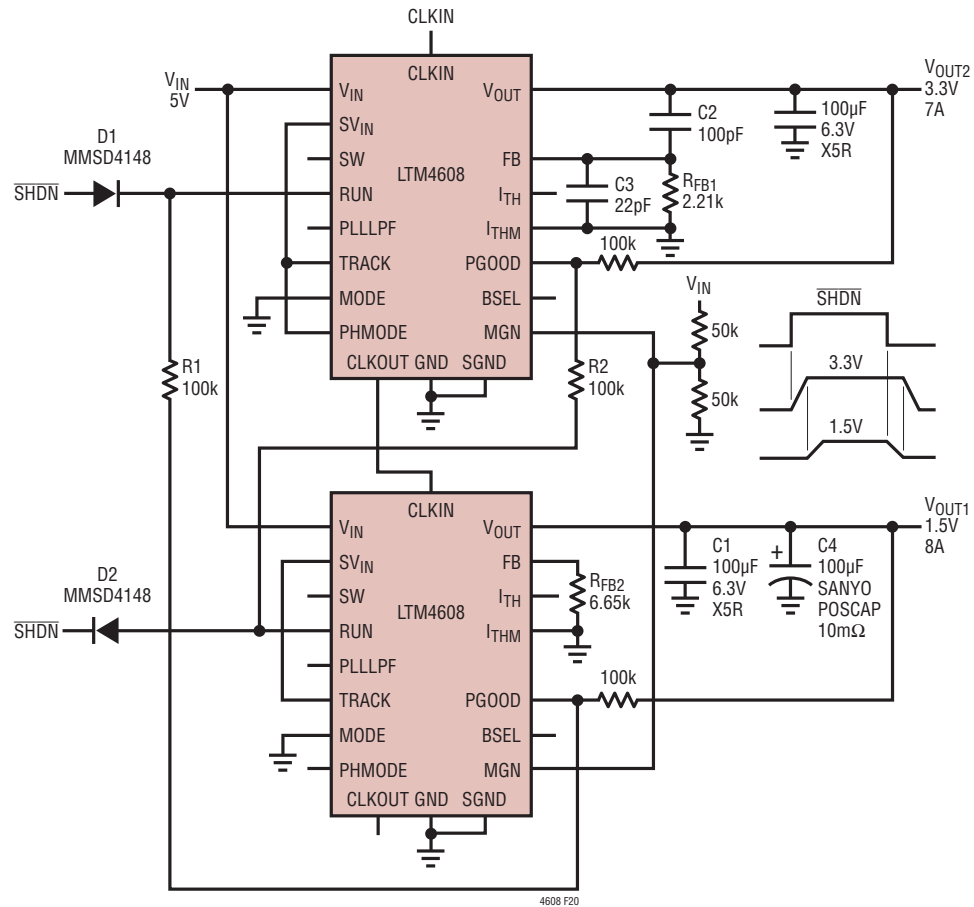


Figure 20. Dual LTM4608 Output Sequencing Application
See Also Dual 8A per Channel LTM4616

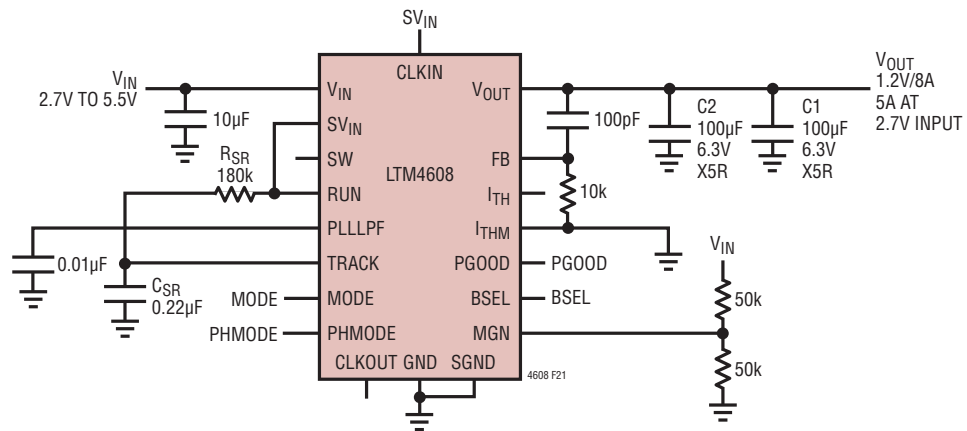


Figure 21. 2.7V to 5.5V_{IN}, 1.2V_{OUT} Design in Spread Spectrum Operation

TYPICAL APPLICATIONS

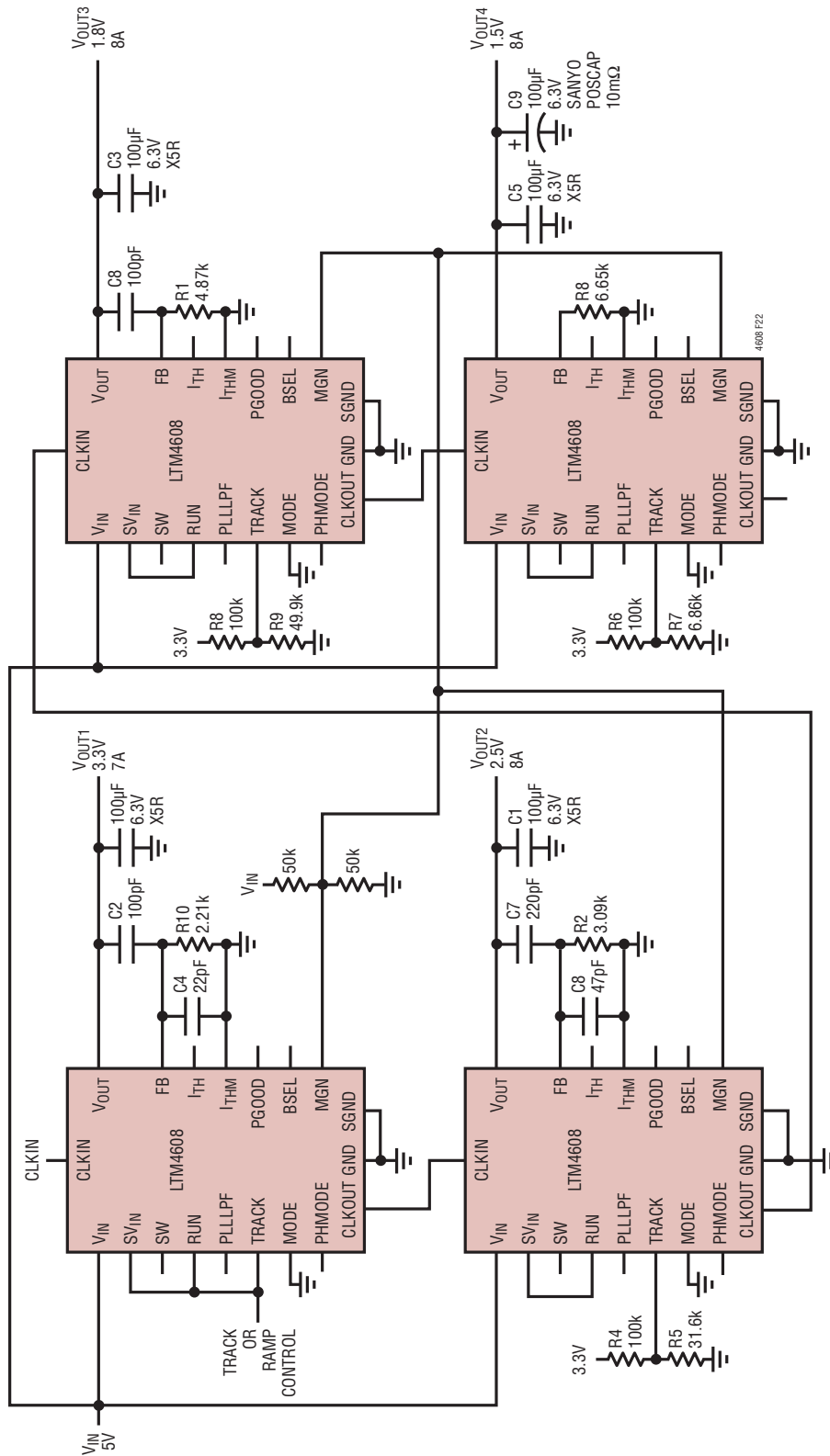
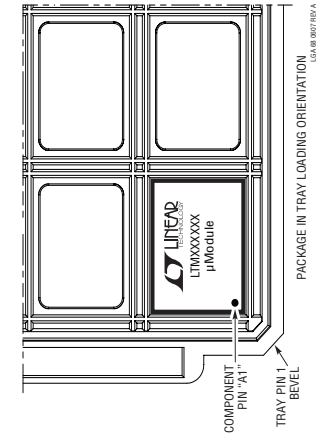
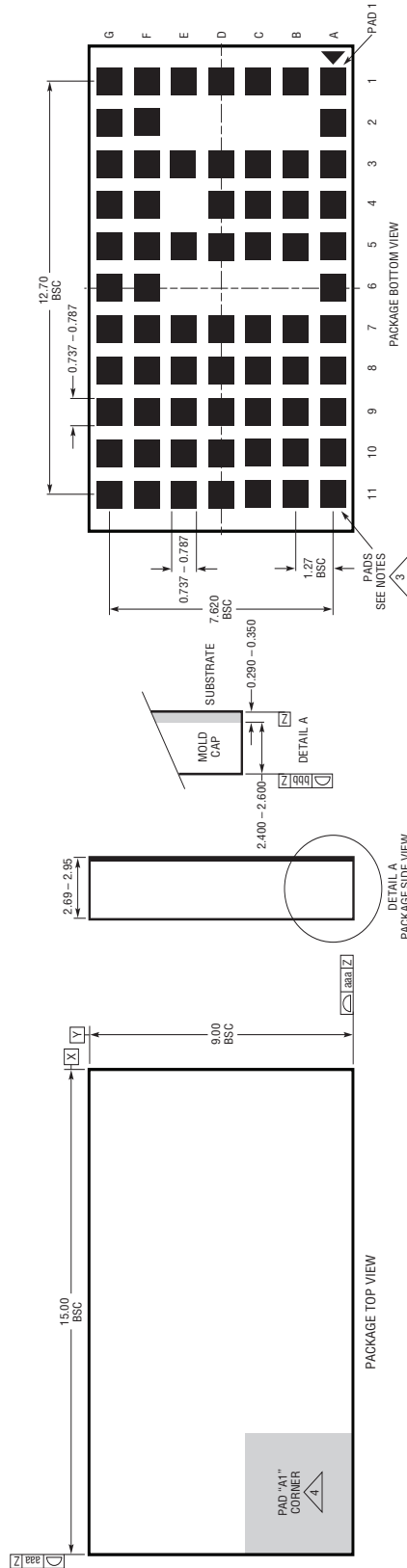


Figure 22. 4-Phase, Four Outputs (3.3V, 2.5V, 1.8V and 1.5V) with Tracking

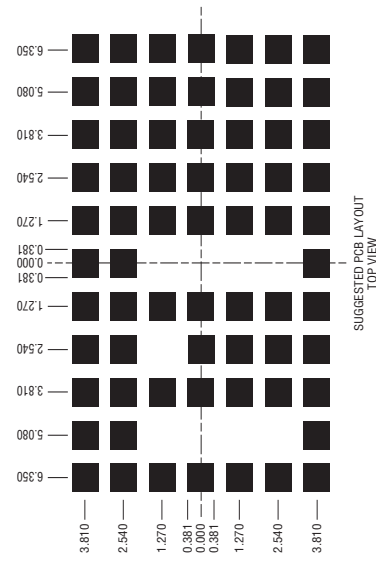
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

LGA Package
68-Lead (15mm × 9mm × 2.82mm)
 (Reference LTC DWG # 05-08-1808 Rev A)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. LAND DESIGNATION PER JEDEC MO-222
 4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR A MARKED FEATURE
 5. PRIMARY DATUM 'Z' IS SEATING PLANE
 6. THE TOTAL NUMBER OF PADS: 68
- | SYMBOL | TOLERANCE |
|--------|-----------|
| aaa | 0.15 |
| bbb | 0.10 |



REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	12/10	Voltage changed in the Typical Application drawing.	1
		Note added to the Absolute Maximum Ratings section.	2
		Note 2 added to the Electrical Characteristics section.	2, 3, 4
		Replaced graphs G05 and G06 in the Typical Performance Characteristics section.	5
		Updated MGN (B8) in the Pin Functions section.	7
		Changes made to Figure 1.	9
		Text changes made to the Applications Information section.	11, 14, 19
		Changes made to Figure 5.	15
		Note added to Figure 17.	20
		Changes made to Figures 18, 21, 22.	21, 22, 23
		Updated the Related Parts table.	26
C	3/11	Removed Pin Configuration drawing from Pin Functions	8
		Added value of 0.22 μ H to Inductor in Figure 1	9
		Updated Figure 3	13
D	3/12	Revised the Typical Application circuit.	1
		Changed the format of the Pin Assignment Table.	26

PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION
A1	GND	B1	GND	C1	V _{IN}	D1	V _{IN}	E1	SGND	F1	RUN	G1	GND
A2	GND	B2	–	C2	–	D2	–	E2	–	F2	CLKOUT	G2	GND
A3	GND	B3	CLKIN	C3	SW	D3	V _{IN}	E3	PLLLPF	F3	GND	G3	GND
A4	GND	B4	PHMODE	C4	SW	D4	V _{IN}	E4	–	F4	SV _{IN}	G4	GND
A5	GND	B5	MODE	C5	SW	D5	V _{IN}	E5	TRACK	F5	I _{THM}	G5	GND
A6	GND	B6	–	C6	–	D6	–	E6	–	F6	I _{TH}	G6	GND
A7	GND	B7	BSEL	C7	PGOOD	D7	V _{IN}	E7	FB	F7	GND	G7	GND
A8	GND	B8	MGN	C8	V _{IN}	D8	V _{IN}	E8	V _{IN}	F8	GND	G8	GND
A9	GND	B9	GND	C9	V _{IN}	D9	V _{IN}	E9	V _{OUT}	F9	V _{OUT}	G9	V _{OUT}
A10	GND	B10	GND	C10	V _{OUT}	D10	V _{OUT}	E10	V _{OUT}	F10	V _{OUT}	G10	V _{OUT}
A11	GND	B11	GND	C11	V _{OUT}	D11	V _{OUT}	E11	V _{OUT}	F11	V _{OUT}	G11	V _{OUT}

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Quad Supply Monitor with Adjustable Reset Timer	Monitors Four Supplies; Adjustable Reset Timer
LTC2923	Power Supply Tracking Controller	Tracks Both Up and Down; Power Supply Sequencing
LT3825/LT3837	Synchronous Isolated Flyback Controllers	No Optocoupler Required; 3.3V, 12A Output; Simple Design
LTM4616	Low V _{IN} Dual 8A DC/DC Step-Down μ Module Regulator	$2.7V \leq V_{IN} \leq 5.5V$, $0.6V \leq V_{OUT} \leq 5V$, 15mm \times 15mm \times 2.82mm LGA Package
LTM4628	Dual 8A, 26V, DC/DC Step-Down μ Module Regulator	$4.5V \leq V_{IN} \leq 26.5V$, $0.6V \leq V_{OUT} \leq 5.5V$, Remote Sense Amplifier, Internal Temperature Sensing Output, 15mm \times 15mm \times 4.32mm LGA Package
LTM4601/ LTM4601A	12A DC/DC μ Module Regulator with PLL, Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4601-1/LTM4601A-1 Version Has No Remote Sensing, LGA and BGA Packages
LTM4602	6A DC/DC μ Module Regulator	Pin Compatible with the LTM4600, LGA Package
LTM4618	6A DC/DC μ Module Regulator with PLL and Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation
LTM4604A	Low V _{IN} 4A DC/DC μ Module Regulator	$2.375V \leq V_{IN} \leq 5.5V$, $0.8V \leq V_{OUT} \leq 5V$, 9mm \times 15mm \times 2.32mm LGA Package

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