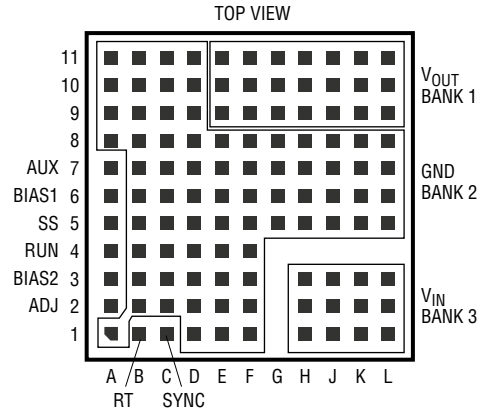
ABSOLUTE MAXIMUM RATINGS

(Note 1)

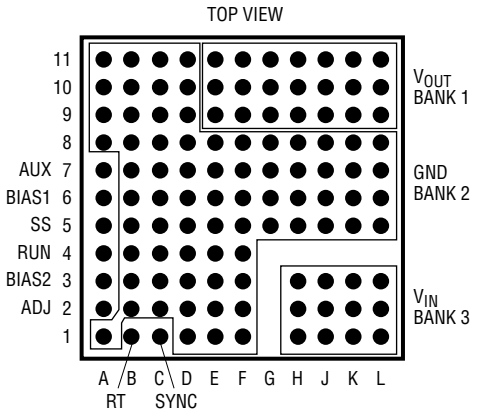
V_{IN} Voltage 65V
BIAS1 ..... 15V
BIAS2 ..... 24V
SYNC, ADJ, R_T, RUN, SS Voltages 5V
Current into RUN Pin (Note 2) 1mA
V_{OUT}, AUX 25V
Current Out of AUX 200mA
Internal Operating Temperature (Note 3)
E-, I-Grade ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
113-LEAD (15mm × 15mm × 4.32mm)

T_{JMAX} = 125°C, θ_{JA} = 12.2°C/W, $\theta_{JC(TOP)}$ = 9.3°C/W,
$\theta_{JC(BOTTOM)}$ = 3.6°C/W, θ_{JBOARD} = 7.54°C/W
θ VALUES DETERMINED PER JESD 51-9
WEIGHT = 2.6 GRAMS



BGA PACKAGE
113-LEAD (15mm × 15mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 12.2°C/W, $\theta_{JC(TOP)}$ = 9.3°C/W,
$\theta_{JC(BOTTOM)}$ = 3.6°C/W, θ_{JBOARD} = 7.54°C/W
θ VALUES DETERMINED PER JESD 51-9
WEIGHT = 2.6 GRAMS

ORDER INFORMATION

http://www.linear.com/product/LTM8027#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (See Note 3)
		DEVICE	FINISH CODE			
LTM8027EV#PBF	Au (RoHS)	LTM8027V	e4	LGA	3	–40°C to 125°C
LTM8027IV#PBF	Au (RoHS)	LTM8027V	e4	LGA	3	–40°C to 125°C
LTM8027MPV#PBF	Au (RoHS)	LTM8027V	e4	LGA	3	–55°C to 125°C
LTM8027EY#PBF	SAC305 (RoHS)	LTM8027Y	e1	BGA	3	–40°C to 125°C
LTM8027IY#PBF	SAC305 (RoHS)	LTM8027Y	e1	BGA	3	–40°C to 125°C
LTM8027IY	SnPb (63/37)	LTM8027Y	e0	BGA	3	–40°C to 125°C
LTM8027MPY#PBF	SAC305 (RoHS)	LTM8027Y	e1	BGA	3	–55°C to 125°C
LTM8027MPY	SnPb (63/37)	LTM8027Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, BIAS1 = BIAS2 = 10V, RUN = 2V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	(Note 5)	●	4.5		60	V
V_{OUT}	Maximum Output DC Voltage	0A < I_{OUT} ≤ 4A, V_{IN} = 48V			24		V
I_{OUT}	Output DC Current	V_{IN} ≤ 60V, V_{OUT} = 12V, (Note 4)		0		4	A
$V_{IN(START)}$	Minimum Start Voltage					7.5	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{OUT} = 12V, 15V< V_{IN} < 60V, I_{LOAD} = 4A			0.2		%
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	V_{OUT} = 12V, V_{IN} = 24V, 0A < I_{LOAD} ≤ 4A			0.2		%
$V_{UVLO(RISING)}$	Input Undervoltage Lockout Threshold (Rising)	(Note 5)			4.6		V
$V_{UVLO(FALLING)}$	Input Undervoltage Lockout Threshold (Falling)	(Note 5)			3.7		V
V_{ADJ}	ADJ Voltage		 ●	1.224 1.215		1.238 1.245	V V
$I_{Q(VIN)}$	Quiescent Current into IN	V_{BIAS} = V_{AUX}, V_{OUT} = 12VDC, No Load V_{RUN} = 0V			39 9		mA µA
V_{BIAS1}	BIAS1 Undervoltage Lockout (Rising) BIAS1 Undervoltage Lockout (Falling)				6.5 6		V V
I_{BIAS1}	Current into BIAS1	No Load RUN = 0V			25 25		mA µA
V_{BIAS2}	Minimum BIAS2 Voltage				3		V
I_{BIAS2}	Current Into BIAS2				1		µA
$V_{BIAS1(MINOV)}$	Minimum Voltage to Overdrive Internal Regulator ($INTV_{CC}$)				8.5		V
R_{FB}	Internal Feedback Resistor				499		kΩ
$V_{RUN(RISING)}$	RUN Enable Voltage (Rising)				1.4		V
$V_{RUN(FALLING)}$	RUN Enable Voltage (Falling)				1.2		V
f_{SW}	Switching Frequency	R_T = 187kΩ R_T = 23.7kΩ			100 500		kHz kHz
R_{SYNC}	SYNC Input Resistance				40		kΩ
$V_{SYNC(TH)}$	SYNC Voltage Threshold	f_{SYNC} = 350kHz	●	2.3			V
I_{SS}	Soft-Start Charging Current				2		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The RUN pin is internally clamped to 5V.

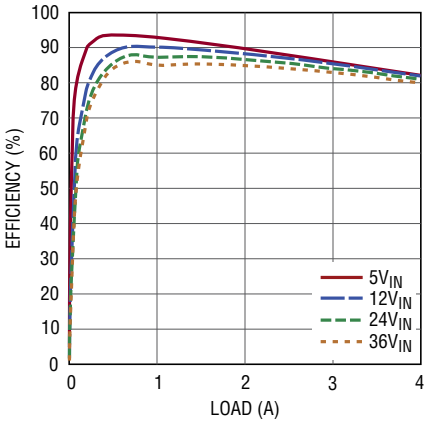
Note 3: The LTM8027E is guaranteed to meet performance specifications from 0°C to 125°C internal operating temperature. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8027I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8027MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 4: The maximum continuous output current may be derated by the LTM8027 junction temperature.

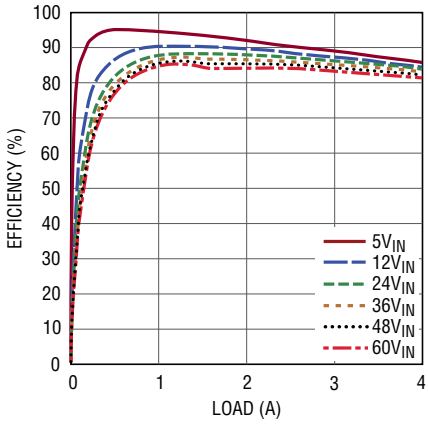
Note 5: V_{IN} voltages below the start-up threshold (7.5V) are only supported when BIAS1 is externally driven above 6.5V.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

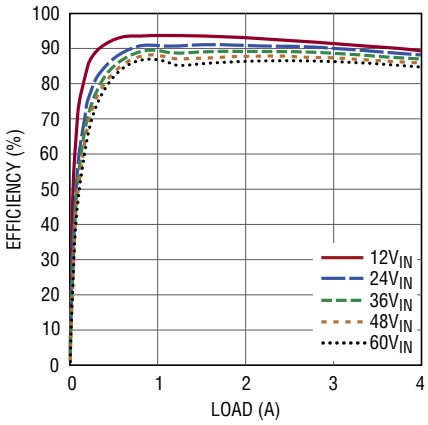
Efficiency vs Load, V_{OUT} = 2.5V



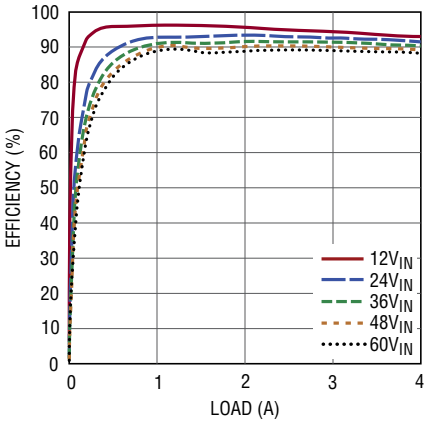
Efficiency vs Load, V_{OUT} = 3.3V



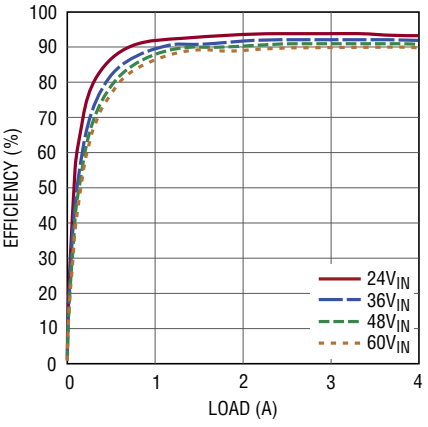
Efficiency vs Load, V_{OUT} = 5V



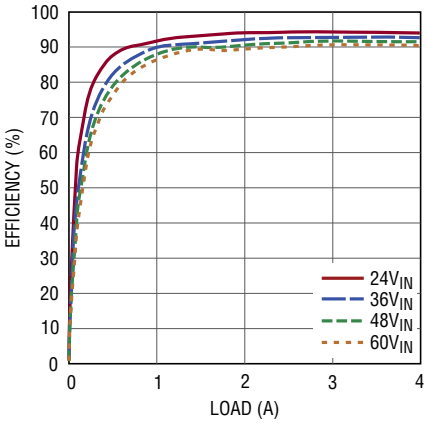
Efficiency vs Load, V_{OUT} = 8V



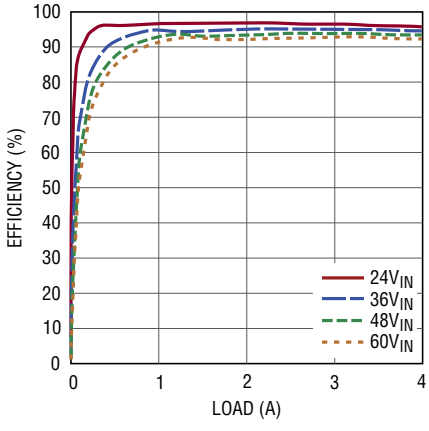
Efficiency vs Load, V_{OUT} = 12V



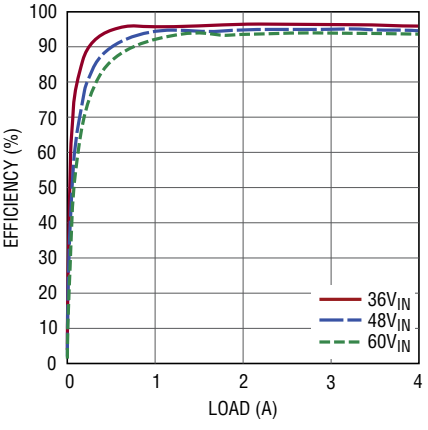
Efficiency vs Load, V_{OUT} = 15V



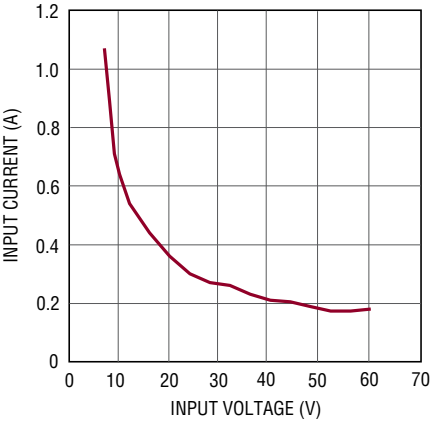
Efficiency vs Load, V_{OUT} = 18V



Efficiency vs Load, V_{OUT} = 24V

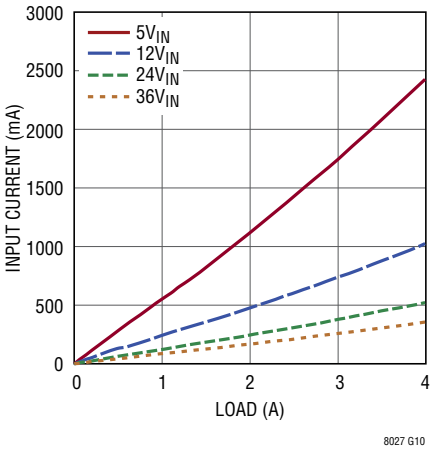


Input Current vs V_{IN} Output Shorted

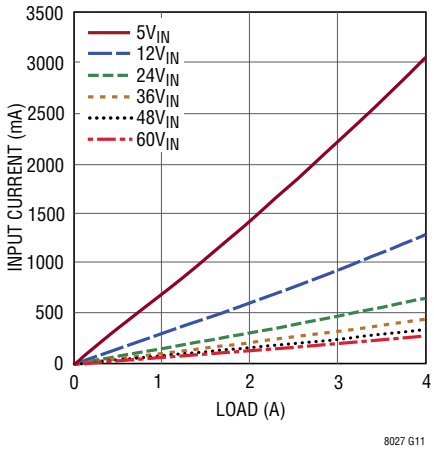


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

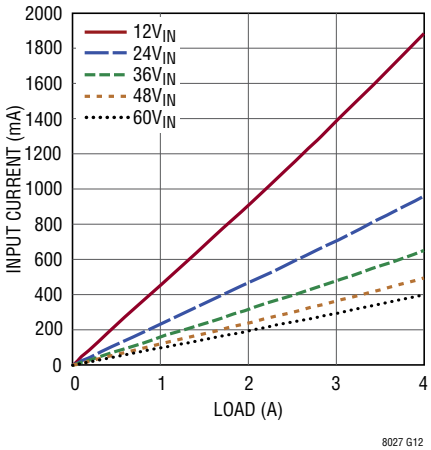
Input Current vs Load, V_{OUT} = 2.5V



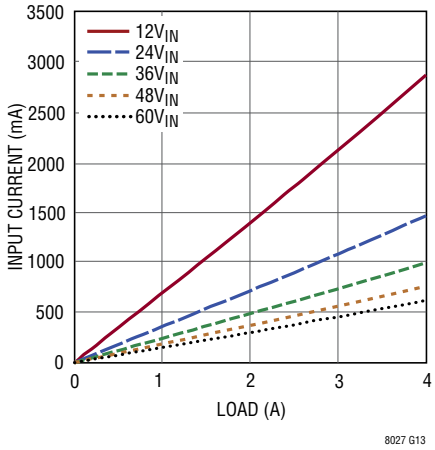
Input Current vs Load, V_{OUT} = 3.3V



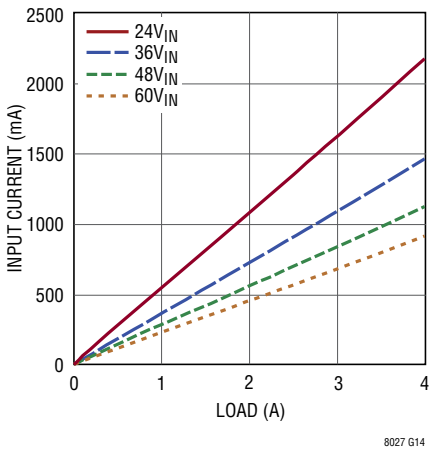
Input Current vs Load, V_{OUT} = 5V



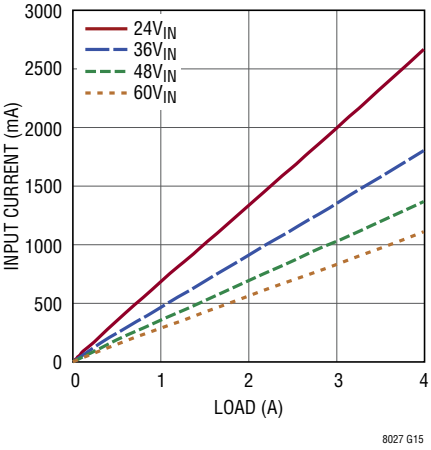
Input Current vs Load, V_{OUT} = 8V



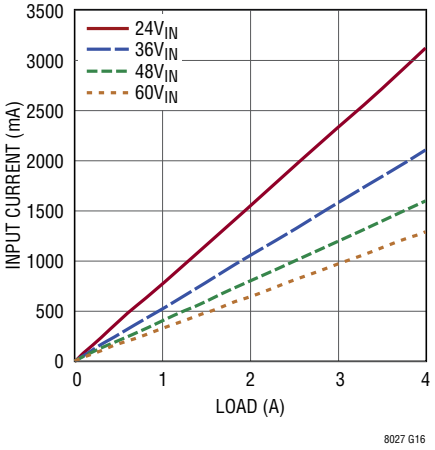
Input Current vs Load, V_{OUT} = 12V



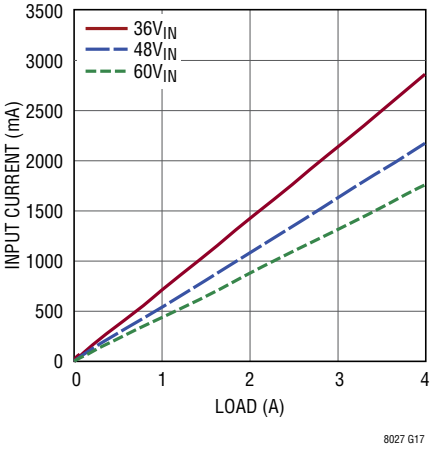
Input Current vs Load, V_{OUT} = 15V



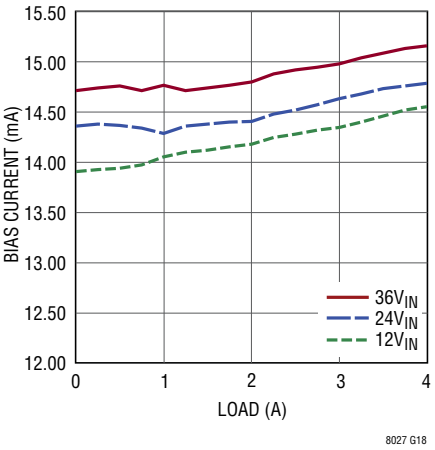
Input Current vs Load, V_{OUT} = 18V



Input Current vs Load, V_{OUT} = 24V

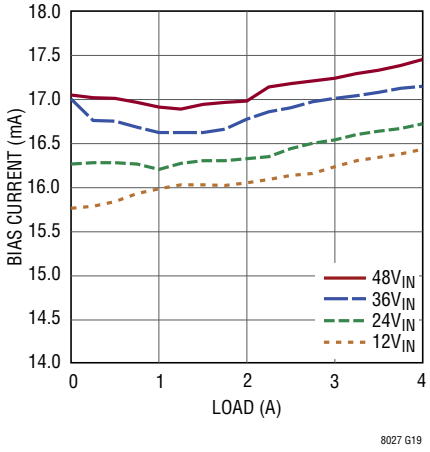


Bias Current vs Load, V_{OUT} = 2.5V

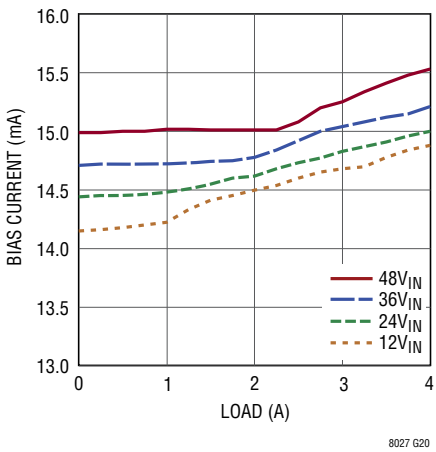


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

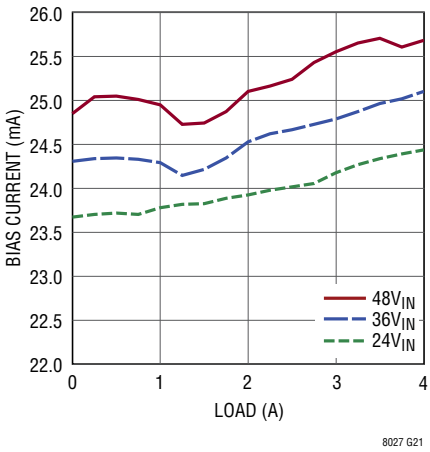
Bias Current vs Load, V_{OUT} = 3.3V



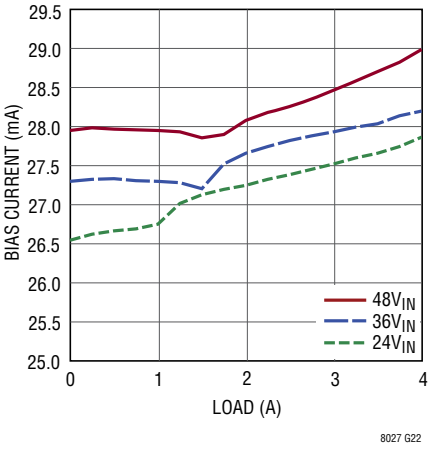
Bias Current vs Load, V_{OUT} = 5V



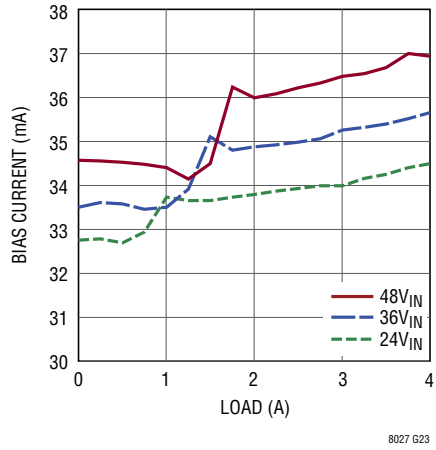
Bias Current vs Load, V_{OUT} = 8V



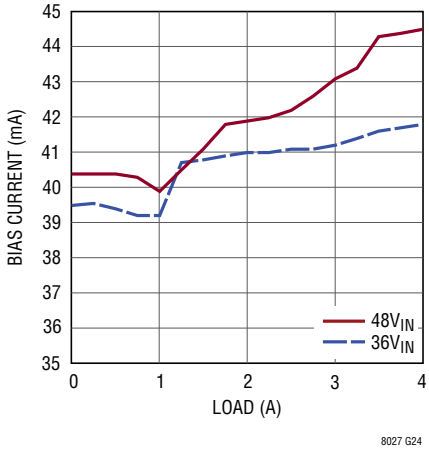
Bias Current vs Load, V_{OUT} = 12V



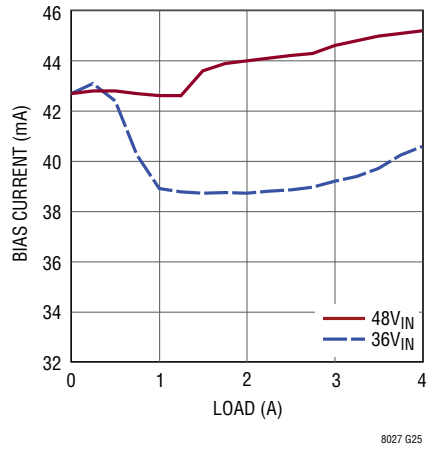
Bias Current vs Load, V_{OUT} = 15V



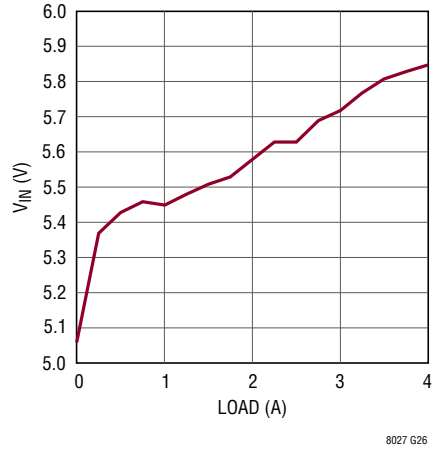
Bias Current vs Load, V_{OUT} = 18V



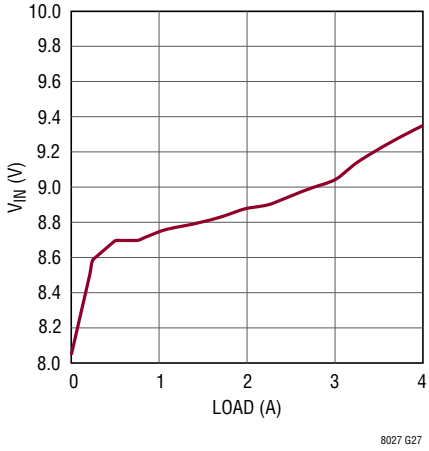
Bias Current vs Load, V_{OUT} = 24V



Minimum V_{IN} vs Load, V_{OUT} = 5V

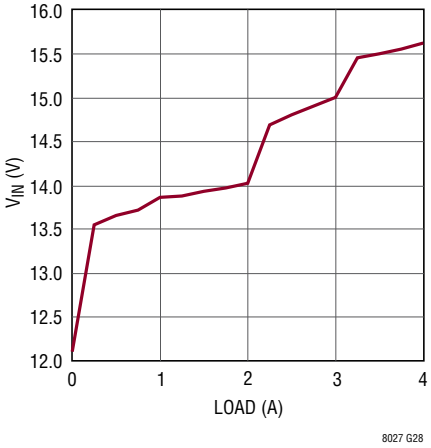


Minimum V_{IN} vs Load, V_{OUT} = 8V

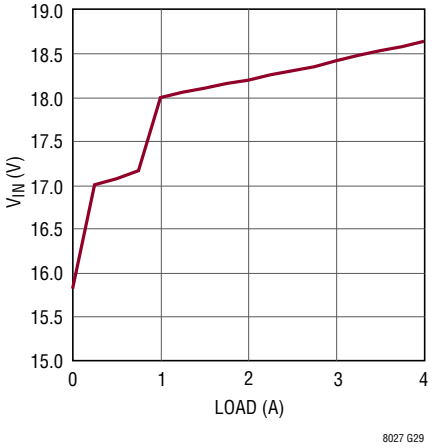


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

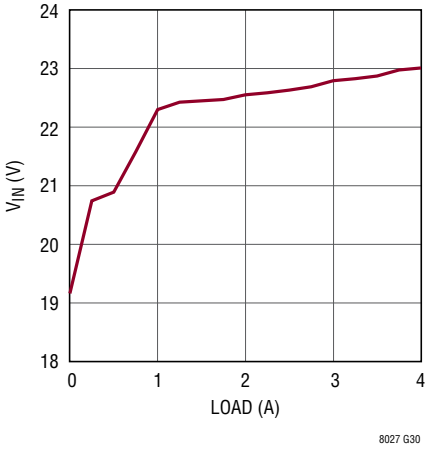
Minimum V_{IN} vs Load, V_{OUT} = 12V



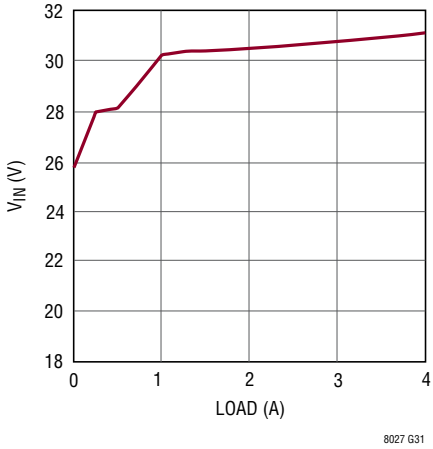
Minimum V_{IN} vs Load, V_{OUT} = 15V



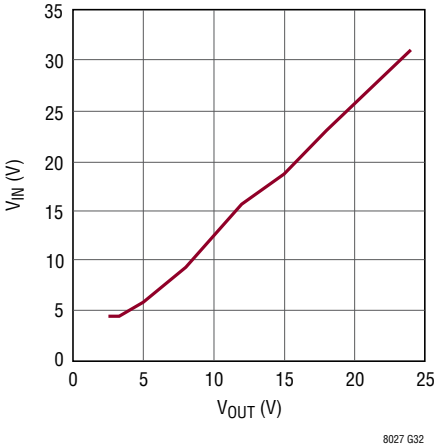
Minimum V_{IN} vs Load, V_{OUT} = 18V



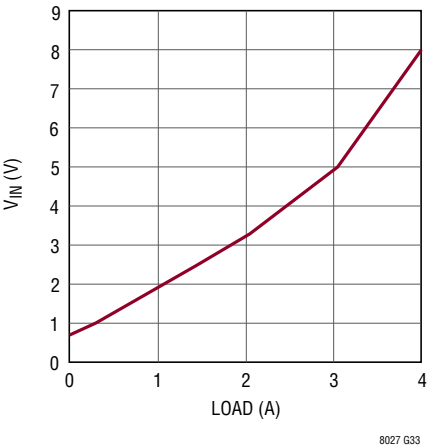
Minimum V_{IN} vs Load, V_{OUT} = 24V



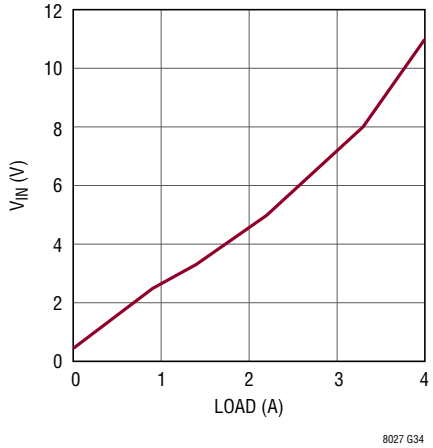
Minimum V_{IN} vs V_{OUT}, I_{OUT} = 4A



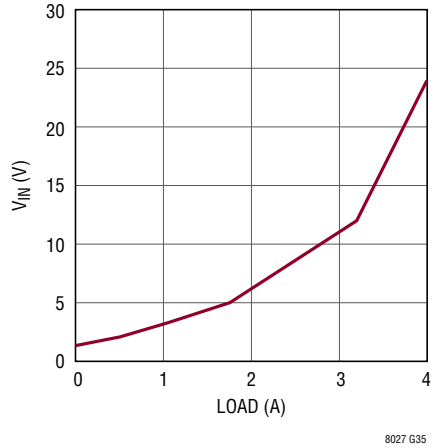
Minimum V_{IN} vs Load, V_{OUT} = –3.3V



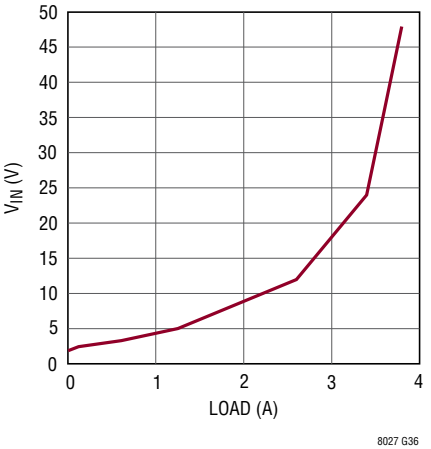
Minimum V_{IN} vs Load, V_{OUT} = –5V



Minimum V_{IN} vs Load, V_{OUT} = –8V

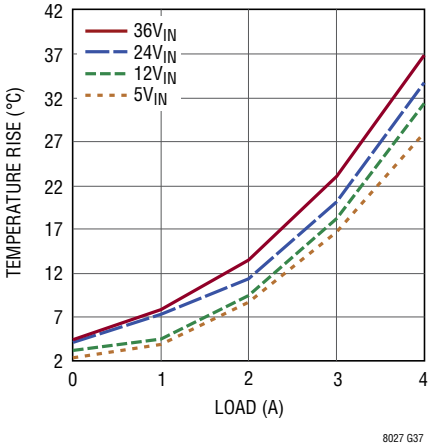


Minimum V_{IN} vs Load, V_{OUT} = –12V

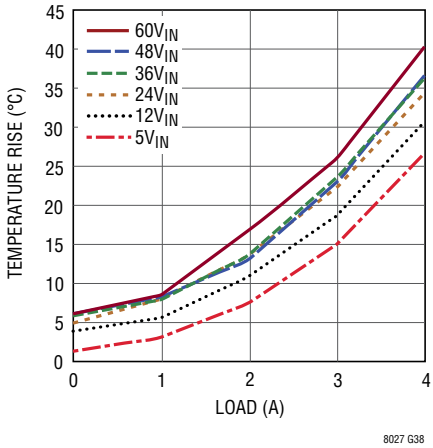


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

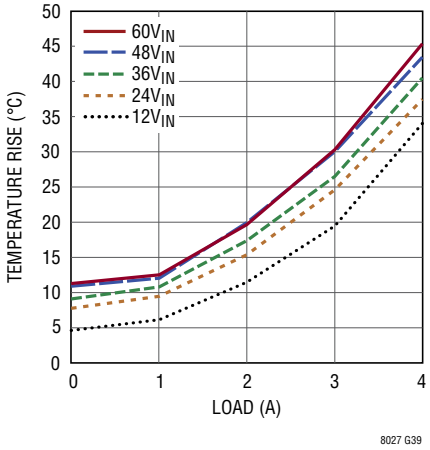
Temperature Rise vs Load, V_{OUT} = 2.5V



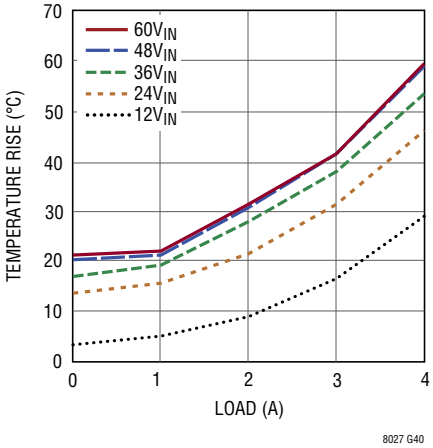
Temperature Rise vs Load, V_{OUT} = 3.3V



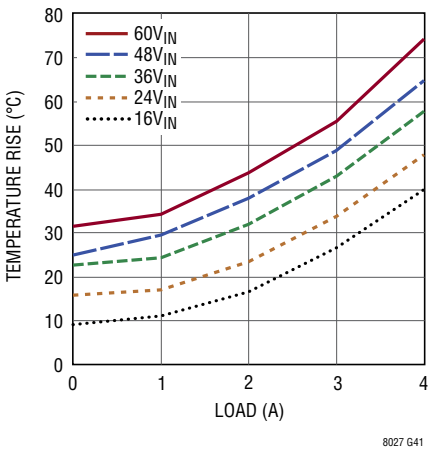
Temperature Rise vs Load, V_{OUT} = 5V



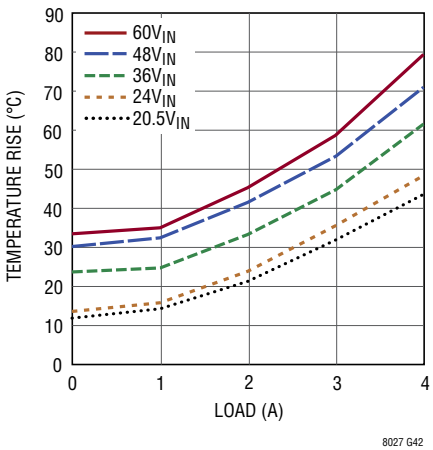
Temperature Rise vs Load, V_{OUT} = 8V



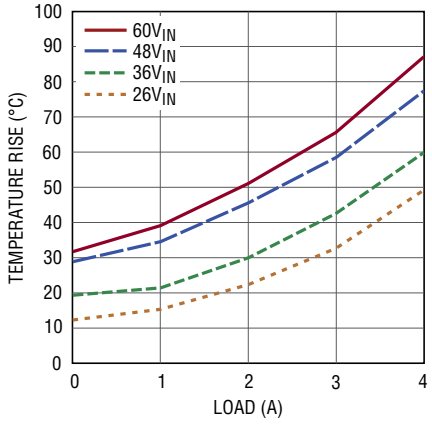
Temperature Rise vs Load, V_{OUT} = 12V



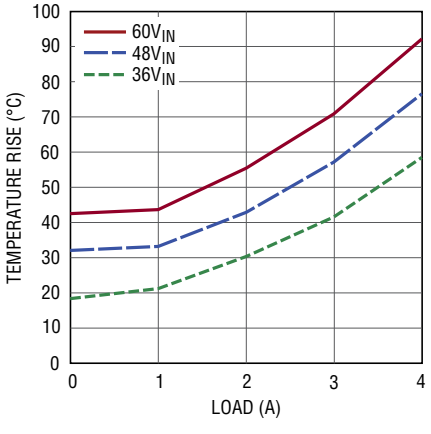
Temperature Rise vs Load, V_{OUT} = 15V



Temperature Rise vs Load, V_{OUT} = 18V



Temperature Rise vs Load, V_{OUT} = 24V



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (Bank 3): The V_{IN} pins supply current to the LTM8027's internal regulator and to the internal power switch. These pins must be locally bypassed with an external, low ESR capacitor (see Table 2).

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these and the GND pins.

AUX (Pin A7): Low Current Voltage Source for BIAS1 and BIAS2. In many designs, the BIAS pin is connected to V_{OUT} by way of the AUX pin. The AUX pin is internally connected to V_{OUT} and is placed near the BIAS pins to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, do NOT connect this pin to the load. If this pin is not tied to BIAS1 and BIAS2, leave it floating.

BIAS1 (Pin A6): The BIAS1 pin connects to the internal power bus. Connect to a power source greater than 8.5V. If the output is greater than 8.5V, connect it to this pin. If the output voltage is less, connect this to a voltage source between 8.5V and 15V.

BIAS2 (Pin A3): Internal Biasing Power. Connect to AUX (if 24V or less) or a voltage source above 3V. Do not leave BIAS2 floating.

RUN (Pin A4): Tie the RUN pin to ground to shut down the LTM8027. Tie to 1.4V or more for normal operation. The RUN pin is internally clamped to 5V, so when it is pulled up, be sure to use a pull-up resistor that limits the current into the RUN pin to less than 1mA. If the shutdown feature is not used, tie this pin to the V_{IN} pin through a pull-up resistor.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8027 and the circuit components.

RT (Pin B1): The RT pin is used to program the switching frequency of the LTM8027 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin.

SYNC (Pin C1): The SYNC pin provides an external clock input for synchronization of the internal oscillator. The R_T resistor should be set such that the internal oscillator frequency is 10% to 25% below the external clock frequency. This external clock frequency must be between 100kHz and 500kHz. If unused, tie the SYNC pin to GND. For more information see Oscillator Sync in the Application Information section of this data sheet.

ADJ (Pin A2): The LTM8027 regulates its ADJ pin to 1.23V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation:

$$R_{ADJ} = 613.77/(V_{OUT} – 1.23)$$

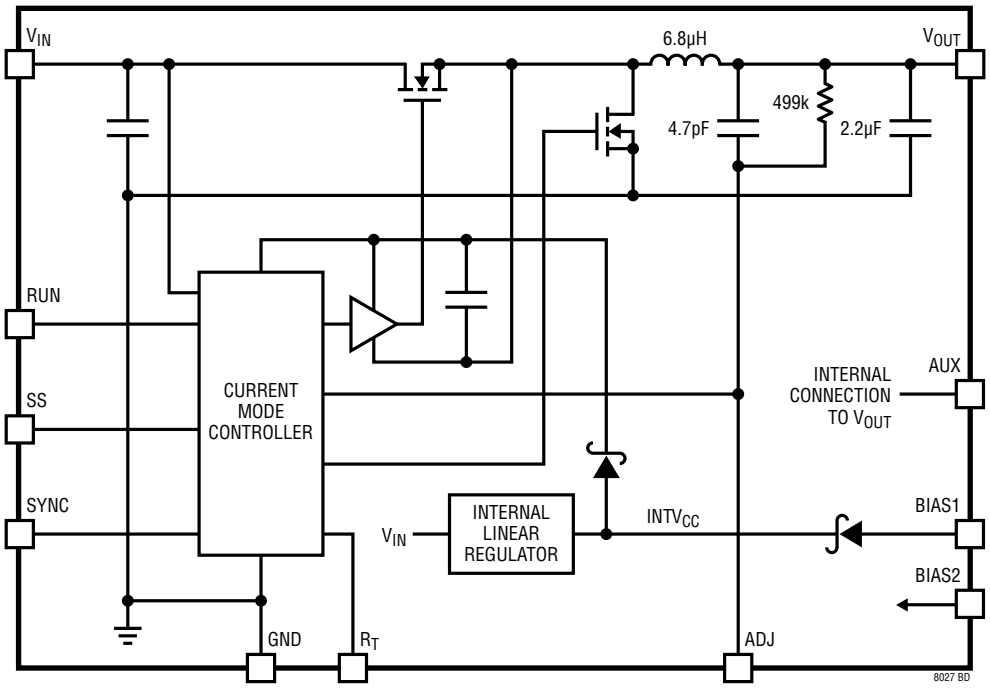
where R_{ADJ} is in kΩ.

SS (Pin A5): The soft-start pin is used to program the supply soft-start function. Use the following formula to calculate C_{SS} for a given output voltage slew rate:

$$C_{SS} = 2\mu A(t_{SS}/1.231V)$$

The pin should be left unconnected when not using the soft-start function.

BLOCK DIAGRAM



OPERATION

The LTM8027 is a standalone nonisolated step-down switching DC/DC power supply with an input voltage range of 4.5V to 60V that can deliver up to 4A of output current. This module provides a precisely regulated output voltage up to 24V, programmable via one external resistor. Given that the LTM8027 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified block diagram is given above. The LTM8027 contains a current mode controller, power switching element, power inductor, power MOSFETs and a modest amount of input and output capacitance.

The LTM8027 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor from the RT pin to GND.

A linear regulator provides internal power (shown as $INTV_{CC}$ on the Block Diagram) to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS1 pin is connected to an external voltage higher than 8.5V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN pin is used to enable or place the LTM8027 in shutdown, disconnecting the output and reducing the input current to less than 9µA.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 2 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{ADJ} and R_T values.
3. Connect the BIAS pins as indicated.

While these component and connection combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 2 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 2 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8027. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8027 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Input Power Requirements

The LTM8027 is biased using an internal linear regulator to generate operational voltages from the V_{IN} pin. Virtually all of the circuitry in the LTM8027 is biased via this internal linear regulator output ($INTV_{CC}$ on the Block Diagram). This pin is internally decoupled with a low ESR capacitor to GND. The $INTV_{CC}$ regulator generates an 8V output provided there is ample voltage on the V_{IN} pin. The $INTV_{CC}$ regulator has approximately 1V of dropout, and will follow the V_{IN} pin with voltages below the dropout threshold.

The LTM8027 has a typical start-up requirement of V_{IN} > 7.5V. This assures that the onboard regulator has ample headroom to bring the internal regulator ($INTV_{CC}$) above its UVLO threshold. The $INTV_{CC}$ regulator can only source current, so forcing the BIAS1 pin above 8.5V allows use of externally derived power for the IC. This effectively shuts down the internal linear regulator and reduces power dissipation within the LTM8027. Using the onboard regulator for start-up, then applying power to BIAS1 from the converter output or external supply maximizes conversion efficiencies and is a common practice. If BIAS1 is maintained above 6.5V using an external source, the LTM8027 can continue to operate with V_{IN} as low as 4.5V.

BIAS Power

The internal circuitry of the LTM8027 is powered by the $INTV_{CC}$ bus, which is derived either from the afore mentioned internal linear regulator or the BIAS1 pin, if it is greater than 8.5V. Since the internal linear regulator is by nature dissipative, deriving $INTV_{CC}$ from an external source through the BIAS pins reduces the power lost within the LTM8027 and can increase overall system efficiency.

APPLICATIONS INFORMATION

For example, suppose the LTM8027 needs to provide 5V from an input voltage source that is nominally 12V. From Table 2, the recommended R_T value is 75k, which corresponds to an operating frequency of 210kHz. From the graphs in the Typical Performance Characteristics, the typical internal regulator ($INTV_{CC}$) current at $12V_{IN}$ and 210kHz is 15mA. The power dissipated by the internal linear regulator at $12V_{IN}$ is given by the equation:

$$P_{INTVCC} = (V_{IN} - 8) \bullet I_{INTVCC}$$

or only 60mW. This has a small but probably acceptable effect on the operating temperature of the LTM8027.

If the input rises to 60V, however, the power dissipation is a lot higher, over 780mW. This can cause unnecessarily high junction temperatures if the $INTV_{CC}$ regulator must dissipate this amount of power for very long.

Connect BIAS2 to AUX (if 24V or less) or a voltage source above 3V.

Soft-Start

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor connected from the SS pin to GND programs the slew rate. The capacitor is charged from an internal 2µA current source producing a ramped voltage that overrides the command reference to the controller, resulting in a smooth output voltage ramp. The soft-start circuit is disabled once the SS pin voltage has been charged to 200mV above the internal reference of 1.231V.

During a V_{IN} UVLO, RUN event, or undervoltage on internal bias, the SS pin voltage is discharged with a 50µA current. Therefore, the value of the SS capacitor determines how long one of these events must be in order to completely discharge the soft-start capacitor. In the case of an output overload or short circuit, the SS pin voltage is clamped to a diode drop above the ADJ pin. Once the short has been removed the V_{ADJ} pin voltage starts to recover. The soft-start circuit takes control of the output voltage slew rate once the V_{ADJ} pin voltage has exceeded the slowly ramping SS pin voltage, reducing the output voltage overshoot during a short-circuit recovery.

The desired soft-start time (t_{SS}) is programmed via the C_{SS} capacitor as follows:

$$C_{SS} = \frac{2\mu A \bullet t_{SS}}{1.231V}$$

The amount of time in which the power supply must be under a V_{IN}, internal regulator ($INTV_{CC}$) or V_{SHDN} UVLO fault condition (t_{FAULT}) before the SS pin voltage enters its active region is approximated by the following formula:

$$t_{FAULT} = \frac{C_{SS} \bullet 0.65V}{50\mu A}$$

Operating Frequency Trade-offs

The LTM8027 uses a constant frequency architecture that can be programmed over a 100kHz to 500kHz range with a single resistor from the RT pin to ground. The nominal voltage on the RT pin is 1V and the current that flows from this pin is used to charge an internal oscillator capacitor. The value of R_T for a given operating frequency can be chosen from Figure 1 or Table 1.

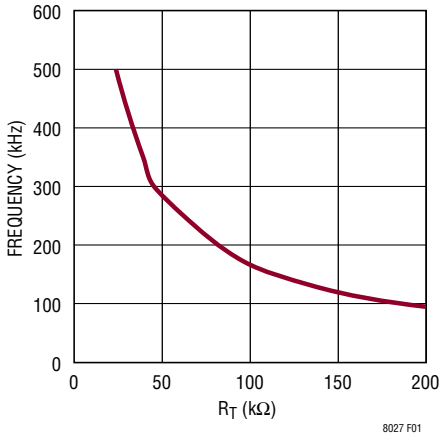


Figure 1. Timing Resistor (R_T) Value

APPLICATIONS INFORMATION

Table 1 lists typical resistor values for common operating frequencies.

Table 1. R_T Resistor Values vs Frequency

R_T (kΩ)	f_{SW} (kHz)
187	100
118	150
82.5	200
63.4k	250
48.7k	300
40.2k	350
31.6k	400
27.4k	450
23.7k	500

It is recommended that the user apply the R_T value given in Table 2 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8027 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can damage the LTM8027 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

The maximum frequency (f_{MAX}) at which the LTM8027 should be allowed to switch and the minimum frequency set resistor value that should be used for a given set of input and output operating condition is given in Table 2 as $R_{T(MIN)}$. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Output Voltage Programming

The LTM8027 regulates its ADJ pin to 1.23V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation $R_{ADJ} = 613.77/(V_{OUT} – 1.23)$, where R_{ADJ} is in kΩ.

RUN Control

The LTM8027 RUN pin uses a reference threshold of 1.4V. This precision threshold allows use of the RUN pin for both logic-level controlled applications and analog monitoring applications such as power supply sequencing. The LTM8027 operational status is primarily controlled by a UVLO circuit on internal power source. When the LTM8027 is enabled via the RUN pin, only the internal regulator ($INTV_{CC}$) is enabled. Switching remains disabled until the UVLO threshold is achieved at the BIAS1 pin, when the remainder of the LTM8027 is enabled and switching commences.

Because the LTM8027 high power converter is a power transfer device, a voltage that is lower than expected on the input supply could require currents that exceed the sourcing capabilities of that supply, causing the system to lock up in an undervoltage state. Input supply start-up protection can be achieved by enabling the RUN pin using a resistive divider from the V_{IN} supply to ground. Setting the divider output to 1.4V when that supply is at an adequate voltage prevents an LTM8027 converter from drawing large currents until the input supply is able to provide the required power. 200mV of input hysteresis on the RUN pin allows for about 15% of input supply droop before disabling the converter.

Input UVLO and RUN

The RUN pin has a precision voltage threshold with hysteresis which can be used as an undervoltage lockout threshold (UVLO) for the power supply. Undervoltage lockout keeps the LTM8027 in shutdown until the supply input voltage is above a certain voltage programmed by the user. The hysteresis voltage prevents noise from falsely tripping UVLO. Resistors are chosen by first selecting R_B (refer to Figure 2). Then:

$$R_A = R_B \bullet \left(\frac{V_{IN(ON)}}{1.4V} - 1 \right)$$

where $V_{IN(ON)}$ is the input voltage at which the undervoltage lockout is disabled and the supply turns on.

APPLICATIONS INFORMATION

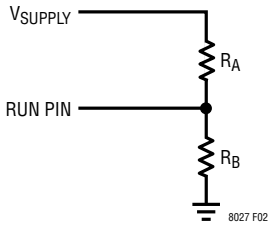


Figure 2. Undervoltage Lockout Resistive Divider

Example: Select R_B = 49.9k, $V_{IN(ON)}$ = 14.5V (based upon a 15V minimum input voltage)

$$R_A = 49.9k \bullet \left(\frac{14.5V}{1.4V} - 1\right) = 464k$$

The V_{IN} turn off voltage is 15% below turn on. In the example the $V_{IN(OFF)}$ would be 12.3V. The shutdown function can be disabled by connecting the RUN pin to the V_{IN} pin through a large value pull-up resistor, (R_{PU}). This pin contains a low impedance clamp at 6V, so the RUN pin will sink current from the R_{PU} pull-up resistor:

$$I_{RUN} = \frac{V_{IN} - 6V}{R_{PU}}$$

Because this arrangement will clamp the RUN pin to 6V, it will violate the 5V absolute maximum voltage rating of the pin. This is permitted, however, as long as the absolute maximum input current rating of 1mA is not exceeded. Input RUN pin currents of <100µA are recommended: a 1M or greater pull-up resistor is typically used for this configuration.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8027. However, these capacitors can cause problems if the LTM8027 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an under damped tank circuit, and the voltage at the V_{IN} pin of the LTM8027 can ring to twice the nominal input voltage, possibly exceeding the LTM8027's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8027 into an energized supply, the input network should be designed to prevent this overshoot by introducing a damping element into the path of current flow. This is often done by adding an inexpensive electrolytic bulk capacitor across the input terminals of the LTM8027. The criteria for selecting this capacitor is that the ESR is high enough to damp the ringing, and the capacitance value is several times larger than the LTM8027 ceramic input capacitor. The bulk capacitor does not need to be located physically close to the LTM8027; it should be located close to the application board's input connector instead.

Synchronization

The oscillator can be synchronized to an external clock. Choose the R_T resistor such that the resultant frequency is at least 10% below the desired synchronization frequency. It is recommended that the SYNC pin be driven with a square wave that has amplitude greater than 2.3V, pulse width greater than 1µs and rise time less than 500ns. The rising edge of the sync wave form triggers the discharge of the internal oscillator capacitor.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8027. The LTM8027 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout.

APPLICATIONS INFORMATION

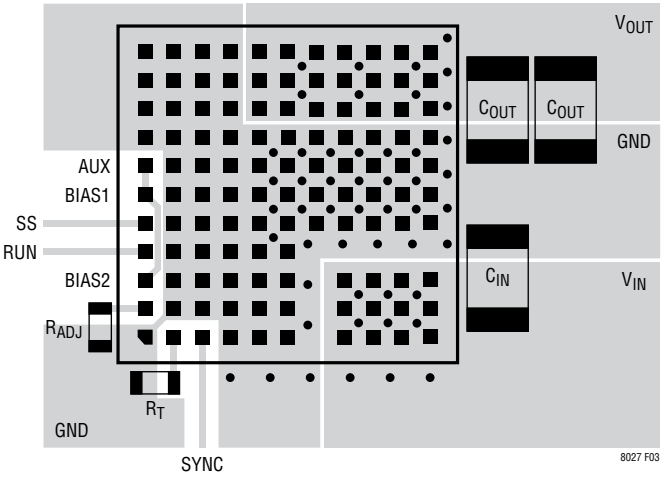


Figure 3. Suggested Layout

Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the R_{ADJ} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8027.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8027.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM8027.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8027.

Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8027 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

Thermal Considerations

The LTM8027 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8027 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

APPLICATIONS INFORMATION

The junction-to-air and junction-to-board thermal resistances given in the Pin Configuration diagram may also be used to estimate the LTM8027 internal temperature. These thermal coefficients are determined per JESD 51-9 (JEDEC standard, test boards for area array surface mount package thermal measurements) through analysis and physical correlation. Bear in mind that the actual thermal resistance of the LTM8027 to the printed circuit board depends upon the design of the circuit board.

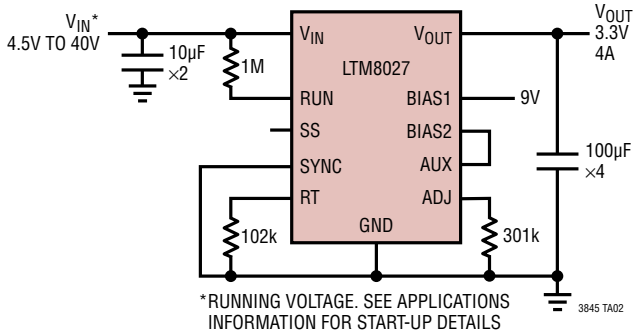
The die temperature of the LTM8027 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8027. The bulk of the heat flow out of the LTM8027 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

Table 2. Recommended Component Values and Configuration
(T_A = 25°C. See Typical Performance Characteristics for load Conditions)

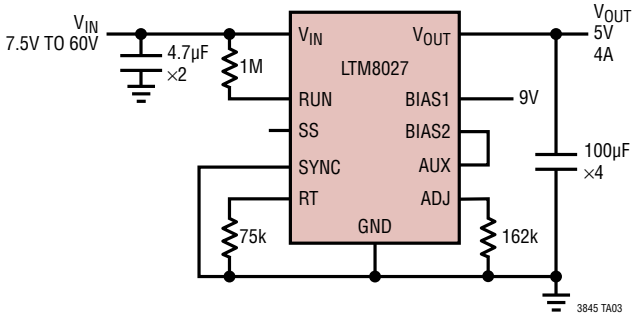
V_{IN} RANGE (V)	V_{OUT} (V)	C_{IN}	C_{OUT}	BIAS1	R_{ADJ} (kΩ)	$f_{OPTIMAL}$ (kHz)	$R_{OPTIMAL}$ (kΩ)	f_{MAX} (kHz)	R_{MAX} (kΩ)
4.5 to 60	3.3	2 × 4.7µF 2220 100V	5 × 100µF 1812 6.3V	8.5V to 15V	301	115	154	160	107
7.5 to 60	5	2 × 4.7µF 2220 100V	4 × 100µF 1210 6.3V	8.5V to 15V	162	210	75.0	230	68.2
10.5 to 60	8	2 × 4.7µF 2220 100V	4 × 47µF 1210 10V	8.5V to 15V	90.9	260	59.0	350	40.2
16 to 60	12	2 × 4.7µF 2220 100V	4 × 22µF 1210 16V	AUX	56.2	300	48.7	500	23.7
20.5 to 60	15	2 × 4.7µF 2220 100V	4 × 22µF 1210 16V	AUX	44.2	350	40.2	500	23.7
26 to 60	18	2 × 4.7µF 2220 100V	4 × 10µF 1812 25V	8.5V to 15V	36.5	400	31.6	500	23.7
34 to 60	24	2 × 4.7µF 2220 100V	4 × 10µF 1812 25V	8.5V to 15V	26.7	430	28.7	500	23.7
4.5 to 40	2.5	2 × 10µF 2220 50V	5 × 100µF 1812 6.3V	8.5V to 15V	487	145	124	185	88.7
4.5 to 40	3.3	2 × 10µF 2220 50V	4 × 100µF 1812 6.3V	8.5V to 15V	301	165	102	240	64.9
7.5 to 40	5	2 × 10µF 2220 50V	4 × 100µF 1210 6.3V	8.5V to 15V	162	210	75.0	315	45.3
10.5 to 40	8	2 × 10µF 2220 50V	4 × 47µF 1210 10V	8.5V to 15V	90.9	260	59.0	500	23.7
16 to 40	12	2 × 10µF 2220 50V	4 × 22µF 1210 16V	AUX	56.2	300	48.7	500	23.7
20.5 to 40	15	1 × 10µF 2220 50V	4 × 22µF 1210 16V	AUX	44.2	350	40.2	500	23.7
26 to 40	18	1 × 10µF 2220 50V	4 × 10µF 1812 25V	8.5V to 15V	36.5	400	31.6	500	23.7
34 to 40	24	1 × 10µF 2220 50V	4 × 10µF 1812 25V	8.5V to 15V	26.7	430	28.7	500	23.7
4.5 to 56	–3.3	2 × 4.7µF 2220 100V	5 × 100µF 1812 6.3V	8.5V to 15V Above Output	301	115	154	155	115
4.5 to 55	–5	2 × 4.7µF 2220 100V	4 × 100µF 1210 6.3V	8.5V to 15V Above Output	162	190	90.9	230	68.2
10.5 to 52	–8	2 × 4.7µF 2220 100V	4 × 47µF 1210 10V	8.5V to 15V Above Output	90.9	260	59.0	350	40.2
16 to 48	–12	2 × 4.7µF 2220 100V	4 × 22µF 1210 16V	AUX	56.2	300	48.7	500	23.7

TYPICAL APPLICATIONS

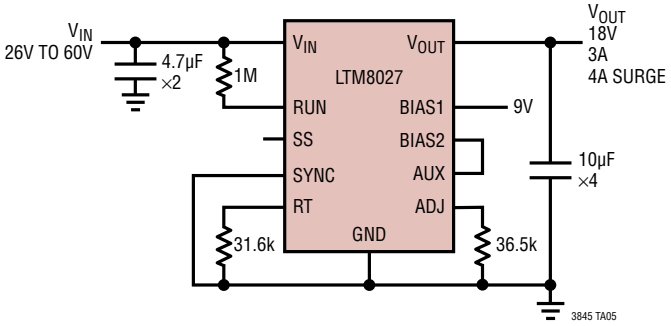
3.3V V_{OUT} Step-Down Converter



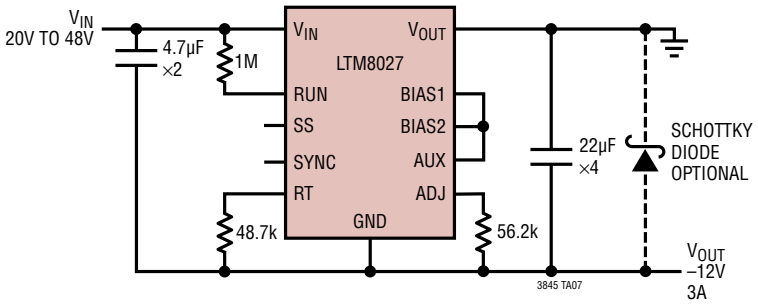
5V V_{OUT} Step-Down Converter



18V V_{OUT} Step-Down Converter

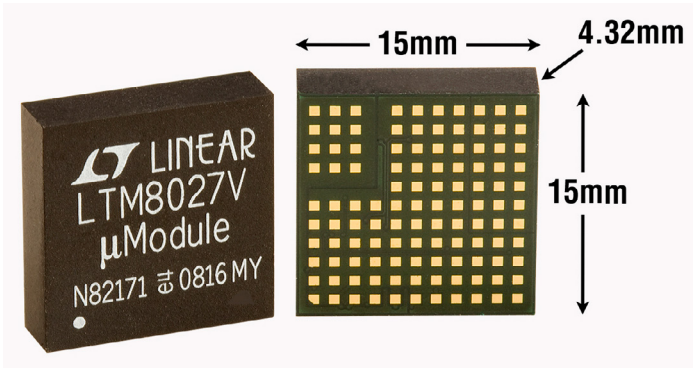


–12V V_{OUT} Positive-to-Negative Converter

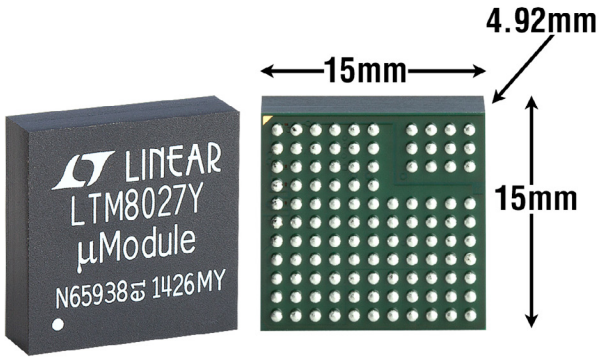


PACKAGE PHOTOGRAPHS

LGA



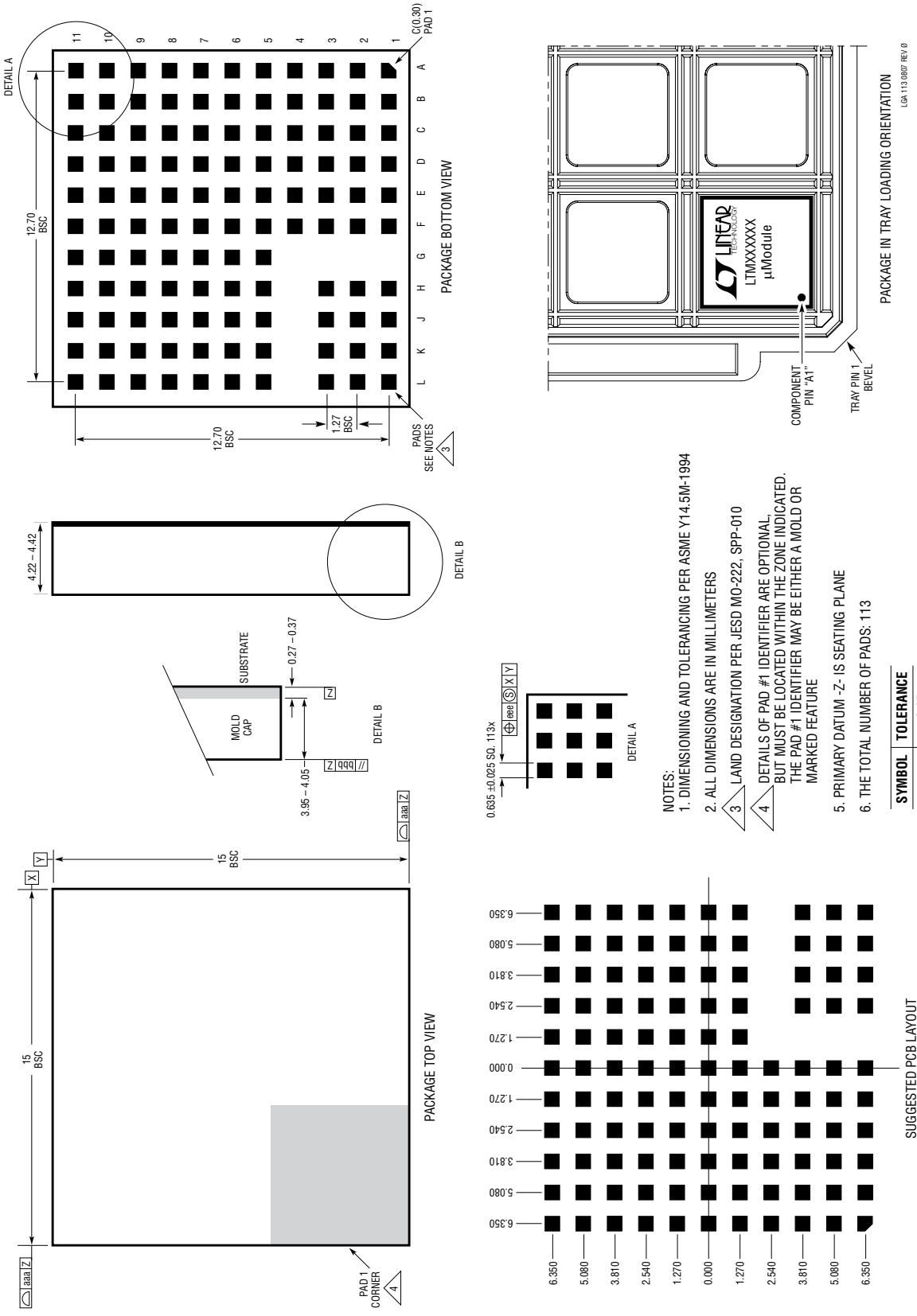
BGA



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM8027#packaging for the most recent package drawings.

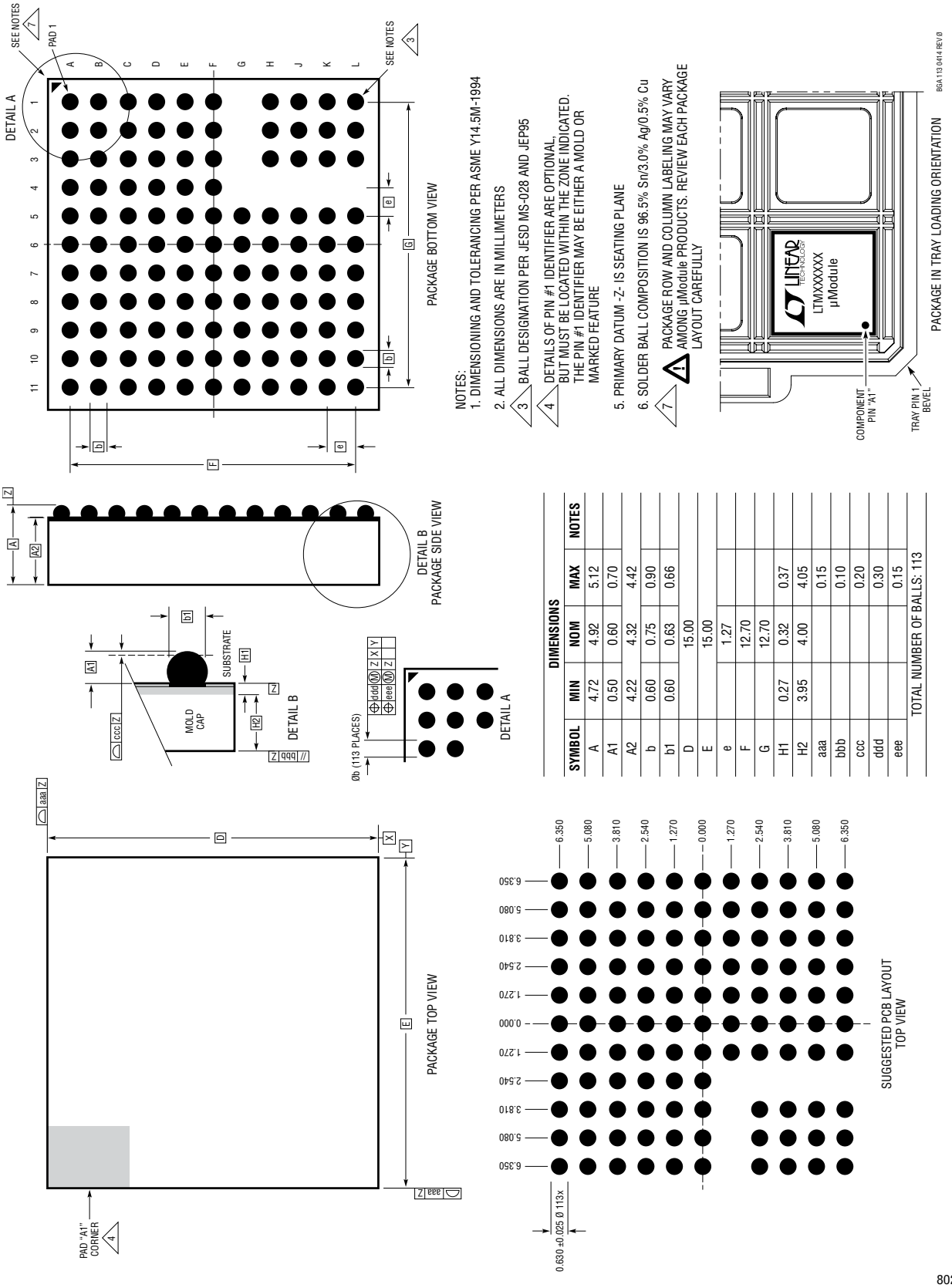
LGA Package
113-Lead (15mm × 15mm × 4.32mm)
(Reference LTC DWG # 05-08-1756 Rev Ø)



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM8027#packaging for the most recent package drawings.

BGA Package
113-Lead (15mm × 15mm × 4.92mm)
(Reference LTC DWG # 05-08-1980 Rev Ø)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		12.70		
G		12.70		
H1	0.27	0.32	0.37	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 113				

PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

PIN	NAME
A1	GND
A2	ADJ
A3	BIAS2
A4	RUN
A5	SS
A6	BIAS1
A7	AUX
A8	GND
A9	GND
A10	GND
A11	GND
B1	RT
B2	GND
B3	GND
B4	GND
B5	GND
B6	GND
B7	GND
B8	GND
B9	GND
B10	GND
B11	GND
C1	SYNC
C2	GND
C3	GND
C4	GND
C5	GND
C6	GND
C7	GND
C8	GND
C9	GND
C10	GND
C11	GND
D1	GND
D2	GND
D3	GND
D4	GND
D5	GND

PIN	NAME
D6	GND
D7	GND
D8	GND
D9	GND
D10	GND
D11	GND
E1	GND
E2	GND
E3	GND
E4	GND
E5	GND
E6	GND
E7	GND
E8	GND
E9	V_{OUT}
E10	V_{OUT}
E11	V_{OUT}
F1	GND
F2	GND
F3	GND
F4	GND
F5	GND
F6	GND
F7	GND
F8	GND
F9	V_{OUT}
F10	V_{OUT}
F11	V_{OUT}
G5	GND
G6	GND
G7	GND
G8	GND
G9	V_{OUT}
G10	V_{OUT}
G11	V_{OUT}
H1	V_{IN}
H2	V_{IN}
H3	V_{IN}

PIN	NAME
H5	GND
H6	GND
H7	GND
H8	GND
H9	V_{OUT}
H10	V_{OUT}
H11	V_{OUT}
J1	V_{IN}
J2	V_{IN}
J3	V_{IN}
J5	GND
J6	GND
J7	GND
J8	GND
J9	V_{OUT}
J10	V_{OUT}
J11	V_{OUT}
K1	V_{IN}
K2	V_{IN}
K3	V_{IN}
K5	GND
K6	GND
K7	GND
K8	GND
K9	V_{OUT}
K10	V_{OUT}
K11	V_{OUT}
L1	V_{IN}
L2	V_{IN}
L3	V_{IN}
L5	GND
L6	GND
L7	GND
L8	GND
L9	V_{OUT}
L10	V_{OUT}
L11	V_{OUT}

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/11	Changed Shutdown Current Supply to 9µA in Features.	1
		Updated Absolute Maximum Ratings section.	2
		Updated $V_{BIAS1(MINOV)}$ and Note 3 in Electrical Characteristics section.	3
		Replaced graph 9.	4
		Updated Pin Functions section.	9
		Text edits to Applications Information.	11-16
		Updated Typical Applications.	17, 18
		Updated Related Parts.	22
B	9/11	Added (Note 3) notation to the Order Information section.	2
		Updated minimum spec for V_{BIAS2}.	3
		Updated descriptions for AUX and BIAS2 in the Pin Functions section.	9
		Updated text in the Input Power Requirements section.	11
		Added text to end of the BIAS Power section.	12
C	05/14	Add BGA package option	1, 2
		Add advisory notice	9
		Add BGA package drawing	19
D	12/16	Corrected R_T value from 162k to 75k	12
		Updated Related Parts	22

LINEAR TECHNOLOGY

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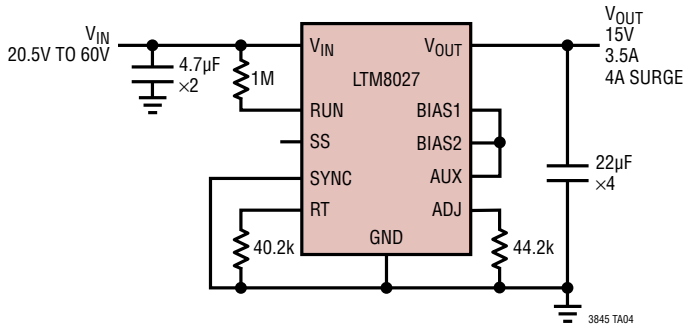
TYPICAL APPLICATION

15V V_{OUT} Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8050	2A, 58V DC/DC µModule Regulator	$3.6V \le V_{IN} \le 58V$, $0.8V \le V_{OUT} \le 24V$, Synchronizable, Parallelable, 9mm × 15mm × 4.92mm BGA
LTM4601/ LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4601-1 Version has no Remote Sensing
LTM4603	6A DC/DC µModule with PLL and Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version has no Remote Sensing, Pin Compatible with the LTM4601
LTM4604A	4A Low V_{IN} DC/DC µModule Regulator	$2.375V \le V_{IN} \le 5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.3mm LGA
LTM4608A	8A Low V_{IN} DC/DC µModule Regulator	$2.7V \le V_{IN} \le 5V$, $0.6V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.8mm LGA
LTM8020	200mA, 36V DC/DC µModule Regulator	Fixed 450kHz Frequency, $1.25V \le V_{OUT} \le 5V$, 6.25mm × 6.25mm × 2.32mm LGA
LTM8022	1A, 36V DC/DC µModule Regulator	Adjustable Frequency, $0.8V \le V_{OUT} \le 5V$, 9mm × 11.25mm × 2.82mm LGA, Pin Compatible to the LTM8023
LTM8023	2A, 36V DC/DC µModule Regulator	Adjustable Frequency, $0.8V \le V_{OUT} \le 5V$, 9mm × 11.25mm × 2.82mm LGA, Pin Compatible to the LTM8022
LTM8025	3A, 36V DC/DC µModule Regulator	$0.8V \le V_{OUT} \le 24V$, 9mm × 15mm × 4.32mm LGA
LTM4624	$14V_{IN}$, 4A, Step-Down µModule Regulator in Tiny 6.25mm × 6.25mm × 5.01mm BGA	$4V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, V_{OUT} Tracking, PGOOD, Light Load Mode, Complete Solution in $1cm^2$ (Single Sided PCB)
LTM4644	Quad 4A, 14V Step-Down µModule Regulator with Configurable Output Array	$4V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, CLK Input and Output, V_{OUT} Tracking, PGOOD, 9mm × 15mm × 5.01mm BGA
LTM8064	$58V_{IN}$, 6A C_{VCC} Step-Down µModule Regulator	$6V \le V_{IN} \le 58V$, $1.2V \le V_{OUT} \le 36V$, 16mm × 11.9mm × 4.92mm BGA Package
LTM8056	$58V_{IN}$, 48 V_{OUT} Buck-Boost µModule Regulator	$5V \le V_{IN} \le 58V$, $1.2V \le V_{OUT} \le 48V$, 15mm × 15mm × 4.92mm BGA Package
LTM8053	$40V_{IN}$, 3.5A Step-Down µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 15V$, 6.25mm × 9mm × 3.32mm BGA Package

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