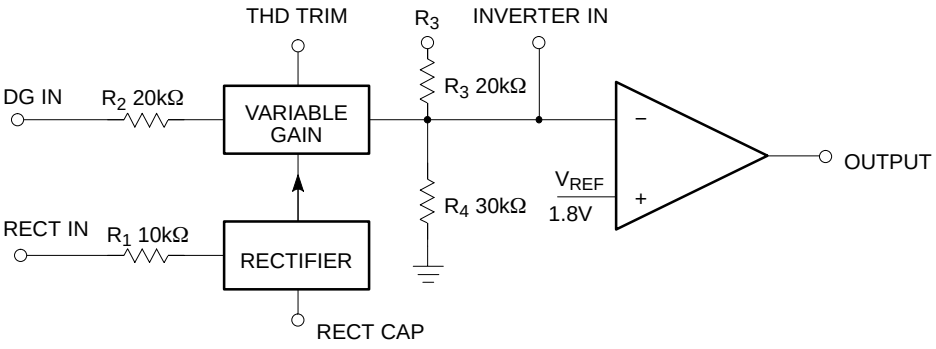


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Operating Voltage	V_{CC}	18	VDC
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Power Dissipation	P_D	400	mW
Thermal Resistance, Junction−to−Ambient N Package D Package	$R_{\theta JA}$	 75 105	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	−	6.0	−	18	V
Supply Current	I_{CC}	No Signal	−	4.2	4.8	mA
Output Current Capability	I_{OUT}	−	± 20	−	−	mA
Output Slew Rate	SR	−	−	± .5	−	V/μs
Gain Cell Distortion (Note 2)		Untrimmed Trimmed	−	0.5 0.1	2.0	%
Resistor Tolerance		−	−	± 5	± 15	%
Internal Reference Voltage		−	1.65	1.8	1.95	V
Output DC Shift (Note 3)		Untrimmed	−	± 90	± 150	mV
Expandor Output Noise		No Signal, 15 Hz−20 kHz (Note 1)	−	20	60	μV
Unity Gain Level (Note 5)		1.0 kHz	−1.5	0	+1.5	dBm
Gain Change (Notes 2 and 4)		−	−	± 0.1	−	dB
Reference Drift (Note 4)		−	−	+2.0, −25	+20, −50	mV
Resistor Drift (Note 4)		−40°C to +85°C	−	+10, −12	−	%
Tracking Error (Measured Relative to Value at Unity Gain) Equals [V_O − V_O (unity gain)] dB − V_2dBm		Rectifier Input, V_{CC} = +6.0 V V_2 = +6.0 dBm, V_1 = 0 dB V_2 = −30 dBm, V_1 = 0 dB	−	 +0.2 +0.2	 −1.0, +1.5	dB
Channel Separation		−	−	60	−	dB

1. Input to V_1 and V_2 grounded.
2. Measured at 0 dBm, 1.0 kHz.
3. Expandor AC input change from no signal to 0 dBm.
4. Relative to value at T_A = 25°C.
5. 0 dBm = 775 mV_{RMS}.

Circuit Description

The SA571 compandor building blocks, as shown in the block diagram, are a full−wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full−wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively−coupled voltage inputs as shown in the following equation. Note that for capacitively−coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1 μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\,avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\,avg}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade−off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{\frac{-t}{\tau}} + G_{final}$$

$$\tau = 10k\Omega \times C_{RECT}$$

The variable gain cell is a current−in, current−out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively−coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non−inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ± 20 mA output current. This allows a +13 dBm (3.5 V_{RMS}) output into a 300 Ω load which, with a series resistor and proper transformer, can result in +13 dBm with a 600 Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input−output transfer curve for basic compressor or expander circuits.

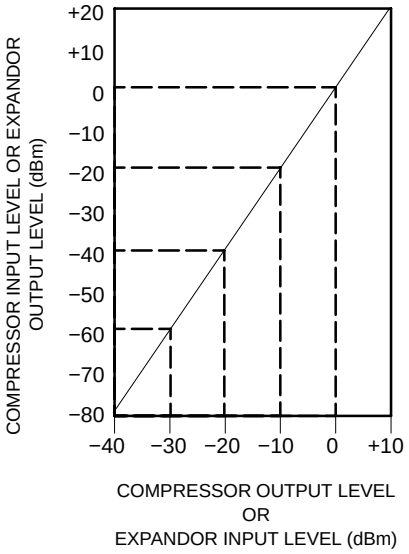


Figure 2. Basic Input−Output Transfer Curve

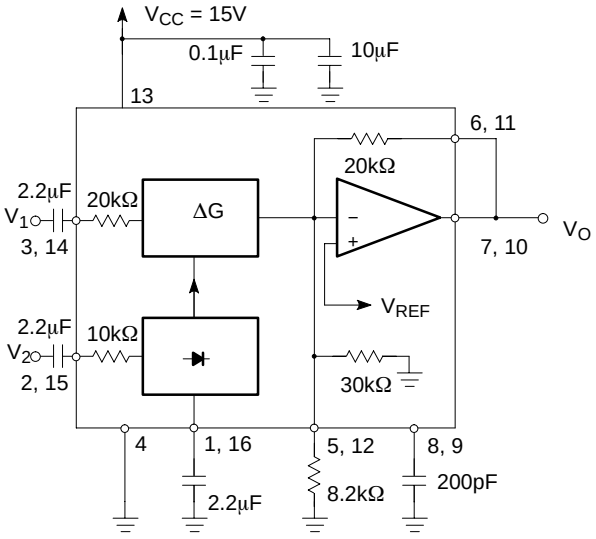


Figure 3. Typical Test Circuit

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non−critical applications, an integrated circuit operational transconductance amplifier can be used, but when high−performance is required, one has to resort to complex discrete circuitry with many expensive, well−matched components. This paper describes an inexpensive integrated circuit, the SA571 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal−to−noise ratio (90 dB), and wide dynamic range (110 dB).

Circuit Background

The SA571 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal−to−noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 4 graphically shows what a compandor can do for the signal−to−noise ratio of a restricted dynamic range channel. The input level range of +20 to −80 dB is shown undergoing a 2−to−1 compression where a 2.0 dB input level change is compressed into a 1.0 dB output level change by the compressor. The original 100 dB of dynamic range is thus compressed to a 50 dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45 dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full−wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple Operational Transconductance Multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

Basic Hook−up and Operation

Figure 5 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full−wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 V reference denoted V_{REF}. The non−inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

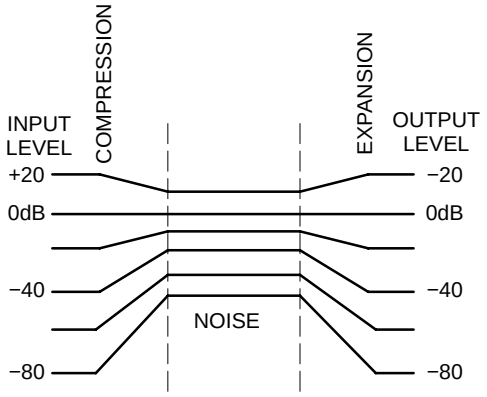


Figure 4. Restricted Dynamic Range Channel

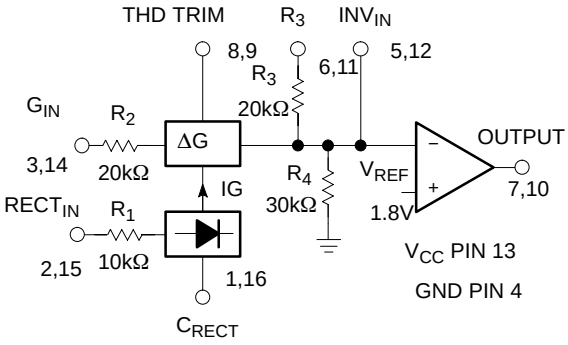
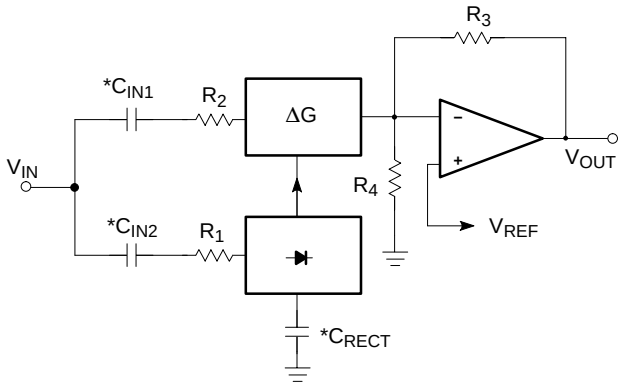


Figure 5. Chip Block Diagram (1 of 2 Channels)

Figure 6 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6.0 dB, the gain control current will drop by a factor of 2, and so the gain will drop 6.0 dB. The output level at V_{OUT} will thus drop 12 dB, giving us the desired 2−to−1 expansion.



NOTE: $\text{GAIN} = \left(\frac{2\,R_3\,V_{IN}\,(avg)}{R_1\,R_2\,I_B}\right)^2$

$I_B = 140\mu A$

*EXTERNAL COMPONENTS

Figure 6. Basic Expander

Figure 7 shows the hook−up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\,DC = \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) V_{REF}$$

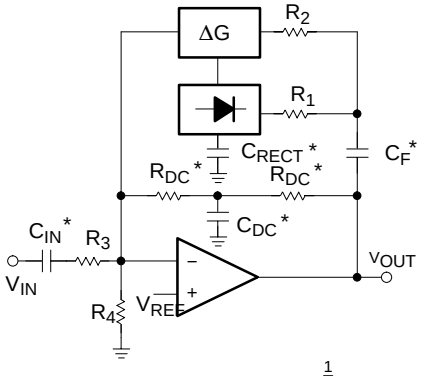
$$V_{OUT}\,DC = \left(1 + \frac{R_{DCTOT}}{30k\Omega}\right) 1.8V$$

The output of the expander will bias up to:

$$V_{OUT}\,DC = \left(1 + \frac{R_3}{R_4}\right) V_{REF}$$

$$V_{OUT}\,DC = \left(1 + \frac{20k\Omega}{30k\Omega}\right) 1.8V = 3.0V$$

The output will bias to 3.0 V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTE: GAIN $= \left(\frac{R_1\,R_2\,I_B}{2R_3\,V_{INavg}}\right)^{\frac{1}{2}}$

$I_B = 140\mu A$

*EXTERNAL COMPONENTS

Figure 7. Basic Compressor

Circuit Details − Rectifier

Figure 8 shows the concept behind the full−wave averaging rectifier. The input current to the summing node of the op amp, V_{IN}/R_1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

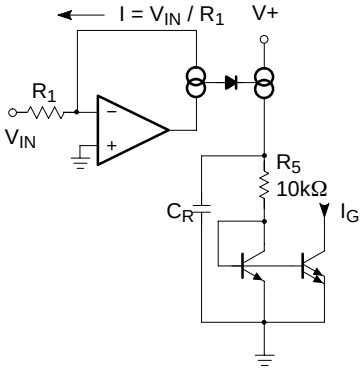
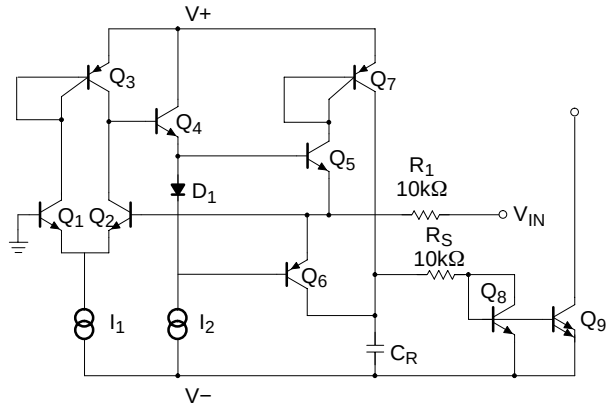


Figure 8. Rectifier Concept

Figure 9 shows the rectifier circuit in more detail. The op amp is a one−stage op amp, biased so that only one output device is on at a time. The non−inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8 V, V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN β's of 200 and PNP β's of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13 dB gain error.



NOTE: $I_G = 2\frac{V_{IN}\ avg}{R\ 1}$

Figure 9. Simplified Rectifier Schematic

At very low input signal levels the bias current of Q_2, (typically 50 nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1.0 mV of offset will cause an input current of 100 nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250 μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 10 shows the rectifier accuracy vs. input level at a frequency of 1.0 kHz.

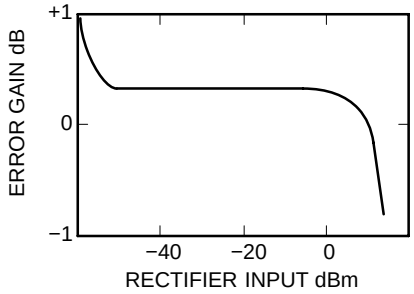


Figure 10. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll−off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0 dBm, −20 dBm, and −40 dBm is shown in Figure 11. The response at all three levels is flat to well above the audio range.

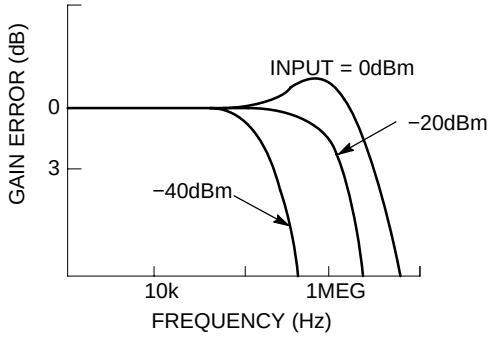
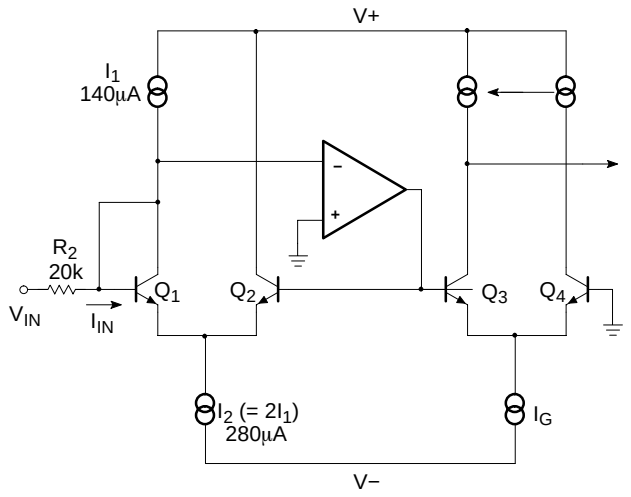


Figure 11. Rectifier Frequency Response vs. Input Level

Variable Gain Cell

Figure 12 is a diagram of the variable gain cell. This is a linearized two−quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.



NOTE: $I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$

Figure 12. Simplified ΔG Cell Schematic

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} (= V_{IN}/R_2) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non−linear for large signals, since it is compensating for the non−linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN} I_G}{R_2 I_1}$$

This equation is linear and temperature−insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non−linearity is generated, which results in second harmonic distortion. Figure 13 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8 dBm level. At a nominal operating level of 0 dBm, a 1.0 mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 14 shows the simple trim network required.

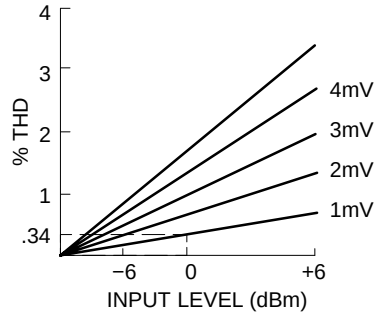


Figure 13. ΔG Cell Distortion vs. Offset Voltage

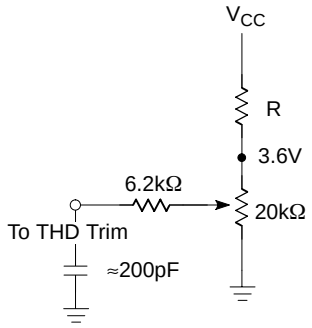


Figure 14. THD Trim Network

Figure 15 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20 kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20 dB of gain reduction. At high gains, the signal to noise ratio is 90 dB, and the total dynamic range from maximum signal to minimum noise is 110 dB.

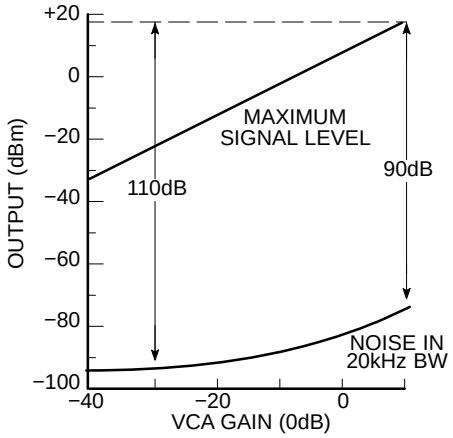


Figure 15. Dynamic Range

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 16 shows such a trim network.

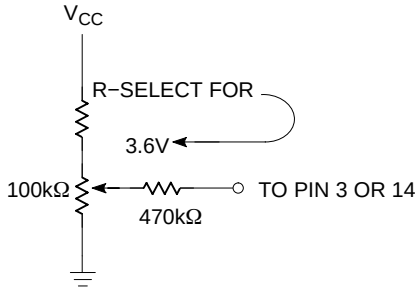


Figure 16. Control Signal Feedthrough

Operation Amplifier

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1.0 MHz bandwidth. Figure 17 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10 pF may be used. The output stage, although capable of output currents in excess of 20 mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

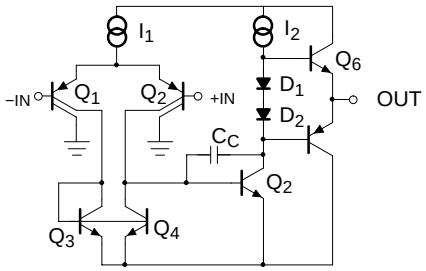


Figure 17. Operational Amplifier

ORDERING INFORMATION

Device	Description	Temperature Range	Shipping†
SA571D	16−Pin Plastic Small Outline (SO−16 WB) Package	−40 to +85°C	47 Units / Rail
SA571DG	16−Pin Plastic Small Outline (SO−16 WB) Package (Pb−Free)	−40 to +85°C	47 Units / Rail
SA571DR2	16−Pin Plastic Small Outline (SO−16 WB) Package	−40 to +85°C	1000 / Tape & Reel
SA571DR2G	16−Pin Plastic Small Outline (SO−16 WB) Package (Pb−Free)	−40 to +85°C	1000 / Tape & Reel
SA571N	16−Pin Plastic Dual In−Line Package (PDIP−16)	−40 to +85°C	25 Units / Rail
SA571NG	16−Pin Plastic Dual In−Line Package (PDIP−16) (Pb−Free)	−40 to +85°C	25 Units / Rail

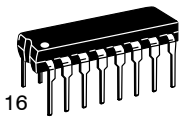
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

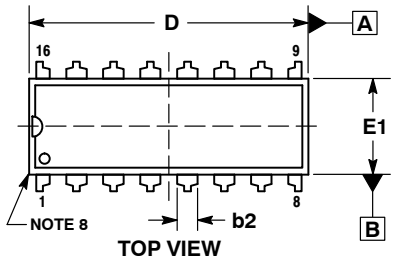
ON Semiconductor®

PDIP−16
CASE 648−08
ISSUE V

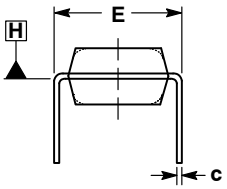
DATE 22 APR 2015



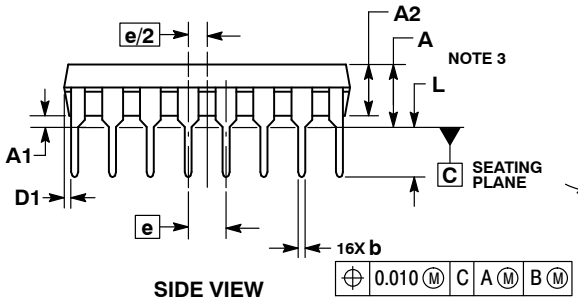
SCALE 1:1



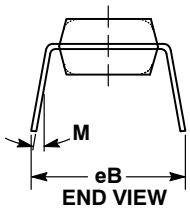
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW
NOTE 6

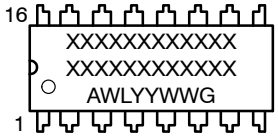
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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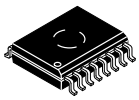
DESCRIPTION:	PDIP−16	PAGE 1 OF 1

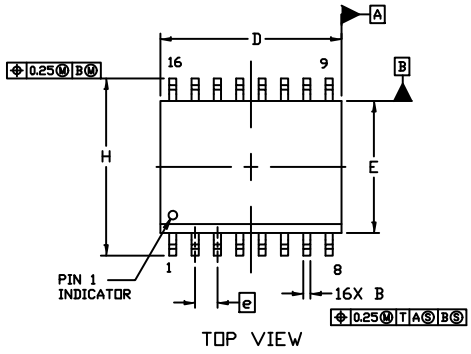
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

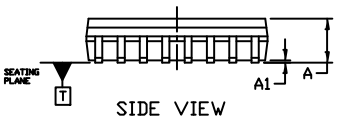
DATE 08 OCT 2021



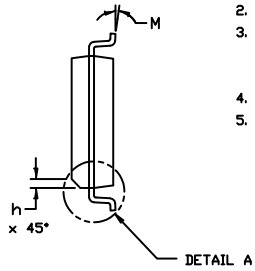
1
SCALE 1:1



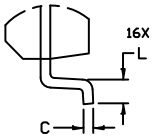
TOP VIEW



SIDE VIEW



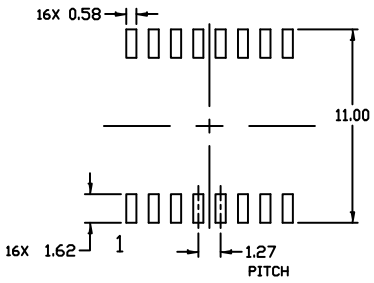
END VIEW



DETAIL A
2X SCALE

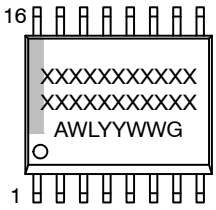
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



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DESCRIPTION:	**SOIC−16 WB**	**PAGE 1 OF 1**

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