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1. Electrical Specifications

Table 1. Recommended	Operating Conditions
----------------------	-----------------------------

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply Voltage ¹	V _{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I _{DD}	Output enabled LVPECL CML LVDS CMOS	 	111 99 90 81	121 108 98 88	mA
		Tristate mode	—	60	75	mA
Output Enable (OE) ²		V _{IH}	0.75 x V _{DD}		—	V
		V _{IL}	—		0.5	V
Operating Temperature Range	T _A		-40		85	٥C
Notes:			-1			

Notes:

1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 8 for further details.

2. OE pin includes a 17 k Ω pullup resistor to V_{DD}.

Table 2. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Nominal Frequency ^{1,2}	f _O	LVPECL/LVDS/CML	10		945	MHz
		CMOS	10	—	160	MHz
Initial Accuracy	f _i	Measured at +25 °C at time of shipping	_	±1.5		ppm
Temperature Stability ^{1,3}			7 20 50		+7 +20 +50	ppm
Aging		Frequency drift over first year	_	_	±3	ppm
	f _a	Frequency drift over 20 year life	_		±10	ppm

Notes:

1. See Section 3. "Ordering Information" on page 8 for further details.

2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.

- 3. Selectable parameter specified by part number.
- **4.** Time from powerup or tristate mode to f_{O} .

Table 2. CLK± Output Frequency Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Total Stability		Temp stability = ±7 ppm	_	_	±20	ppm
		Temp stability = ±20 ppm	—	_	±31.5	ppm
		Temp stability = ±50 ppm		_	±61.5	ppm
Powerup Time ⁴	tosc		_	_	10	ms
Notes:						

1. See Section 3. "Ordering Information" on page 8 for further details.

2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.

3. Selectable parameter specified by part number.

4. Time from powerup or tristate mode to f_O.

Table 3. CLK± Output Levels and Symmetry

Symbol	Test	Condition	Min	Тур	Max	Unit
Vo	mi	mid-level			V _{DD} – 1.25	V
V _{OD}	swi	ing (diff)	1.1	_	1.9	V_{PP}
V _{SE}	swing (s	ingle-ended)	0.55		0.95	V_{PP}
Vo	m	id-level	1.125	1.20	1.275	V
V _{OD}	swi	swing (diff)		0.7	0.9	V_{PP}
V	2.5/3.3 V o	2.5/3.3 V option mid-level 1.8 V option mid-level		V _{DD} – 1.30	—	V
۷O	1.8 V op			V _{DD} – 0.36	—	V
V	2.5/3.3 V oj	2.5/3.3 V option swing (diff)		1.50	1.90	V_{PP}
VOD	1.8 V option swing (diff)		0.35	0.425	0.50	V_{PP}
V _{OH}	I _{OH} = 32 mA		0.8 x V _{DD}	_	V _{DD}	V
V _{OL}	I _{OL}	= 32 mA	—		0.4	V
t _{R,} t _F	LVPECI	_/LVDS/CML	—		350	ps
	CMOS w	ith C _L = 15 pF	—	1	—	ns
SYM	LVPECL: (diff) LVDS: CMOS:	V _{DD} – 1.3 V 1.25 V (diff) V _{DD} /2	45		55	%
	V _O V _{OD} V _{SE} V _O V _{OD} V _{OD} V _{OD} V _{OH} V _{OL}	$\begin{tabular}{ c c c c } \hline V_O & mi \\ \hline V_{OD} & swind (s) \\ \hline V_{SE} & swind (s) \\ \hline V_{OD} & swind (s) \\ \hline V_{OD} & swind (s) \\ \hline V_{OD} & 1.8 \mbox{ V opt} \\ \hline V_{OD} & 1.8 \mbox{ V opt} \\ \hline V_{OD} & 1.8 \mbox{ V opt} \\ \hline V_{OH} & I_{OH} \\ \hline V_{OL} & I_{OL} \\ \hline V_{R, \ TF} & LVPECL \\ \hline CMOS \ w \\ \hline SYM & LVPECL : \\ (diff) \\ LVDS : \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c } \hline V_O & mid-level \\ \hline V_{OD} & swing (diff) \\ \hline V_{SE} & swing (single-ended) \\ \hline V_O & mid-level \\ \hline V_{OD} & swing (diff) \\ \hline V_O & 2.5/3.3 \ V \ option \ mid-level \\ \hline 1.8 \ V \ option \ mid-level \\ \hline V_{OD} & 2.5/3.3 \ V \ option \ mid-level \\ \hline 1.8 \ V \ option \ swing (diff) \\ \hline V_{OD} & 2.5/3.3 \ V \ option \ swing (diff) \\ \hline 1.8 \ V \ option \ swing (diff) \\ \hline 1.8 \ V \ option \ swing (diff) \\ \hline V_{OD} & 1.8 \ V \ option \ swing (diff) \\ \hline V_{OH} & I_{OH} = 32 \ mA \\ \hline V_{OL} & I_{OL} = 32 \ mA \\ \hline V_{OL} & I_{OL} = 32 \ mA \\ \hline t_{R}, t_{F} & LVPECL/LVDS/CML \\ \hline CMOS \ with \ C_L = 15 \ pF \\ \hline SYM & LVPECL: \ V_{DD} - 1.3 \ V \\ (diff) \\ LVDS: \ 1.25 \ V (diff) \\ \hline \end{array}$	$\begin{tabular}{ c c c c c c } \hline V_O & mid-level & V_{DD} - 1.42 \\ \hline V_{OD} & swing (diff) & 1.1 \\ \hline V_{SE} & swing (single-ended) & 0.55 \\ \hline V_O & mid-level & 1.125 \\ \hline V_{OD} & swing (diff) & 0.5 \\ \hline V_O & swing (diff) & 0.5 \\ \hline V_O & 2.5/3.3 \ V \ option \ mid-level & \\ \hline 1.8 \ V \ option \ mid-level & \\ \hline 1.8 \ V \ option \ swing (diff) & 1.10 \\ \hline 1.8 \ V \ option \ swing (diff) & 1.10 \\ \hline 1.8 \ V \ option \ swing (diff) & 0.35 \\ \hline V_{OD} & 1.8 \ V \ option \ swing (diff) & 0.35 \\ \hline V_{OD} & 1.8 \ V \ option \ swing (diff) & 0.35 \\ \hline V_{OH} & 1_{OH} = 32 \ mA & 0.8 \ x \ V_{DD} \\ \hline V_{OL} & 1_{OL} = 32 \ mA & \\ \hline t_{R}, t_F & LVPECL/LVDS/CML & \\ \hline CMOS \ with \ C_L = 15 \ pF & \\ \hline SYM & LVPECL: \ \ V_{DD} - 1.3 \ V \\ (diff) & LVDS: \ 1.25 \ V \ (diff) & 45 \\ \hline \end{tabular}$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{tabular}{ c c c c c c c } \hline V_{O} & mid-level & V_{DD} - 1.42 & & V_{DD} - 1.25 \\ \hline V_{OD} & swing (diff) & 1.1 & & 1.9 \\ \hline V_{SE} & swing (single-ended) & 0.55 & & 0.95 \\ \hline V_{O} & mid-level & 1.125 & 1.20 & 1.275 \\ \hline V_{OD} & swing (diff) & 0.5 & 0.7 & 0.9 \\ \hline V_{OD} & swing (diff) & 0.5 & 0.7 & 0.9 \\ \hline V_{OD} & 2.5/3.3 V option mid-level & & V_{DD} - 1.30 & \\ \hline V_{OD} & 2.5/3.3 V option swing (diff) & 1.10 & 1.50 & 1.90 \\ \hline V_{OD} & 2.5/3.3 V option swing (diff) & 1.10 & 1.50 & 1.90 \\ \hline V_{OD} & 2.5/3.3 V option swing (diff) & 0.35 & 0.425 & 0.50 \\ \hline V_{OD} & 1.8 V option swing (diff) & 0.35 & 0.425 & 0.50 \\ \hline V_{OL} & I_{OH} = 32 mA & 0.8 x V_{DD} & & V_{DD} \\ \hline V_{OL} & I_{OL} = 32 mA & & & 0.4 \\ \hline t_{R,} t_{F} & LVPECL/LVDS/CML & & & 350 \\ \hline CMOS with C_{L} = 15 pF & & 1 & \\ \hline SYM & LVPECL: & V_{DD} - 1.3 V \\ (diff) \\ LVDS: & 1.25 V (diff) & 45 & & 55 \\ \hline \end{tabular}$

1. 50 Ω to V_{DD} – 2.0 V. **2.** R_{term} = 100 Ω (differential).

3. $C_L = 15 \, pF$

Table 4. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Phase Jitter (RMS) ¹	фJ	12 kHz to 20 MHz (OC-48)	—	0.25	0.40	ps
for $F_{OUT} \ge 500 \text{ MHz}$		50 kHz to 80 MHz (OC-192)		0.26	0.37	ps
Phase Jitter (RMS) ¹	φJ	12 kHz to 20 MHz (OC-48)		0.36	0.50	ps
for F_{OUT} of 125 to 500 MHz		50 kHz to 80 MHz (OC-192) ²	—	0.34	0.42	ps
Phase Jitter (RMS)	φJ	12 kHz to 20 MHz (OC-48) ²		0.62		ps
for F _{OUT} of 10 to 160 MHz CMOS Output Only		50 kHz to 20 MHz ²		0.61	_	ps
Notes:	•		•	•	•	

Notes:

1. Refer to AN256 for further information.

2. Max offset frequencies: 80 MHz for FOUT \geq 250 MHz, 20 MHz for 50 MHz \leq FOUT <250 MHz,

2 MHz for 10 MHz \leq FOUT <50 MHz.

Table 5. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Period Jitter*	J _{PER}	RMS	_	2	_	ps
		Peak-to-Peak	_	14	_	ps
*Note: Any output mode, including C	CMOS, LVPI	ECL, LVDS, CML. N = 1000 cycles.	Refer to AN	279 for furt	her informa	tion.

Table 6. CLK± Output Phase Noise (Typical)

Offset Frequency (f)	120.00 MHz LVDS	156.25 MHz LVPECL	622.08 MHz LVPECL	Unit
100 Hz	-112 -122	-105	-97	
1 kHz 10 kHz	-122 -132	-122 -128	-107 -116	
100 kHz 1 MHz	-137 -144	-135 -144	-121 -134	dBc/Hz
10 MHz 100 MHz	-144 -150 n/a	-144 -147 n/a	-134 -146 -148	

5

Table 7. Environmental Compliance

The Si530/531 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross & Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	J-STD-020, MSL1
Contact Pads	Gold over Nickel

Table 8. Thermal Characteristics

(Typical values TA = 25 °C, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	_	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	_	°C/W
Ambient Temperature	Τ _Α		-40	_	85	°C
Junction Temperature	Т _Ј		_		125	°C

Table 9. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T _{AMAX}	85	٥C
Supply Voltage, 1.8 V Option	V _{DD}	-0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V _{DD}	-0.5 to +3.8	V
Input Voltage (any input pin)	VI	–0.5 to V _{DD} + 0.3	V
Storage Temperature	Τ _S	-55 to +125	٥C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile) ²	T _{PEAK}	260	٥C
Soldering Temperature Time @ T _{PEAK} (Pb-free profile) ²	t _P	20–40	seconds

Notes:

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.skyworksinc.com/en/application-pages/timing-lookup-customize for further information, including soldering profiles.

2. Pin Descriptions

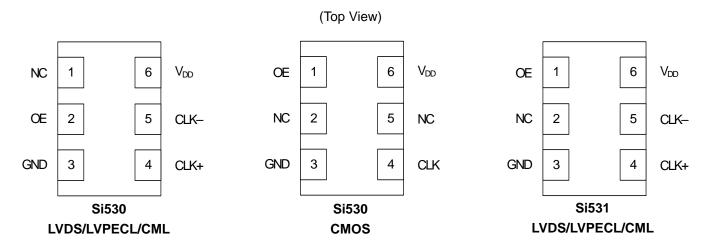


Table 10. Pinout for Si530 Series

Pin	Symbol	LVDS/LVPECL/CML Function	CMOS Function			
1	OE (CMOS only)*	No connection	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled			
2	OE (LVPECL,LVDS, CML)*	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled	No connection			
3	GND	Electrical and Case Ground	Electrical and Case Ground			
4	CLK+	Oscillator Output	Oscillator Output			
5	CLK–	Complementary Output	No connection			
6	V _{DD}	Power Supply Voltage	Power Supply Voltage			
*Note	*Note: OE includes a 17 k Ω pullup resistor to V _{DD} .					

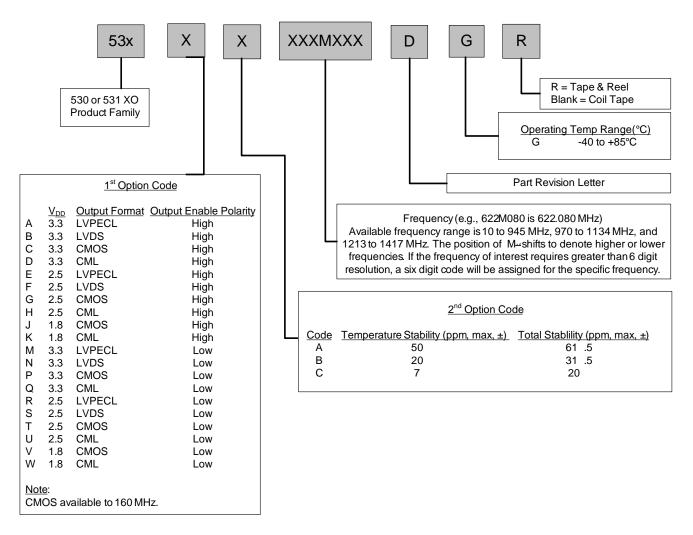
Table 11. Pinout for Si531 Series

Pin	Symbol	LVDS/LVPECL/CML Function		
1	OE (LVPECL, LVDS, CML)*	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled		
2	No connection	No connection		
3	GND	Electrical and Case Ground		
4	CLK+	Oscillator Output		
5	CLK-	Complementary output		
6	V _{DD}	Power Supply Voltage		
*Note: OE includes a 17 k Ω pullup resistor to V _{DD} .				

3. Ordering Information

The Si530/531 XO supports a variety of options including frequency, temperature stability, output format, and V_{DD} . Specific device configurations are programmed into the Si530/531 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Skyworks Solutions provides a web browser-based part number configuration utility to simplify this process.

Refer to www.skyworksinc.com/en/application-pages/timing-lookup-customize to access this tool and for further ordering instructions. The Si530 and Si531 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm package. The Si531 Series supports an alternate OE pinout (pin #1) for the LVPECL, LVDS, and CML output formats. See Tables 10 and 11 for the pinout differences between the Si530 and Si531 series.



Example P/N: 530AB622M080DGR is a 5 x 7 XO in a 6 pad package. The frequency is 622.080 MHz, with a 3.3 V supply, LVPECL output and Output Enable active high polarity Temperature stability is specified as ± 20 ppm. The part is specified for -40 to ± 85 °C ambient temperature range operation and is shipped in tape and reel format

Figure 1. Part Number Convention

4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si530/531. Table 12 lists the values for the dimensions shown in the illustration.

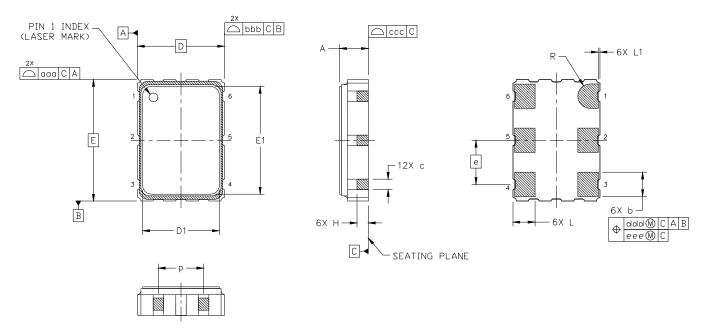


Figure 2. Si530/531 Outline Diagram

Table 12. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
С	0.50	0.60	0.70
D	5.00 BSC		
D1	4.30	4.40	4.50
е	2.54 BSC		
E	7.00 BSC		
E1	6.10	6.20	6.30
Н	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
р	1.80	—	2.60
R	0.70 REF		
aaa	0.15		
bbb	0.15		
CCC	0.10		
ddd	ddd 0.10		
eee 0.05			
 Notes: All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 			

5. Si530/Si531 Mark Specification

Figure 3 illustrates the mark specification for the Si530/Si531. Table 13 lists the line information.

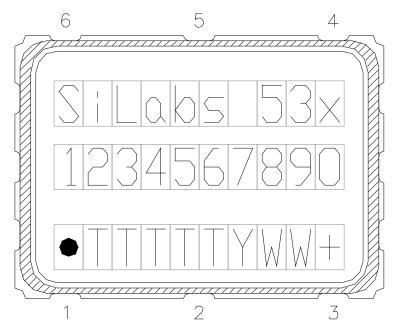


Figure 3. Mark Specification

Table 13. Si53x Top Mark Description

Line	Position	Description	
1	1–10	"SiLabs"+ Part Family Number, 53x (First 3 characters in part number where $x = 0$ indicates a 530 device and $x = 1$ indicates a 531 device).	
2	1–10	Si530, Si531: Option1 + Option2 + Freq(7) + Temp Si532, Si533, Si534, Si530/Si531 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp	
3			
	Position 1	Pin 1 orientation mark (dot)	
	Position 2	Product Revision (D)	
Position 3–6 Tiny Trace Code (4 alphanumeric charac		Tiny Trace Code (4 alphanumeric characters per assembly release instructions)	
Position 7 Year (least significant year digit), to be assigned by a		Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)	
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site	
	Position 10	"+" to indicate Pb-Free and RoHS-compliant	

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6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the

Si530/531. Table 14 lists the values for the dimensions shown in the illustration.

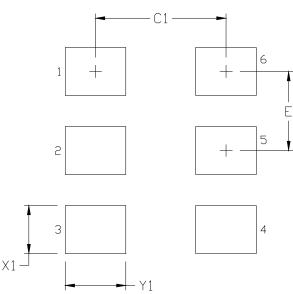


Figure 4. Si530/531 PCB Land Pattern Table 14. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95
Neteo	

Notes:

- General
 - 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
 - 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
 - 3. This Land Pattern Design is based on the IPC-7351 guidelines.
 - **4.** All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be $60 \ \mu m$ minimum, all the way around the pad.

Stencil Design

- **1.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 0.5

- Updated Table 1, "Recommended Operating Conditions," on page 3.
 - Added maximum supply current specifications.
 - Specified relationship between temperature at startup and operation temperature.
- Updated Table 4, "CLK± Output Phase Jitter," on page 5 to include maximum rms jitter generation specifications and updated typical rms jitter specifications.
- Added Table 6, "CLK± Output Phase Noise (Typical)," on page 5.
- Added Output Enable active polarity as an option in Figure 1, "Part Number Convention," on page 8.

Revision 0.5 to Revision 1.0

- Updated Note 3 in Table 1, "Recommended Operating Conditions," on page 3.
- Updated Figure 1, "Part Number Convention," on page 8.

Revision 1.0 to Revision 1.1

- Updated Table 1, "Recommended Operating Conditions," on page 3.
 - Device maintains stable operation over –40 to +85 °C operating temperature range.
 - Supply current specifications updated for revision D.
- Updated Table 2, "CLK± Output Frequency Characteristics," on page 3.
 - Added specification for ±20 ppm lifetime stability (±7 ppm temperature stability) XO.
- Updated Table 3, "CLK± Output Levels and Symmetry," on page 4.
 - Updated LVDS differential peak-peak swing specifications.
- Updated Table 4, "CLK± Output Phase Jitter," on page 5.
- Updated Table 5, "CLK± Output Period Jitter," on page 5.
 - Revised period jitter specifications.
- Updated Table 9, "Absolute Maximum Ratings¹," on page 6 to reflect the soldering temperature time at 260 °C is 20–40 sec per JEDEC J-STD-020C.
- Updated 3. "Ordering Information" on page 8.
- Changed ordering instructions to revision D.
 Added 5. "Si530/Si531 Mark Specification" on page 10.

Revision 1.1 to Revision 1.2

- Updated 2.5 V/3.3 V and 1.8 V CML output level specifications for Table 3 on page 4.
- Added footnotes clarifying max offset frequency test conditions for Table 4 on page 5.
- Added CMOS phase jitter specs to Table 4 on page 5.
- Removed the words "Differential Modes: LVPECL/LVDS/CML" in the footnote referring to AN256 in Table 4 on page 5.
- Separated 1.8 V, 2.5 V/3.3 V supply voltage specifications in Table 9 on page 6.
- Updated and clarified Table 9 on page 6 to include the "Moisture Sensitivity Level" and "Contact Pads" rows.
- Updated Figure 3 on page 10 and Table 13 on page 10 to reflect specific marking information.
 Previously, Figure 3 was generic.

Revision 1.2 to Revision 1.3

 Added Table 8, "Thermal Characteristics," on page 6.

Revision 1.3 to Revision 1.4

- Revised Figure 2 and Table 12 on page 9 to reflect current package outline diagram.
- Revised Figure 4 and Table 14 on page 11 to reflect the recommended PCB land pattern.

Revision 1.4 to Revision 1.5

• Changed "Trays" to "Coil Tape" in Ordering Guide.

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530AA64M2000DG	531FA162M000DG	530PA10M2400DG	530AC80M0000DG	530AC46M0800DG	
530AC184M320DG	530AA66M6600DG	530AB400M000DG	531BA250M000DG	531BA200M000DG	
530CA25M0000DG	531FC000199DG 5	30AB51M2000DG 5	30CC56M2800DG 5	30NB25M0000DG	
530BA80M0000DG	531AC1220M00DG	530AA166M000DG	531FA200M000DG	531FA250M000DG	
530JC80M0000DG	530CC24M5760DG	530JA98M3040DG	531FB156M250DG	530AA95M5730DG	
530PA128M000DG	530NB19M4400DG	531AA720M000DG	530CC14M0000DG	530PA140M000DG	
530JA100M000DG	530CB22M5792DG	530CB24M5760DG	530CC122M880DG	530CB122M880DG	
530CA61M4400DG	531KB800M000DG	530CB80M0000DG	530AA80M0000DG	530BA159M375DG	
531BA98M0000DG	530AA100M000DG	530BC125M000DG	530CA28M6000DG	531BB100M000DG	
531FA125M000DG	530GA22M5792DG	530GA24M5760DG	530CC25M0000DG	530GB80M0000DG	
531BA106M250DG	530NA65M0000DG	530GB45M1584DG	530GB49M1520DG	530BB50M0000DG	
530AA321M740DG	530NB24M5760DG	530FC100M000DG	530SC100M000DG	530VA100M000DG	
530NC400M000DG	530VC50M0000DG	530VC150M000DG	530SC200M000DG	530PC150M000DG	
530VC100M000DG	530GB160M000DG	530HC100M000DG	530HC125M000DG	531BA159M375DG	
530AB90M0000DG	530AC125M000DG	530AC90M0000DG	530AB10M0000DG	530AB135M000DG	
530AB93M3333DG	530AC10M0000DG	530AC135M000DG	530AC93M3333DG	530CB10M0000DG	
530CB27M0000DG	530BB470M000DG	530CC11M2896DG	531BB125M000DG	530HB156M250DG	
530KB156M250DG	530PB12M2880DG	530PB16M9344DG	530PB18M4320DG	531EB155M520DG	