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# SPECIFICATIONS

## AC SPECIFICATIONS

AVDD18x = 1.8 V, AVDD33x = 3.3 V, DVDD18x = 1.8 V, DVDD33x = 3.3 V, 1.0 V internal ADC reference, $f_{IN}$ = 2.5 MHz, $f_S$ = 80 MSPS, $R_S$ = 50 Ω, LNA + PGA gain = 35 dB, LPF cutoff = $f_{SAMPLECH}$/4, 12-bit operation, temperature = −40°C to +105°C, all specifications guaranteed by testing, unless otherwise noted.

**Table 1.**

| Parameter[1] | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ANALOG CHANNEL CHARACTERISTICS | LNA, PGA, and AAF channel | | | | |
| Gain | Programmable | | 17/23/29/35 | | dB |
| Gain Range | | | 18 | | dB |
| Gain Error | | −1.25 | | +1.25 | dB |
| Input Voltage Range[2] | Channel gain = 17 dB | | 0.283 | | V p-p |
| | Channel gain = 23 dB | | 0.142 | | V p-p |
| | Channel gain = 29 dB | | 0.071 | | V p-p |
| | Channel gain = 35 dB | | 0.036 | | V p-p |
| Input Resistance | 200 Ω input impedance | 0.200 | 0.265 | 0.300 | kΩ |
| | 200 kΩ input impedance | 160 | 200 | 240 | kΩ |
| Input Capacitance[2] | | | 7 | | pF |
| Input Referred Voltage Noise[2] | Maximum gain at 1 MHz | | | 1.85 | nV/√Hz |
| | Minimum gain at 1 MHz | | | 6.03 | nV/√Hz |
| Noise Figure[2] | Maximum gain, $R_S$ = 50 Ω, not terminated | | 7.1 | | dB |
| | Maximum gain, $R_S$ = $R_{IN}$ = 50 Ω | | 12.7 | | dB |
| Output Offset | Gain = 17 dB | −60 | | +60 | LSB |
| | Gain = 35 dB | −250 | | +250 | LSB |
| AAF Low-Pass Filter Cutoff | −3 dB, programmable | | 9.0 to 15.0 | | MHz |
| Tolerance | After filter autotune | −10 | ±5 | +10 | % |
| AAF Attenuation in Stop Band[2] | Third-order elliptic filter | | | | |
| | 2× cutoff | | 30 | | dB |
| | 3× cutoff | | 40 | | dB |
| Group Delay Variation[2] | Filter set at 9 MHz | | 400 | | ns |
| 1 dB Compression[2] | Relative to output | | 11.9 | | dBm |
| Saturation Flag Response Time | Time between saturation event and saturation flag going high (1 dB overdrive) | | 30 | 100 | ns |
| | Time between end of saturation event and saturation flag going low | 25 | 40 | | ns |
| Saturation Flag Accuracy | Gain = 29 dB | | | | |
| Off | For PGA voltages below 2 V p-p | | 2 | | V p-p |
| On | For PGA voltages above 2.25 V p-p | | 2.25 | | V p-p |
| Mux[2] | | | | | |
| On Resistance | | | 50 | | Ω |
| Switching Time | | | 200 | | ns |
| POWER SUPPLY | | | | | |
| AVDD18x[2] | | 1.7 | 1.8 | 1.9 | V |
| AVDD33x[2] | | 3.1 | 3.3 | 3.5 | V |
| DVDD18x[2] | | 1.7 | 1.8 | 1.9 | V |
| DVDD33x[2] | | 3.1 | 3.3 | 3.5 | V |
| $I_{AVDD18}$ | $f_S$ = 60 MSPS | | | 54 | mA |
| $I_{AVDD33}$ | $f_S$ = 60 MSPS | | | 65 | mA |
| $I_{DVDD18}$ | $f_S$ = 60 MSPS | | | 15 | mA |
| $I_{DVDD33}$ | $f_S$ = 60 MSPS | | | 2 | mA |
| Total Power Dissipation | No signal, typical supply voltage × maximum supply current; excludes output current | | | 345 | mW |

| Parameter[1] | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power-Down Dissipation | $T_A$ = −25°C to +105°C | | 2.5 | 4.0 | mW |
| | $T_A$ = −40°C to +25°C | | 2.5 | 8.0 | mW |
| Power Supply Rejection Ratio (PSRR)[2] | Relative to input | | 1.6 | | mV/V |
| ADC | | | | | |
| Resolution[2] | | | 12 | | Bits |
| Maximum Sample Rate | | | 80 | | MSPS |
| Signal-to-Noise Ratio (SNR) | $f_{IN}$ = 1 MHz | | 67 | | dB |
| Signal-to-Noise-and-Distortion Ratio (SINAD) [2] | | | 66 | | dB |
| SNRFS[2] | | | 68 | | dB |
| Differential Nonlinearity (DNL) | Guaranteed no missing codes | | | 1 | LSB |
| Integral Nonlinearity (INL) | $f_S$ = 60 MSPS | | 4 | 10 | LSB |
| | $f_S$ = 80 MSPS | | | 17 | LSB |
| Effective Number of Bits (ENOB)[2] | | | 10.67 | | LSB |
| ADC Output Characteristics[2] | | | | | |
| Maximum Capacitor Load | Per bit | | 20 | | pF |
| $I_{DVDD33}$ Peak Current with Capacitor Load[2] | Peak current per bit when driving a 20 pF load; can be programmed via the SPI port, if required | | | 40 | mA |
| ADC REFERENCE | | | | | |
| Output Voltage Error | VREF = 1.000 V | | | ±20 | mV |
| Load Regulation | At 1.0 mA, VREF = 1.000 V | | 2 | | mV |
| Current Output | | −1 | | +1 | mA |
| Input Resistance | | | 6 | | kΩ |
| FULL CHANNEL CHARACTERISTICS | LNA, PGA, AAF, and ADC | | | | |
| SNRFS | $f_{IN}$ = 1 MHz, −10 dBFS output | | | | |
| | Gain = 17 dB, $f_S$ = 60 MSPS | 60 | 64 | | dBFS |
| | Gain = 23 dB, $f_S$ = 60 MSPS | 60 | 64 | | dBFS |
| | Gain = 29 dB, $f_S$ = 60 MSPS | 60 | 64 | | dBFS |
| | Gain = 35 dB, $f_S$ = 60 MSPS | 60 | 64 | | dBFS |
| | Gain = 17 dB, $f_S$ = 80 MSPS | 45 | 62 | | dBFS |
| SINAD[2] | $f_{IN}$ = 1 MHz | | | | |
| | Gain = 17 dB | | 62 | | dB |
| | Gain = 23 dB | | 63 | | dB |
| | Gain = 29 dB | | 64 | | dB |
| | Gain = 35 dB | | 63 | | dB |
| Spurious-Free Dynamic Range (SFDR) | $f_{IN}$ = 1 MHz, −10 dBFS output | | | | |
| | Gain = 17 dB, $f_S$ = 60 MSPS | 62 | 68 | | dBc |
| | Gain = 23 dB, $f_S$ = 60 MSPS | 62 | 68 | | dBc |
| | Gain = 29 dB, $f_S$ = 60 MSPS | 62 | 68 | | dBc |
| | Gain = 35 dB, $f_S$ = 60 MSPS | 62 | 71 | | dBc |
| | Gain = 17 dB, $f_S$ = 80 MSPS | 45 | 62 | | dBc |
| Harmonic Distortion[2] | $f_{IN}$ = 1 MHz at −10 dBFS output | | | | |
| Second Harmonic | Gain = 17 dB | | −70 | | dBc |
| | Gain = 35 dB | | −70 | | dBc |
| Third Harmonic | Gain = 17 dB | | −66 | | dBc |
| | Gain = 35 dB | | −75 | | dBc |
| IM3 Distortion | $f_{IN1}$ = 1 MHz, $f_{IN2}$ = 1.1 MHz, −1 dBFS, gain = 35 dB | | −69 | | dBc |
| Gain Response Time | | | 600 | | ns |
| Overdrive Recovery Time | | | 200 | | ns |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and testing methodology.
[2] Guaranteed by design only.

## DIGITAL SPECIFICATIONS

AVDD18x = 1.8 V, AVDD33x = 3.3 V, DVDD18x = 1.8 V, DVDD33x = 3.3 V, 1.00 V internal ADC reference, $f_{IN}$ = 2.5 MHz, $f_S$ = 80 MSPS, $R_S$ = 50 Ω, LNA + PGA gain = 35 dB, LPF cutoff = $f_{SAMPLECH}$/4, 12-bit operation, temperature = −40°C to +105°C, all specifications guaranteed by testing, unless otherwise noted.

**Table 2.**

| Parameter[1] | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CLOCK INPUTS (CLK+, CLK–)[2] | | | | | |
| Logic Compliance | | | CMOS/LVDS/LVPECL | | |
| Differential Input Voltage[3] | Full | 250 | | | mV p-p |
| Input Common-Mode Voltage | Full | | 1.2 | | V |
| Input Resistance (Differential) | 25°C | | 20 | | kΩ |
| Input Capacitance | 25°C | | 1.5 | | pF |
| LOGIC INPUTS (PDWN, SCLK, AUX, MUX[0], MUX[1], ZSEL)[2] | | | | | |
| Logic 1 Voltage | Full | 1.2 | | 3.6 | V |
| Logic 0 Voltage | Full | | | 0.3 | V |
| Input Resistance | 25°C | | 30 | | kΩ |
| Input Capacitance | 25°C | | 0.5 | | pF |
| LOGIC INPUT ($\overline{CS}$)[2] | | | | | |
| Logic 1 Voltage | Full | 1.2 | | 3.6 | V |
| Logic 0 Voltage | Full | | | 0.3 | V |
| Input Resistance | 25°C | | 70 | | kΩ |
| Input Capacitance | 25°C | | 0.5 | | pF |
| LOGIC INPUT (SDI)[2] | | | | | |
| Logic 1 Voltage | Full | 1.2 | | DVDD33x + 0.3 | V |
| Logic 0 Voltage | Full | 0 | | 0.3 | V |
| Input Resistance | 25°C | | 30 | | kΩ |
| Input Capacitance | 25°C | | 2 | | pF |
| LOGIC OUTPUT (SDO) | | | | | |
| Logic 1 Voltage ($I_{OH}$ = 800 µA) | Full | 3.0 | | | V |
| Logic 0 Voltage ($I_{OL}$ = 50 µA) | Full | | | 0.3 | V |
| LOGIC OUTPUTS (D11 to D0, SFLAG) | | | | | |
| Logic 1 Voltage ($I_{OH}$ = 2 mA) | Full | 3.0 | | | V |
| Logic 0 Voltage ($I_{OL}$ = 2 mA) | Full | | | 0.3 | V |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and testing methodology.
[2] Guaranteed by design only.
[3] Specified for LVDS and LVPECL only.

## SWITCHING SPECIFICATIONS

AVDD18x = 1.8 V, AVDD33x = 3.3 V, DVDD18x = 1.8 V, DVDD33x = 3.3 V, 1.00 V internal ADC reference, $f_{IN}$ = 2.5 MHz, $f_S$ = 80 MSPS, $R_S$ = 50 Ω, LNA + PGA gain = 35 dB, LPF cutoff = $f_{SAMPLECH}/4$, 12-bit operation, temperature = −40°C to +105°C, unless otherwise noted. All specifications guaranteed by design only.

**Table 3.**

| Parameter[1] | Symbol | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CLOCK | | | | | | |
| Clock Rate | | Full | 10 | | 80 | MSPS |
| Clock Pulse Width High at 80 MSPS | $t_{EH}$ | Full | | 6.25 | | ns |
| Clock Pulse Width Low at 80 MSPS | $t_{EL}$ | Full | | 6.25 | | ns |
| Clock Pulse Width High at 40 MSPS | $t_{EH}$ | Full | | 12.5 | | ns |
| Clock Pulse Width Low at 40 MSPS | $t_{EL}$ | Full | | 12.5 | | ns |
| OUTPUT PARAMETERS | | | | | | |
| Propagation Delay at 80 MSPS | $t_{PD}$ | Full | | 6 | | ns |
| Rise Time | $t_R$ | Full | | 1.9 | | ns |
| Fall Time | $t_F$ | Full | | 1.2 | | ns |
| Data Setup Time at 80 MSPS | $t_{DS}$ | Full | | 6.2 | | ns |
| Data Hold Time at 80 MSPS | $t_{DH}$ | Full | | 6.0 | | ns |
| Data Setup Time at 40 MSPS | $t_{DS}$ | Full | | 18 | | ns |
| Data Hold Time at 40 MSPS | $t_{DH}$ | Full | | 6 | | ns |
| Pipeline Latency | | Full | | 7 | | Clock cycles |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and testing methodology.

### *Timing and Switching Diagram*

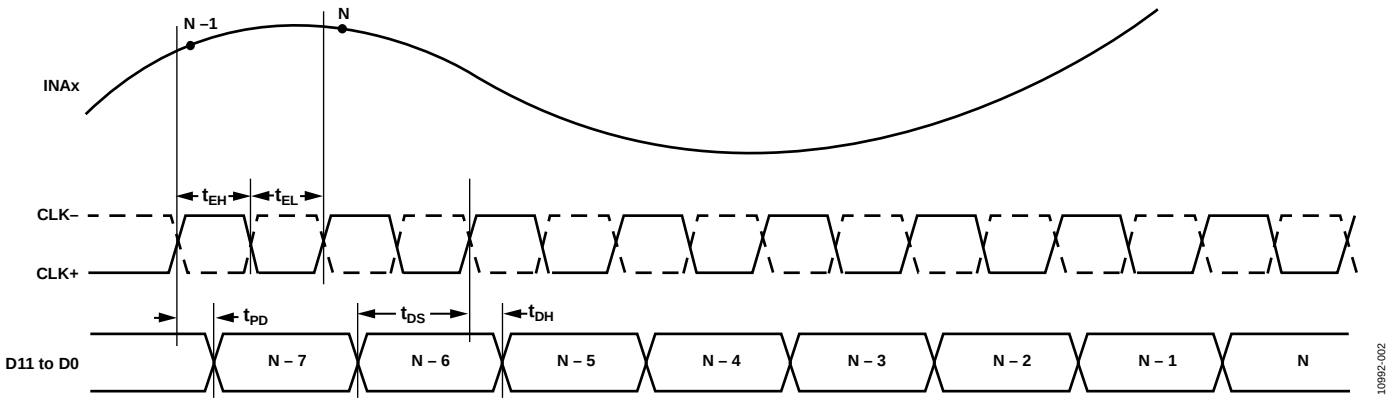



*Figure 2. Timing Definitions for Switching Specifications*

## ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| Electrical | |
| AVDD18, AVDD18 ADC to AGND | −0.3 V to +2.0 V |
| AVDD33, AVDD33REF to AGND | −0.3 V to +3.9 V |
| DVDD18, DVDD18CLK to AGND | −0.3 V to +2.0 V |
| DVDD33CLK, DVDD33DRV, and DVDD33SPI to AGND | −0.3 V to +3.9 V |
| Analog Inputs | |
| INx+, INx− to AGND | −0.3 V to +3.9 V |
| Auxiliary Inputs | |
| INADC+, INADC− to AGND | −0.3 V to +2.0 V |
| Digital Outputs (D11 to D0, SDO) and SDI to AGND | −0.3 V to +3.9 V |
| CLK+, CLK− to AGND | −0.3 V to +3.9 V |
| PDWN, SCLK, $\overline{CS}$, AUX, ZSEL to AGND | −0.3 V to +3.9 V |
| RBIAS, VREF to AGND | −0.3 V to +2.0 V |
| Environmental | |
| Operating Temperature Range (Ambient) | −40°C to +105°C |
| Storage Temperature Range (Ambient) | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

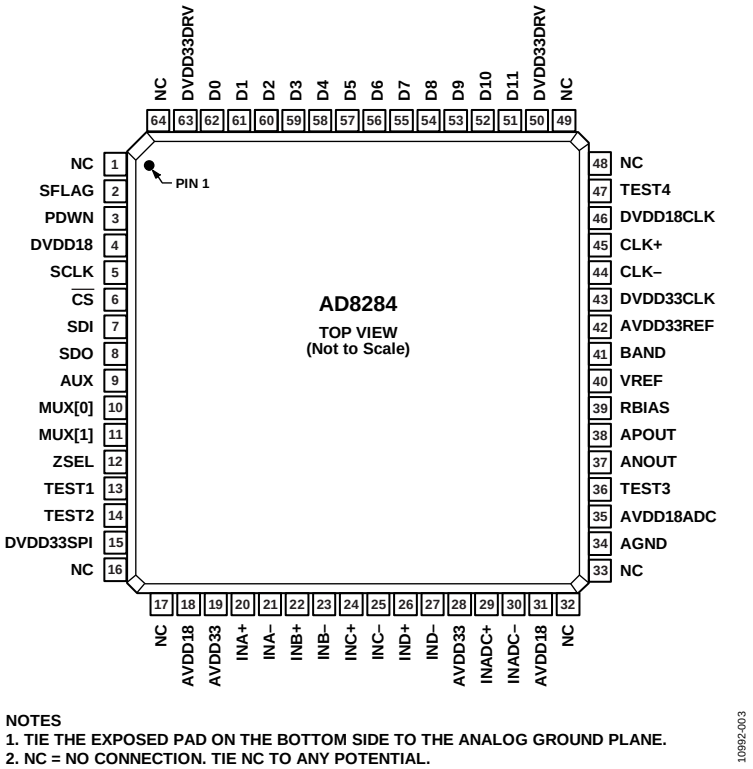



*Figure 3. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | NC | No Connection. Tie NC to any potential. |
| 2 | SFLAG | Saturation Flag. |
| 3 | PDWN | Full Power-Down. A logic high on PDWN overrides the SPI and powers down the part; a logic low allows selection through the SPI. |
| 4 | DVDD18 | 1.8 V Digital Supply. |
| 5 | SCLK | Serial Clock. |
| 6 | $\overline{CS}$ | Chip Select. |
| 7 | SDI | Serial Data Input. |
| 8 | SDO | Serial Data Output. |
| 9 | AUX | Auxiliary Channel. A logic high on AUX switches the AUX channel to ADC (INADC+/INADC–). |
| 10 | MUX[0] | Digital Control for Mux Channel Selection. |
| 11 | MUX[1] | Digital Control for Mux Channel Selection. |
| 12 | ZSEL | Input Impedance Select. A logic high on ZSEL overrides the SPI and sets the input impedance to 200 kΩ; a logic low allows selection through the SPI. |
| 13 | TEST1 | Test. Do not use the TEST1 pin; tie TEST1 to ground. |
| 14 | TEST2 | Test. Do not use the TEST2 pin; tie TEST2 to ground. |
| 15 | DVDD33SPI | 3.3 V Digital Supply, SPI Port. |
| 16 | NC | No Connection. Tie NC to any potential. |
| 17 | NC | No Connection. Tie NC to any potential. |
| 18 | AVDD18 | 1.8 V Analog Supply. |
| 19 | AVDD33 | 3.3 V Analog Supply. |
| 20 | INA+ | Positive Mux Analog Input for Channel A. |
| 21 | INA– | Negative Mux Analog Input for Channel A. |
| 22 | INB+ | Positive Mux Analog Input for Channel B. |
| 23 | INB– | Negative Mux Analog Input for Channel B. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 24 | INC+ | Positive Mux Analog Input for Channel C. |
| 25 | INC− | Negative Mux Analog Input for Channel C. |
| 26 | IND+ | Positive Mux Analog Input for Channel D. |
| 27 | IND− | Negative Mux Analog Input for Channel D. |
| 28 | AVDD33 | 3.3 V Analog Supply. |
| 29 | INADC+ | Positive Analog Input for Alternate Channel (ADC Only). |
| 30 | INADC− | Negative Analog Input for Alternate Channel (ADC Only). |
| 31 | AVDD18 | 1.8 V Analog Supply. |
| 32 | NC | No Connection. Tie NC to any potential. |
| 33 | NC | No Connection. Tie NC to any potential. |
| 34 | AGND | Ground. |
| 35 | AVDD18ADC | 1.8 V Analog Supply. |
| 36 | TEST3 | Test. Do not use the TEST3 pin; tie TEST3 to ground. |
| 37 | ANOUT | Analog Output. ANOUT is for debug purposes only. Leave ANOUT floating. |
| 38 | APOUT | Analog Output. APOUT is for debug purposes only. Leave APOUT floating. |
| 39 | RBIAS | External Resistor. The RBIAS pin sets the internal ADC core bias current. |
| 40 | VREF | Voltage Reference Input/Output. |
| 41 | BAND | Band Gap Voltage. BAND is for debug purposes only. Leave BAND floating. |
| 42 | AVDD33REF | 3.3 V Analog Supply. |
| 43 | DVDD33CLK | 3.3 V Digital Supply. |
| 44 | CLK− | Clock Input Complement. |
| 45 | CLK+ | Clock Input True. |
| 46 | DVDD18CLK | 1.8 V Digital Supply. |
| 47 | TEST4 | Test. Do not use the TEST4 pin; tie TEST4 to ground. |
| 48 | NC | No Connection. Tie NC to any potential. |
| 49 | NC | No Connection. Tie NC to any potential. |
| 50 | DVDD33DRV | 3.3 V Digital Supply. |
| 51 | D11 | ADC Data Output (MSB). |
| 52 | D10 | ADC Data Output. |
| 53 | D9 | ADC Data Output. |
| 54 | D8 | ADC Data Output. |
| 55 | D7 | ADC Data Output. |
| 56 | D6 | ADC Data Output. |
| 57 | D5 | ADC Data Output. |
| 58 | D4 | ADC Data Output. |
| 59 | D3 | ADC Data Output. |
| 60 | D2 | ADC Data Output. |
| 61 | D1 | ADC Data Output. |
| 62 | D0 | ADC Data Output (LSB). |
| 63 | DVDD33DRV | 3.3 V Digital Supply. |
| 64 | NC | No Connection. Tie NC to any potential. |
|  | EP | Exposed Pad. Tie the exposed pad on the bottom side to the analog ground plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD18x = 1.8 V, AVDD33x = 3.3 V, $T_A$ = 25°C, $f_S$ = 80 MSPS, $R_{IN}$ = 200 kΩ, $V_{REF}$ = 1.0 V.

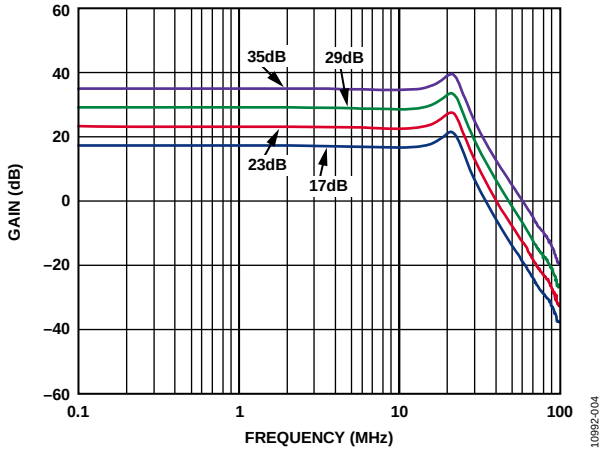



Figure 4. Channel Gain vs. Frequency

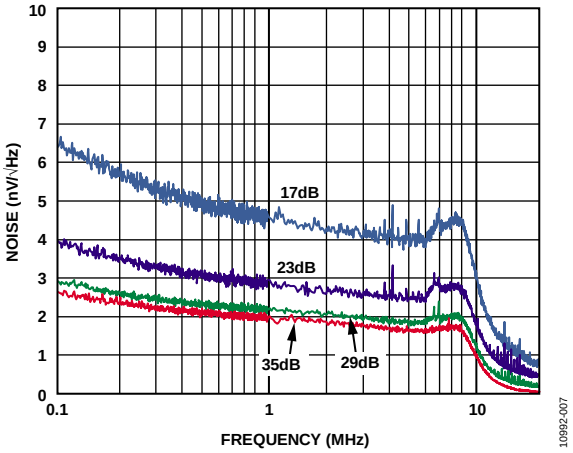



Figure 7. Short-Circuit Input Referred Noise vs. Frequency

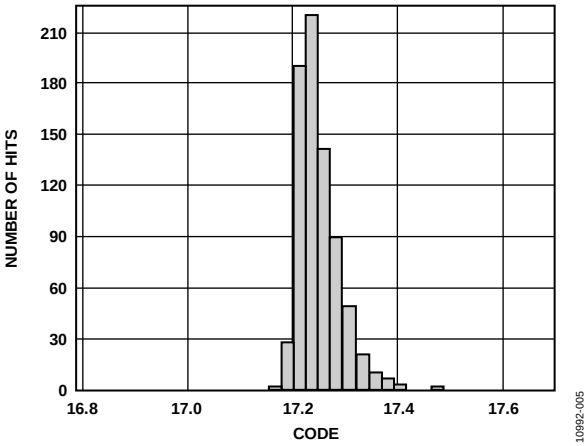



Figure 5. Gain Histogram (Gain = 17 dB)

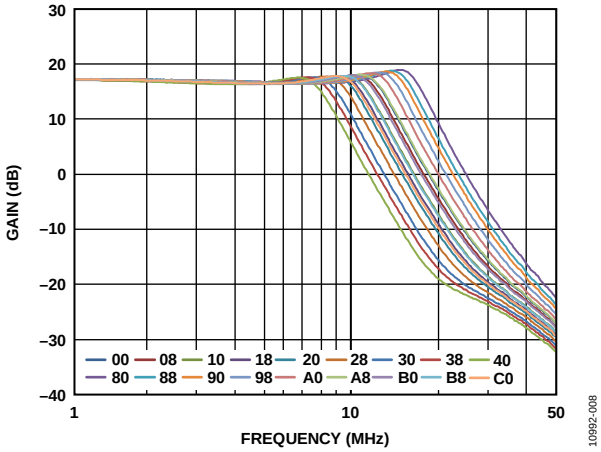



Figure 8. Filter Frequency Response

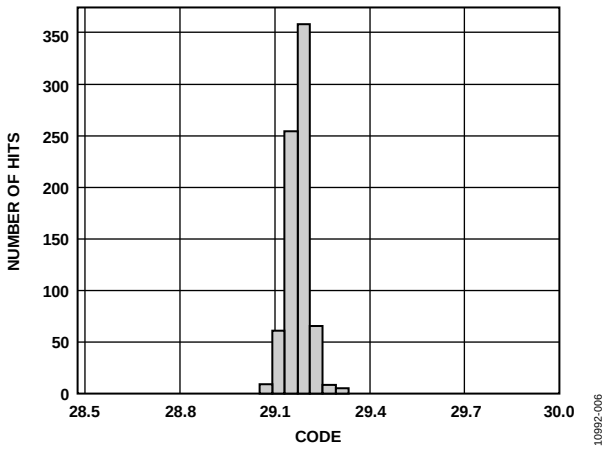



Figure 6. Gain Histogram (Gain = 29 dB)

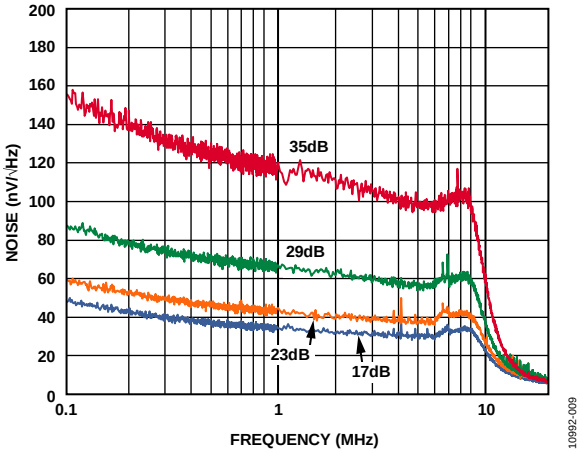



Figure 9. Short-Circuit Output Referred Noise vs. Frequency

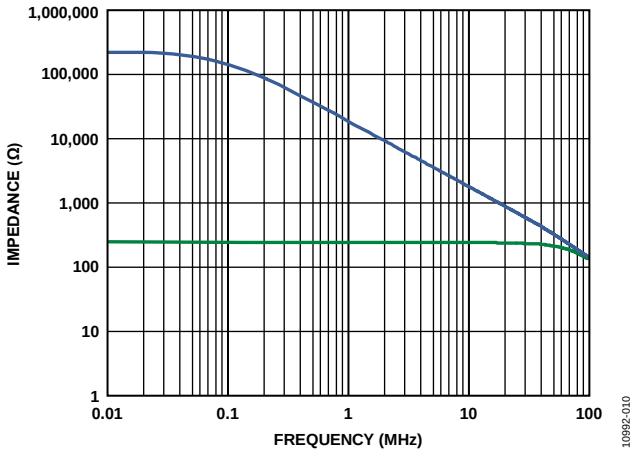



Figure 10. $R_{IN}$ vs. Frequency

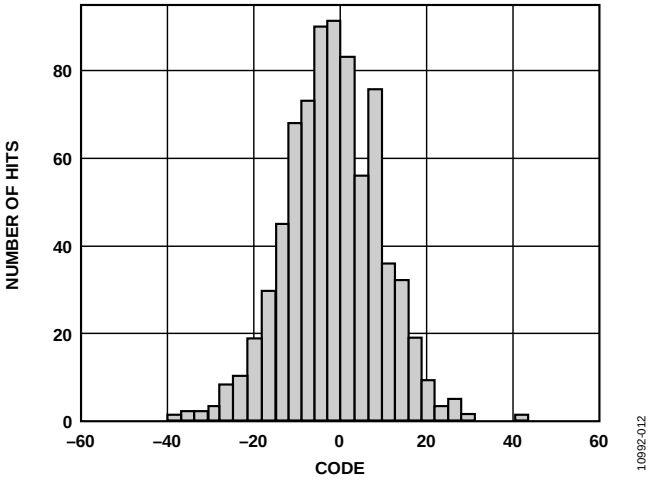



Figure 12. Channel Offset Distribution (Gain = 17 dB)

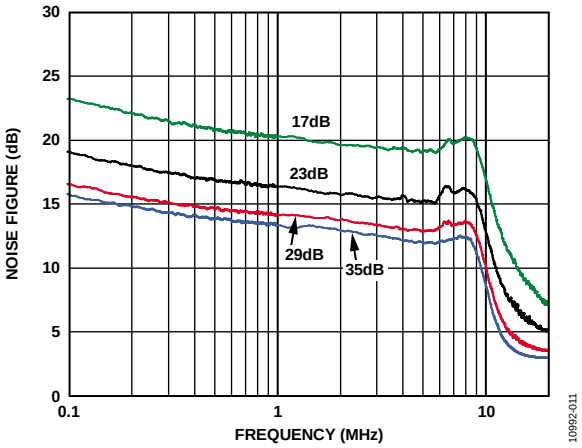



Figure 11. Noise Figure vs. Frequency

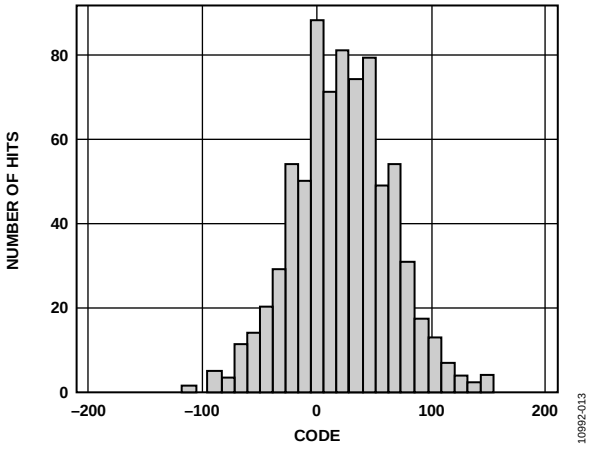



Figure 13. Channel Offset Distribution (Gain = 35 dB)

# THEORY OF OPERATION

## RADAR RECEIVE PATH AFE

The primary application for the AD8284 is high speed ramp, frequency modulated, continuous wave (HSR-FMCW) radar requiring baseband signal bandwidths of up to 15 MHz. Figure 14 shows a simplified block diagram of an HSR-FMCW radar system.

The signal chain requires multiple channels, each of which is routed into a low noise amplifier (LNA), a programmable gain amplifier (PGA), an antialiasing filter (AAF), and an analog-to-digital converter (ADC). The AD8284 provides all of these key components in a single 10 mm × 10 mm TQFP package.

The performance of each component is designed to meet the demands of an HSR-FMCW radar system. Some examples of these performance metrics include the LNA noise, PGA gain range, AAF cutoff characteristics, and ADC sample rate and resolution.

The AD8284 includes a multiplexer (mux) in front of the analog signal chain as a cost-saving alternative to having an AFE for each channel. The mux can be switched between active inputs using the mux pins or through the SPI port.

The AD8284 also includes a saturation detection circuit that indicates when the LNA or PGA signals are no longer in the linear region. This feature helps detect fault conditions that might otherwise be filtered out by the AAF.

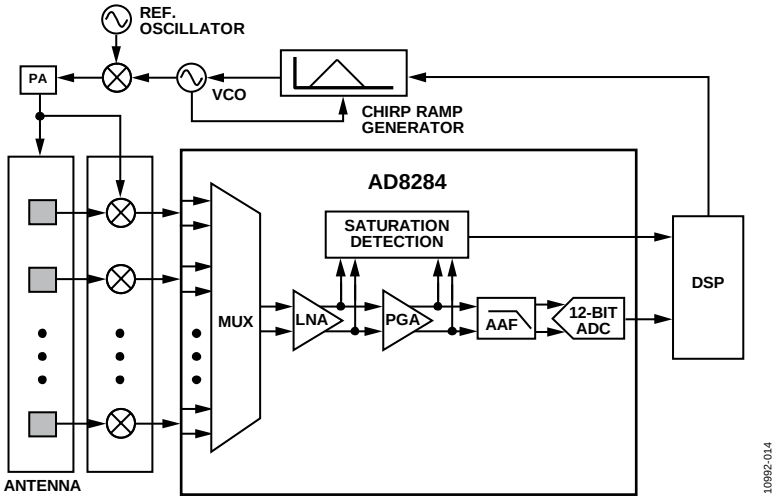



*Figure 14. Simplified Block Diagram, HSR-FMCW Radar System*

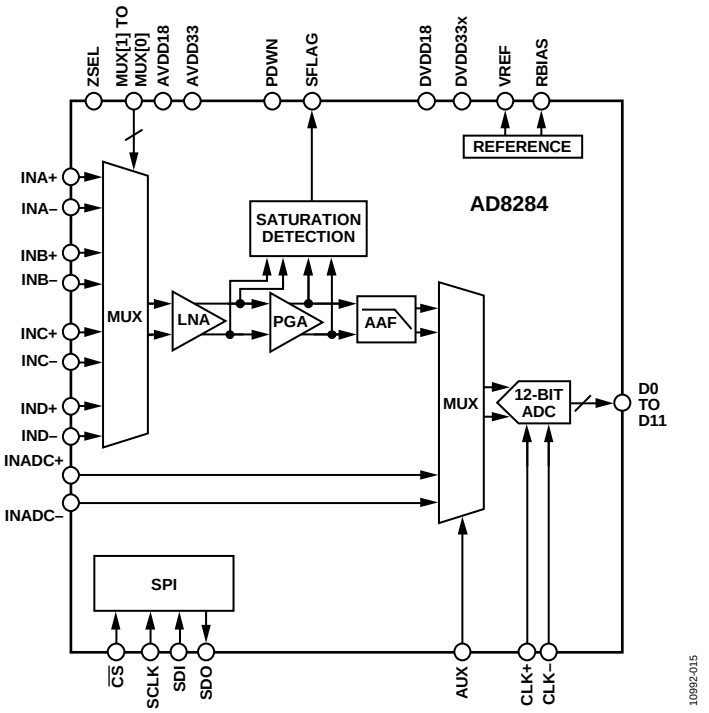



*Figure 15. Simplified Block Diagram*

## CHANNEL OVERVIEW

The AD8284 contains a four-input mux, an LNA, a PGA, and an AAF in the signal path, as shown in Figure 15. The signal chain input impedance can be either 200 Ω or 200 kΩ. The PGA has selectable gains that result in channel gains ranging from 17 dB to 35 dB. The AAF has a three-pole elliptical response with a selectable cutoff frequency from 9 MHz to 15 MHz. The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion. The LNA is designed to be driven from either a differential or single-ended signal source.

### *Multiplexer*

The AD8284 has a multiplexer (mux) at the input to switch as many as four differential channels into the signal chain. The active mux channel is controlled by the SPI port or by using the external pins, MUX[0] and MUX[1]. The relationship between the input code and the selected mux channel is listed in Table 6.

**Table 6. Digital Input Values to Select the Active ADC Channel**

| AUX | MUX[1] | MUX[0] | Active Channel |
|---|---|---|---|
| 1 | X | X | AUX |
| 0 | 0 | 0 | A |
| 0 | 0 | 1 | B |
| 0 | 1 | 0 | C |
| 0 | 1 | 1 | D |

The external pins are the default method for selecting the active mux channel but the SPI Register 0x0C can also control the mux. Bit 3 of Register 0x0C specifies whether the SPI or the external pins control the mux.

### *Low Noise Amplifier*

Good noise performance relies on a proprietary ultralow noise LNA at the beginning of the signal chain; the LNA minimizes the noise contributions from the PGA and AAF that are next in the signal chain. The input impedance can be either 200 Ω or 200 kΩ, the value of which is selected through the SPI port or by the ZSEL pin.

The LNA supports differential output voltages as high as 5.0 V p-p with positive and negative excursions of ±1.25 V from a common-mode voltage of 1.5 V. Because the output saturation level is fixed, the channel gain sets the maximum input signal before saturation.

Low value feedback resistors and the current driving capability of the output stage allow the LNA to achieve a low input referred noise voltage of 3.5 nV/√Hz at a channel gain of 35 dB. The use of a fully differential topology and negative feedback minimizes second-order distortion. Differential signaling enables smaller swings at each output, further reducing third-order distortion.

#### Recommendation

To achieve the best possible noise performance, it is important to match the impedances seen by the positive and negative inputs. Matching the impedances ensures that the signal path rejects any common-mode noise.

### *Antialiasing Filter*

The AAF uses a combination of poles and zeros to create a third-order elliptic filter. An elliptic filter is used to achieve a sharp roll-off after the cutoff frequency. This architecture achieves a −30 dB per octave roll-off in the first octave after the cutoff frequency.

The filter uses on-chip tuning to trim the internal resistors and capacitors to set the desired cutoff frequency. The tuning method reduces variations in the cutoff frequency due to standard IC process tolerances of resistors and capacitors.

The default tuning settings for a −3 dB low-pass filter cutoff is 1/3 × 1.125 × the ADC sample clock frequency. This setting can be changed to 1/4 the ADC sample clock frequency. The cutoff can also be scaled from 0.75 to 1.25 (in 0.0625 increments) times these frequencies through the SPI.

Tuning is normally off and is initiated by the user via the SPI port. After the filter is tuned to a specific frequency, it remains at that frequency until another tuning sequence is initiated. The tuning process can take up to 2048 clock cycles.

The filter defaults to its highest frequency setting before it is tuned. To maintain the expected ratio of clock frequency to cutoff frequency, tune the filter after initial power-up, after reprogramming the filter cutoff scaling via the SPI, or after changing the ADC sample rate. Occasional retuning during an idle time is recommended to compensate for temperature drift.

A cutoff frequency range of 9 MHz to 15 MHz is possible, for example

- ADC clock: 40 MHz
- Default tuned cutoff frequency = (40 MHz ÷ 3) × 1.125 = 15 MHz

The autotune cycle takes several clock cycles to complete. During this time, the mux channels, A to D, are not operational; however, the AUX input can be used during the autotuning cycle.

### *Saturation Flag*

The saturation flag function detects overvoltage conditions that may push the LNA or PGA out of their linear regions. The flag is set when the PGA output voltage exceeds 2.0 V p-p or the LNA output voltage exceeds 4.0 V p-p. This function is particularly useful for detecting saturation events that may be filtered out by the AAF and are, therefore, undetectable by monitoring the ADC output.

When the saturation flag trips, it remains on for a minimum of 25 ns after the saturation event has ended.

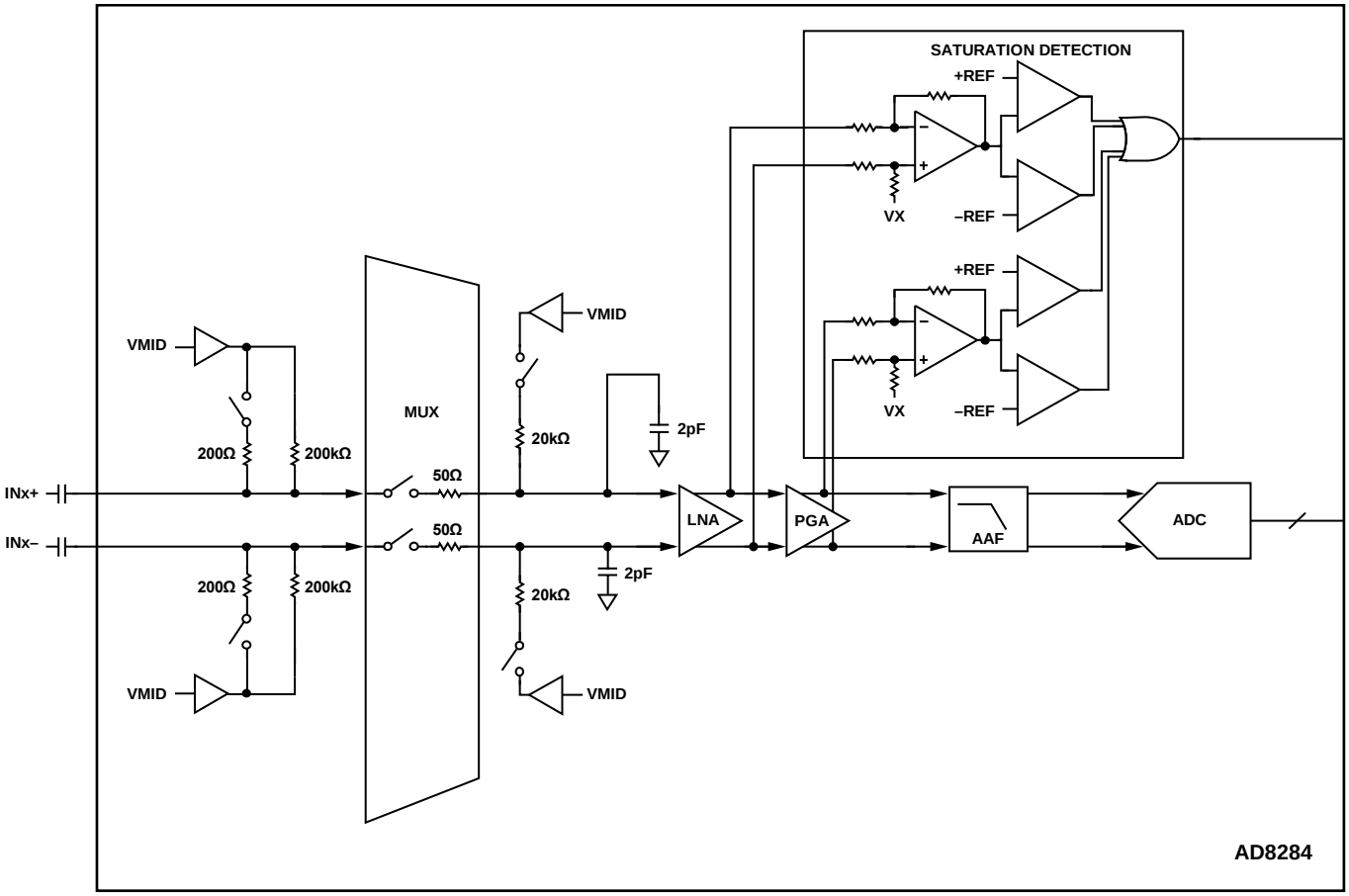



*Figure 16. Simplified Block Diagram of the Analog Channel*

## ADC

The AD8284 uses a pipelined ADC architecture. The quantized output from each stage is combined into a 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock. The output staging block aligns the data and passes the data to the output buffers.

## AUX CHANNEL

The AD8284 allows direct access to the ADC when the mux settings are used to select the AUX channel. When this channel is selected, the inputs of the ADC can be accessed using the INADC+ and INADC– pins. To ensure enough headroom for full-scale, differential, 2.0 V p-p input signals, bias the INADC± pins with a 0.9 V common-mode voltage.

## CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD8284 sample clock inputs (CLK+ and CLK–) with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or by using capacitors; these pins are biased internally and require no additional bias.

Figure 17 shows the preferred method for clocking the AD8284. A low jitter clock source, such as the Valpey Fisher oscillator, VFAC3-BHL (50 MHz), is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD8284 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD8284 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

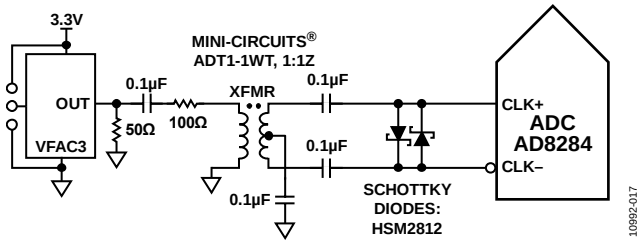



*Figure 17. Transformer-Coupled Differential Clock*

If a low jitter clock is available, another option is to ac-couple a differential PECL or LVDS signal to the sample clock input pins as shown in Figure 18 and Figure 19. The AD951x/AD952x family of clock drivers offers excellent jitter performance.

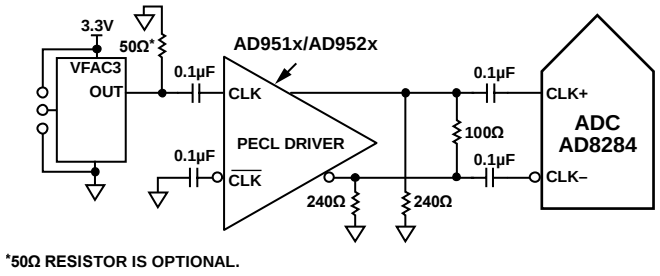



*Figure 18. Differential PECL Sample Clock*

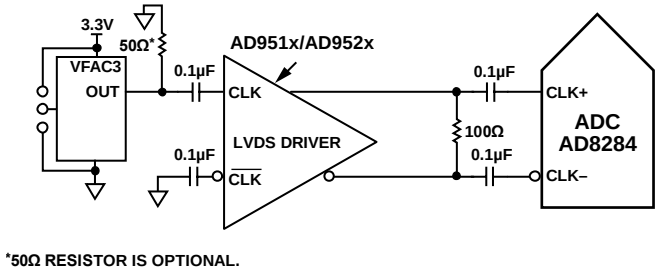



*Figure 19. Differential LVDS Sample Clock*

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, drive CLK+ directly from a CMOS gate, and bypass the CLK– pin to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 20). Although the CLK+ input circuit supply is via Pin 46, DVDD18CLK, this input is designed to withstand input voltages of up to 3.3 V, making the selection of the logic voltage of the driver very flexible. The AD951x/AD952x family of parts can be used to provide 3.3 V inputs (see Figure 21). In this case, the 39 kΩ resistor is not needed.

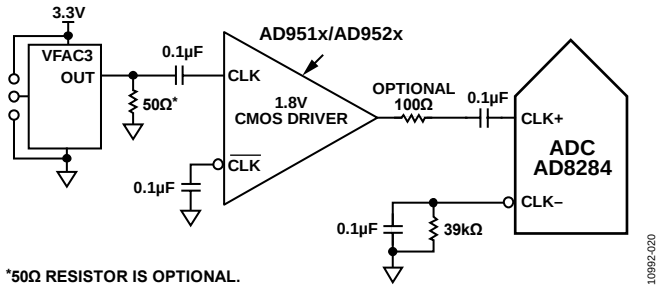



*Figure 20. Single-Ended 1.8 V CMOS Sample Clock*

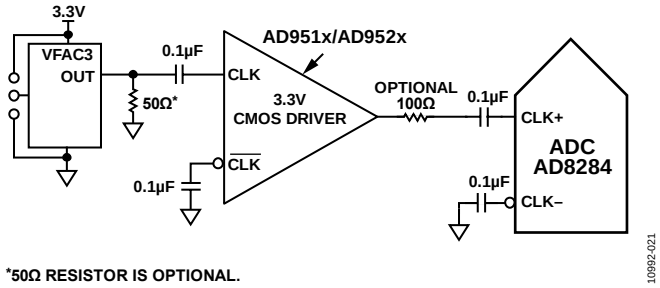



*Figure 21. Single-Ended 3.3 V CMOS Sample Clock*

## CLOCK DUTY CYCLE CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD8284 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD8284.

When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, note that the dynamic range performance can be affected when operating in this mode. See Table 9 for more details on using this feature.

The duty cycle stabilizer uses a delay locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

## CLOCK JITTER CONSIDERATIONS

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency ($f_A$) due only to aperture jitter ($t_J$) can be calculated by

$$SNR\ Degradation = 20 \times \log 10[1/2 \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter.

In cases where aperture jitter may affect the dynamic range of the AD8284, treat the clock input as an analog signal. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources, such as the Valpey Fisher VFAC3 series. If the clock is generated from another type of source by using the sequential steps of gating, dividing, or other methods, it should be retimed by the original clock during the last step in that sequence.

See the AN-501 Application Note and the AN-756 Application Note for more information about how jitter performance relates to ADCs.

## SDI AND SDO PINS

The SDI and SDO pins are required to operate the SPI. The SDI pin has an internal 30 kΩ pull-down resistor that pulls this pin low and is 1.8 V and 3.3 V tolerant. The SDO output pin is 3.3 V logic.

## SCLK PIN

The SCLK pin is required to operate the SPI. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is both 1.8 V and 3.3 V tolerant.

## $\overline{CS}$ PIN

The $\overline{CS}$ pin is required to operate the SPI. It has an internal 70 kΩ pull-up resistor that pulls this pin high and is both 1.8 V and 3.3 V tolerant.

## RBIAS PIN

To set the internal core bias current of the ADC, place a resistor nominally equal to 10.0 kΩ to ground at the RBIAS pin. Using a resistor other than the recommended 10.0 kΩ resistor for RBIAS degrades the performance of the device. Therefore, it is imperative that at least a 1.0% tolerance on this resistor be used to achieve consistent performance.

## VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD8284. This is gained up internally by a factor of 2, setting $V_{REF}$ to 1.0 V, which results in a full-scale differential input span of 2.0 V p-p for the ADC. $V_{REF}$ is set internally by default, but the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy. However, the AD8284 is not specified for ADC full-scale ranges below 2.0 V p-p.

When applying decoupling capacitors to the VREF pin, use ceramic, low ESR capacitors. Place these capacitors close to the reference pin and on the same layer of the PCB as the AD8284. The VREF pin should have both a 0.1 µF capacitor and a 1 µF capacitor connected in parallel to the analog ground. These capacitor values are recommended for the ADC to properly settle and acquire the next valid sample.

## POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD8284, it is recommended that two separate 1.8 V supplies and two separate 3.3 V supplies be used: one supply each for analog 1.8 V (AVDD18x), digital 1.8 V (DVDD18x), analog 3.3 V (AVDD33x), and digital 3.3 V (DVDD33x). If only one supply is available for both analog and digital, for example, AVDD18x and DVDD18x, route the supply to AVDD18x first and then tap the supply off and isolate it with a ferrite bead or a filter choke preceded by decoupling capacitors for the DVDD18x. The same method is used for the analog and digital 3.3 V supplies. Use several decoupling capacitors on all supplies to cover both high and low frequencies. Locate these capacitors close to the point of entry at the printed circuit board (PCB) level and close to the AD8284 using minimal trace lengths.

The 12 power supply pins are separated into four power supply domains, AVDD18, AVDD33, DVDD18, and DVDD33. Each pin within a domain must be powered simultaneously, but each domain can be turned on independently of the other domains.

A single PCB ground plane should be sufficient when using the AD8284. With proper decoupling and smart partitioning of the analog, digital, and clock sections of the PCB, optimum performance can be easily achieved.

## EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the device be connected to a quiet analog ground to achieve the best electrical and thermal performance of the AD8284. Mate an exposed continuous copper plane on the PCB to the AD8284 exposed pad, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB.

To maximize the coverage and adhesion between the device and the PCB, it is recommended that the continuous copper pad be partitioned by overlaying a silkscreen or solder mask to divide the copper pad into uniform sections. This partitioning helps to ensure several tie points between the PCB and the device during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the AD8284 and the PCB. For more information about packaging and for additional PCB layout examples, see the AN-772 Application Note.

# SERIAL PORT INTERFACE (SPI)

The AD8284 serial port interface allows the user to configure the signal chain for specific functions or operations through a structured register space provided inside the chip. The SPI offers the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Four pins define the serial port interface, or SPI: the SCLK, SDI, SDO, and $\overline{CS}$ pins. The serial clock pin (SCLK) synchronizes the read and write data presented to the device. The serial data input and output pins, SDI and SDO, allow data to be sent to and read from the internal memory map registers of the device. The chip select pin ($\overline{CS}$) is an active low control that enables or disables the read and write cycles (see Table 7).

**Table 7. Serial Port Interface Pins**

| Pin | Function |
|---|---|
| SCLK | Serial clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes. |
| SDI | Serial data input. |
| SDO | Serial data output. |
| $\overline{CS}$ | Chip select (active low). This control gates the read and write cycles. |

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. See Figure 22 and Table 8 for an example of the serial timing and its definitions.

In normal operation, $\overline{CS}$ signals to the device that SPI commands are about to be received and processed. When $\overline{CS}$ is brought low, the device processes SCLK and SDI to process instructions. Normally, $\overline{CS}$ remains low until the communication cycle is complete. However, if the AD8284 is connected to a slow device, $\overline{CS}$ can be brought high between bytes, allowing older microcontrollers enough time to transfer data into the shift registers. $\overline{CS}$ can be stalled when transferring one, two, or three bytes of data.

When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until $\overline{CS}$ is taken high to end the communication cycle. This allows complete memory transfers without the need to provide additional instructions. Regardless of the mode, if $\overline{CS}$ is taken high in the middle of any byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different manners. For applications that do not require a control port, the $\overline{CS}$ line can be tied and held high. This places the remainder of the SPI pins in their secondary mode as defined in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. $\overline{CS}$ can also be tied low to enable 3-wire mode. When $\overline{CS}$ is tied low, SCLK, SDO, and SDI are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the $\overline{CS}$ line. When operating in 3-wire mode, it is recommended that a a 1-, 2-, or 3-byte transfer be used exclusively. Without an active $\overline{CS}$ line, streaming mode can be entered but not exited.

Data can be sent in MSB-first or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

## HARDWARE INTERFACE

The pins described in Table 7 constitute the physical interface between the user's programming device and the serial port of the AD8284. The SCLK, SDI, and $\overline{CS}$ pins function as inputs when using the SPI interface. The SDO pin is an output during readback.

This interface is flexible enough to be controlled by either serial-programmable read-only memory (PROM) or PIC micro-controllers. This provides the user with alternative means, other than a full SPI controller, for programming the device (see the AN-812 Application Note).

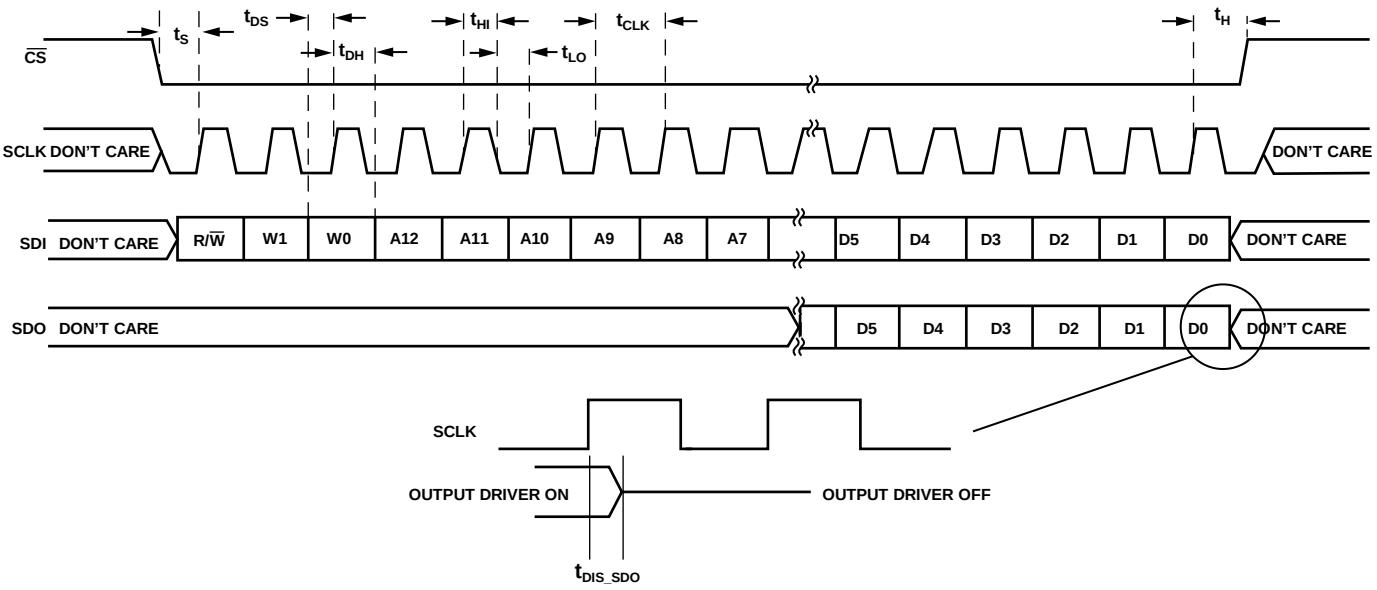



*Figure 22. Serial Timing Details*

**Table 8. Serial Timing Definitions**

| Parameter | Minimum Timing (ns) | Description |
|---|---|---|
| $t_{DS}$ | 5 | Setup time between the data and the rising edge of SCLK. |
| $t_{DH}$ | 2 | Hold time between the data and the rising edge of SCLK. |
| $t_{CLK}$ | 40 | Period of the clock. |
| $t_S$ | 5 | Setup time between $\overline{CS}$ and SCLK. |
| $t_H$ | 2 | Hold time between $\overline{CS}$ and SCLK. |
| $t_{HI}$ | 16 | Minimum period that SCLK should be in a logic high state. |
| $t_{LO}$ | 16 | Minimum period that SCLK should be in a logic low state. |
| $t_{DIS\_SDO}$ | 10 | Minimum time it takes the SDO pin to switch between an output and a high impedance node, relative to the rising edge of SCLK. |

# MEMORY MAP

## READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: the chip configuration registers map (Address 0x00 and Address 0x01), the device index and transfer registers map (Address 0x04 to Address 0xFF), and the ADC channel functions registers map (Address 0x08 to Address 0x2C).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second rightmost column.

The Bit 7 (MSB) column is the start of the default hexadecimal value that is given. For example, Address 0x09, the GLOBAL_CLOCK register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address followed by writing 0x01 to the SW transfer bit in Register 0xFF, the duty cycle stabilizer is turned off. It is important to follow each writing sequence with a write to the SW transfer bit to update the SPI registers.

**Caution**

All registers except for Register 0x00 and Register 0xFF are buffered with a master slave latch and require writing to the transfer bit. For more information about this and other functions, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

## LOGIC LEVELS

An explanation of various registers follows: "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "bit is cleared" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit.

## RESERVED LOCATIONS

Do not write to undefined memory except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

## DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 9, where an X refers to an undefined feature.

**Table 9. Memory Map Registers[1]**

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Chip Configuration Registers | | | | | | | | | | | |
| 0x00 | CHIP_PORT_CONFIG | 0 | LSB first 1 = on 0 = off (default) | Soft reset 1 = on 0 = off (default) | 1 | 1 | Soft reset 1 = on 0 = off (default) | LSB first 1 = on 0 = off (default) | 0 | 0x18 | Mirror the nibbles to correctly set LSB-first or MSB-first mode, regardless of shift mode. |
| 0x01 | CHIP_ID | Chip ID Bits[7:0] (AD8284 = 0xAA, default) | | | | | | | | Read only | The default is a unique chip ID, specific to the AD8284. This is a read-only register. |
| Device Index and Transfer Registers | | | | | | | | | | | |
| 0xFF | DEVICE_UPDATE | X | X | X | X | X | X | X | SW transfer 1 = on 0 = off (default) | 0x00 | Synchronously transfers data from the master shift register to the slave. |
| Channel Functions Registers | | | | | | | | | | | |
| 0x08 | GLOBAL_MODES | Channel A buffer power 0 = power off 1 = power on (default) | Channel B buffer power 0 = power off 1 = power on (default) | Channel C buffer power 0 = power off 1 = power on (default) | Channel D buffer power 0 = power off 1 = power on (default) | Channel power-down 0 = power on (default) 1 = power off | X | Internal power-down mode 00 = chip run (default) 01 = full power-down 11 = reset | | 0xF0 | Determines the power-down mode (global). |
| 0x09 | GLOBAL_CLOCK | X | X | X | X | X | X | X | Duty cycle stabilizer 1 = on (default) 0 = off | 0x01 | Turns the internal duty cycle stabilizer on and off (global). |
| 0x0C | FLEX_MUX_CONTROL | X | Power down unused channels 0 = PD power-down (default) 1 = power on | X | 0 = signal channel (A, B, C, D) on (default) 1 = AUX channel on | 0 = use external pins (default) 1 = use internal registers | 0 = all channels are off 1= selected channel is on (default) | 00 = Channel A (default) 01 = Channel B 10 = Channel C 11 = Channel D | | 0x04 | Sets which mux input channel is in use and whether to power down unused channels. |
| 0x0D | FLEX_TEST_IO | User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once | | Reset PN long gen 1 = on 0 = off (default) | Reset PN short gen 1 = on 0 = off (default) | Output test mode—see Table 10 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = −FS short 0100 = checkerboard output 0101 = PN sequence long 0110 = PN sequence short 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-bit/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by the OUTPUT_MODE register) | | | | 0x00 | When this register is set, the test data is placed on the output pins in place of normal data. (Local, except for PN sequence.) |

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0E | TEST_REGISTER | Enable analog outputs (APOUT, ANOUT)<br>0x01 = analog output enabled | | | | | | | | 0x00 | Routes the differential output of the AAF to APOUT and ANOUT. |
| 0x0F | FLEX_CHANNEL_INPUT | Filter cutoff frequency control<br>00000 = 1.25 × 1/4 × $f_{SAMPLECH}$<br>00001 = 1.1875 × 1/4 × $f_{SAMPLECH}$<br>00010 = 1.125 × 1/4 × $f_{SAMPLECH}$<br>00011 = 1.0625 × 1/4 × $f_{SAMPLECH}$<br>00100 = 1.0 × 1/4 × $f_{SAMPLECH}$<br>00101 = 0.9375 × 1/4 × $f_{SAMPLECH}$<br>00110 = 0.875 × 1/4 × $f_{SAMPLECH}$<br>00111 = 0.8125 × 1/4 × $f_{SAMPLECH}$<br>01000 = 0.75 × 1/4 × $f_{SAMPLECH}$<br>01001 to 01111 = reserved<br><br>10000 = 1.25 × 1/3 × $f_{SAMPLECH}$<br>10001 = 1.1875 × 1/3 × $f_{SAMPLECH}$<br>10010 = 1.125 × 1/3 × $f_{SAMPLECH}$ (default)<br>10011 = 1.0625 × 1/3 × $f_{SAMPLECH}$<br>10100 = 1.0 × 1/3 × $f_{SAMPLECH}$<br>10101 = 0.9375 × 1/3 × $f_{SAMPLECH}$<br>10110 = 0.875 × 1/3 × $f_{SAMPLECH}$<br>10111 = 0.8125 × 1/3 × $f_{SAMPLECH}$<br>11000 = 0.75 × 1/3 × $f_{SAMPLECH}$<br>11001 to 11111 = reserved | | | | | X | X | X | 0x90 | Low-pass filter cutoff (global). $f_{SAMPLECH}$ = ADC sample rate. Note that the absolute range is limited to 9 MHz to 15 MHz. |
| 0x10 | FLEX_OFFSET | X | X | 6-bit LNA offset adjustment<br>00 0000 for LNA offset low<br>10 0000 for LNA offset mid (default)<br>11 1111 for LNA offset high | | | | | | 0x20 | LNA force offset correction. |
| 0x11 | FLEX_GAIN_1 | X | X | X | X | X | 000 = 17 dB<br>001 = 17 dB<br>010 = 17 dB<br>011 = 23 dB<br>100 = 29 dB (default)<br>101 = 35 dB | | | 0x04 | Total LNA + PGA gain adjustment (local). |
| 0x12 | FLEX_BIAS_CURRENT | X | X | X | X | X | X | LNA bias<br>00 = high (default)<br>01 = mid to high<br>10 = mid to low<br>11 = low | | 0x00 | LNA bias current adjustment (global). |
| 0x14 | FLEX_OUTPUT_MODE | X | X | X | X | X | 1 = output invert (local) | 0 = offset binary<br>1 = twos complement (default) | | 0x01 | Configures the outputs and the format of the data. |
| 0x15 | FLEX_OUTPUT_ADJUST | 0 = enable Data Bits[11:0]<br>1 = disable Data Bits[11:0] | X | X | X | Output drive current<br>0000 = low<br>…<br>1111 = high (default) | | | | 0x0F | Selects output drive strength to limit the noise added to the channels by output switching. |
| 0x18 | FLEX_VREF | X | 0 = internal reference (default)<br>1 = external reference | X | X | X | X | Internal reference adjust<br>00 = 0.625 V<br>01 = 0.750 V<br>10 = 0.875 V<br>11 = 1.000 V (default) | | 0x03 | Select internal reference (recommended default) or external reference (global); adjust internal reference. |
| 0x19 | FLEX_USER_PATT1_LSB | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User defined Pattern 1, LSB. |
| 0x1A | FLEX_USER_PATT1_ MSB | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User defined Pattern 1, MSB. |

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x1B | FLEX_USER_PATT2_LSB | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User defined Pattern 2, LSB. |
| 0x1C | FLEX_USER_PATT2_ MSB | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User defined Pattern 2, MSB. |
| 0x2B | FLEX_FILTER | X | Enable automatic low-pass tuning 1 = on (self clearing) | X | X | X | X | X | X | 0x00 | Enables low-pass filter tuning |
| 0x2C | CH_IN_IMP | Saturation detector limit adjust 000 = 1.90 V p-p at PGA output 011 = 2.00 V p-p at PGA output (default) 111 = 2.15 V p-p at PGA output Other values reserved (001, 010, 100, 101, 110) | | | Satura-tion detect hysteresis 0 = low hysteresis (25 mV nominal at PGA output) (default) 1 = high hysteresis (nominally 60 mV at PGA output) | X | X | X | Input imped-ance 0 = 200 Ω 1 = 200 kΩ (default) | 0x61 | Saturation detector adjustment and input impedance adjustment (global). |

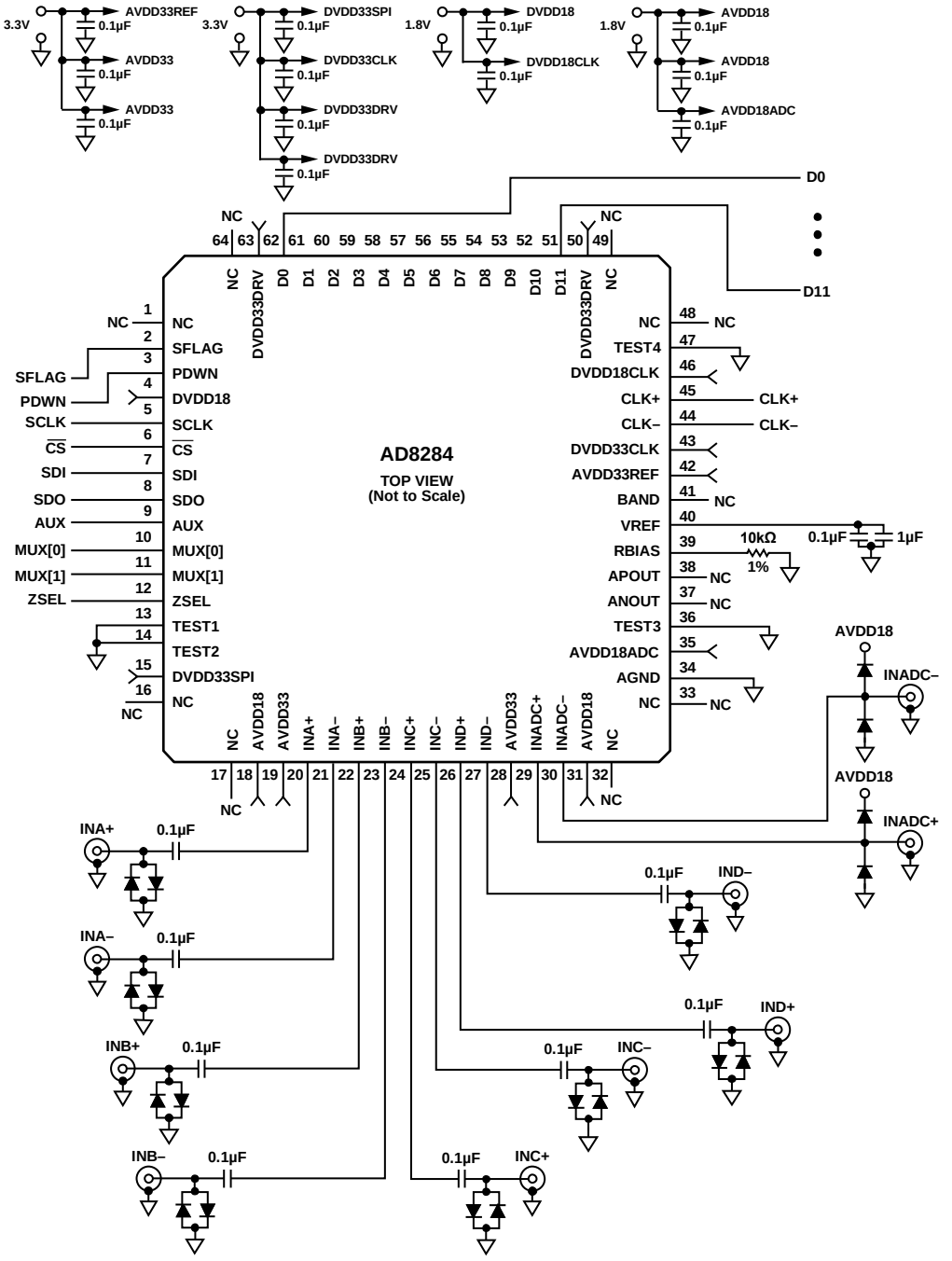
[1] X = undefined feature.

**Table 10. Flexible Output Test Modes[1]**

| Output Test Mode Bit Sequence | Pattern Name | Digital Output Word 1 | Digital Output Word 2 | Subject to Data Format Select |
|---|---|---|---|---|
| 0000 | Off (default) | N/A | N/A | N/A |
| 0001 | Midscale short | 1000 0000 0000 | Same | Yes |
| 0010 | +Full-scale short | 1111 1111 1111 | Same | Yes |
| 0011 | –Full-scale short | 0000 0000 0000 | Same | Yes |
| 0100 | Checkerboard output | 1010 1010 1010 | 0101 0101 0101 | No |
| 0101 | PN sequence long | N/A | N/A | Yes |
| 0110 | PN sequence short | N/A | N/A | Yes |
| 0111 | One-/zero-word toggle | 1111 1111 1111 | 0000 0000 0000 | No |
| 1000 | User input | Register 0x19 and Register 0x1A | Register 0x1B and Register 0x1C | No |
| 1001 | 1-bit/0-bit toggle | 1010 1010 1010 | N/A | No |
| 1010 | 1× sync | 0000 0011 1111 | N/A | No |
| 1011 | One bit high | 1000 0000 0000 | N/A | No |
| 1100 | Mixed bit frequency | 1010 0011 0011 | N/A | No |

[1] N/A means not applicable.

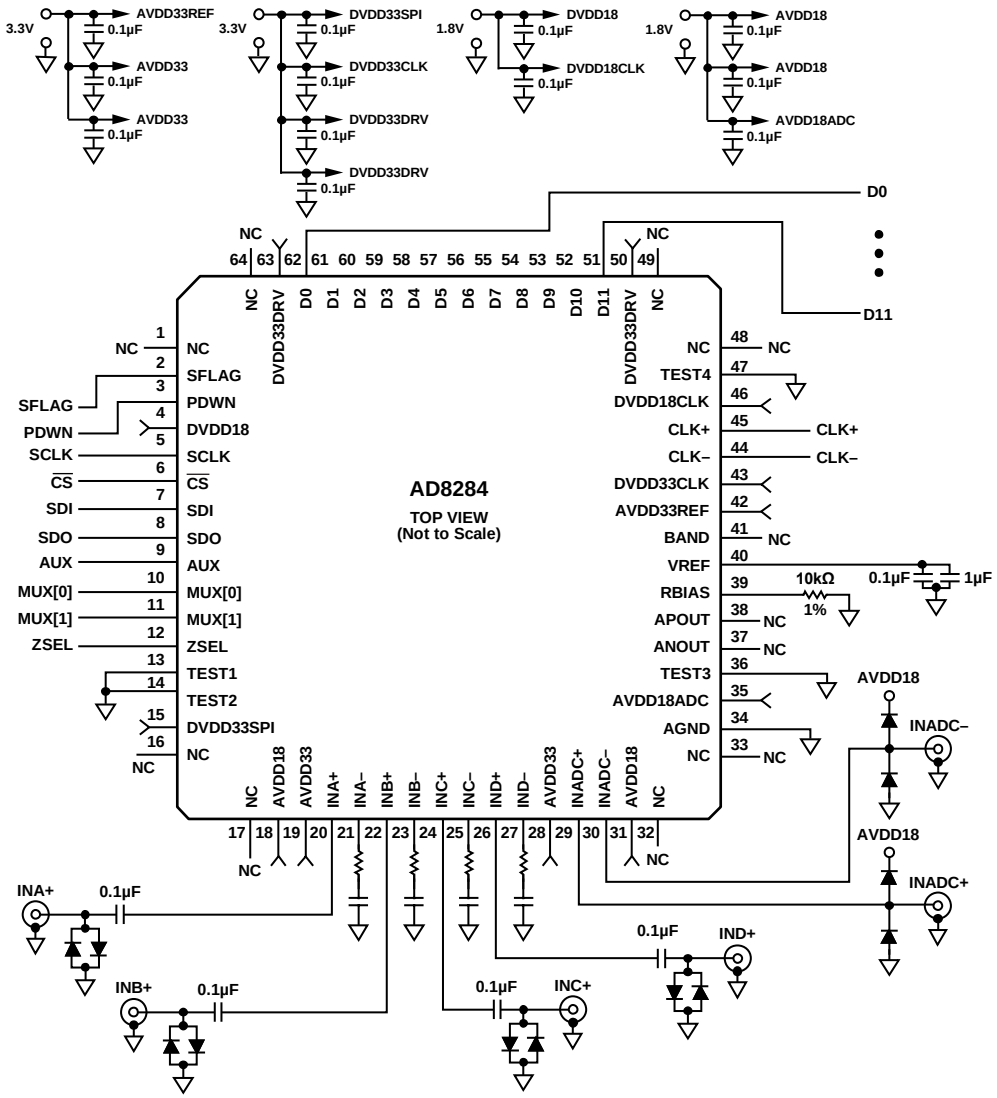
# APPLICATION CIRCUITS




NOTES
1. ALL CAPACITORS FOR SUPPLIES AND REFERENCES SHOULD BE PLACED CLOSE TO THE PART.
2. TIE THE EXPOSED PAD ON THE BOTTOM SIDE TO THE ANALOG GROUND PLANE.

10992-023

*Figure 23. Differential Inputs*




NOTES
1. RESISTOR R (INX– INPUTS) SHOULD MATCH THE OUTPUT IMPEDANCE OF THE INPUT DRIVER.
2. ALL CAPACITORS FOR SUPPLIES AND REFERENCES SHOULD BE PLACED CLOSE TO THE PART.
3. TIE THE EXPOSED PAD ON THE BOTTOM SIDE TO THE ANALOG GROUND PLANE.

10992-024

*Figure 24. Single-Ended Inputs*

# PACKAGING AND ORDERING INFORMATION

## OUTLINE DIMENSIONS

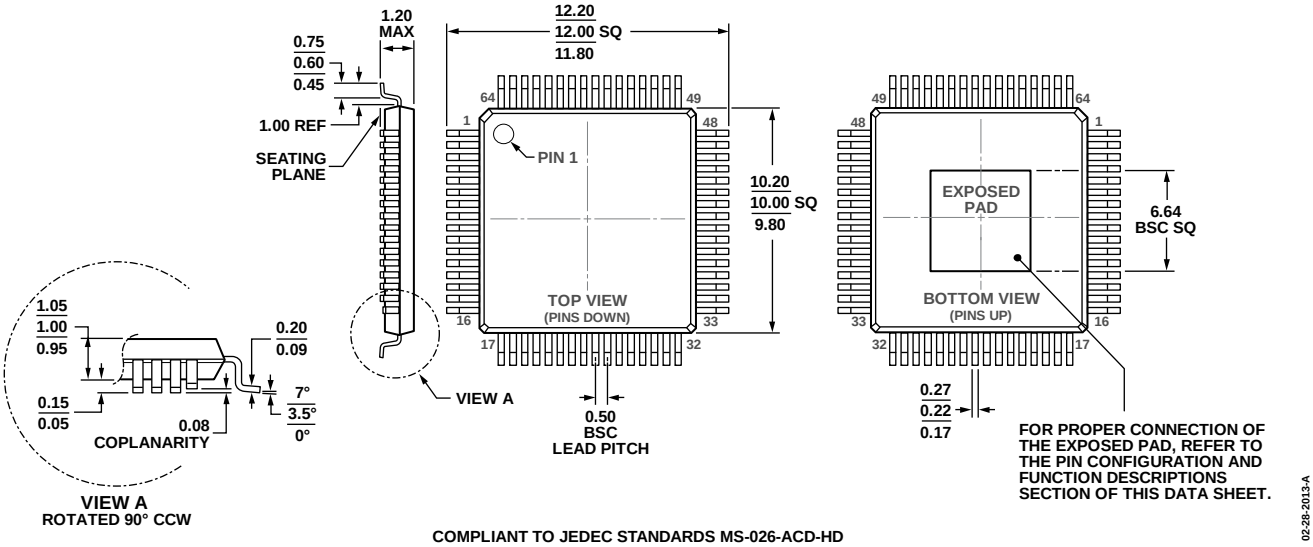



*Figure 25. 64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]*
*(SV-64-5)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2, 3] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD8284WCSVZ | −40°C to +105°C | 64-Lead TQFP_EP, Waffle Pack | SV-64-5 |
| AD8284WCSVZ-RL | −40°C to +105°C | 64-Lead TQFP_EP, 13" Tape and Reel | SV-64-5 |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Compliant to JEDEC Standard MS-026-ACD-HD.

## AUTOMOTIVE PRODUCTS

The AD8284WCSVZ models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

## NOTES

## NOTES


D10992-0-7/13(B)

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