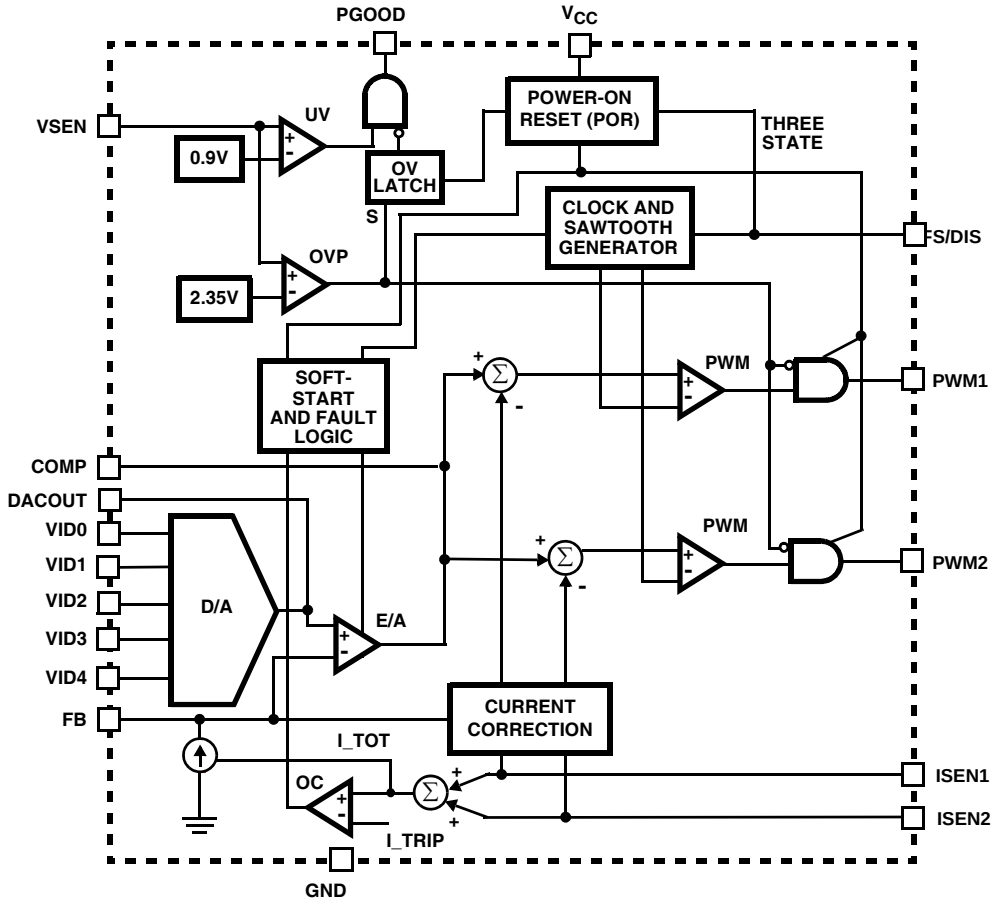
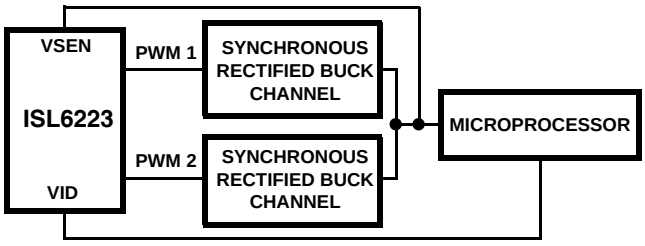
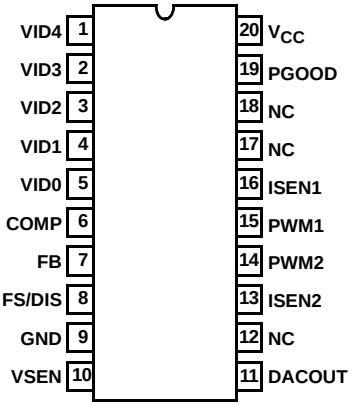
Block Diagram



Simplified Power System Diagram



Functional Pin Descriptions



VID4 (Pin 1), VID3 (Pin 2), VID2 (Pin 3), VID1 (Pin 4) and VID0 (Pin 5)

Voltage Identification inputs from microprocessor. These pins respond to TTL and 3.3V logic signals. The ISL6223 decodes VID bits to establish the output voltage. See Table 1.

COMP (Pin 6)

Output of the internal error amplifier. Connect this pin to the external feedback and compensation network.

FB (Pin 7)

Inverting input of the internal error amplifier.

FS/DIS (Pin 8)

Channel frequency, F_{SW}, select and disable. A resistor from this pin to ground sets the switching frequency of the converter. Pulling this pin to ground disables the converter and three states the PWM outputs. See Figure 11.

GND (Pin 9)

Bias and reference ground. All signals are referenced to this pin.

VSEN (Pin 10)

Power good monitor input. Connect to the microprocessor-CORE voltage.

DACOUT (Pin 11)

The DAC output. Connect a capacitor to this pin slows down the transition of the DAC output that is also the reference voltage to the error amplifier.

NC (Pin 12, Pin 17, Pin 18)

No connection.

ISEN2 (Pin 13) and ISEN1 (Pin 16)

Current sense inputs from the individual converter channel's phase nodes.

PWM2 (Pin 14) and PWM1 (Pin 15)

PWM outputs for each driven channel in use. Connect these pins to the PWM input of a HIP6601/2/3 driver.

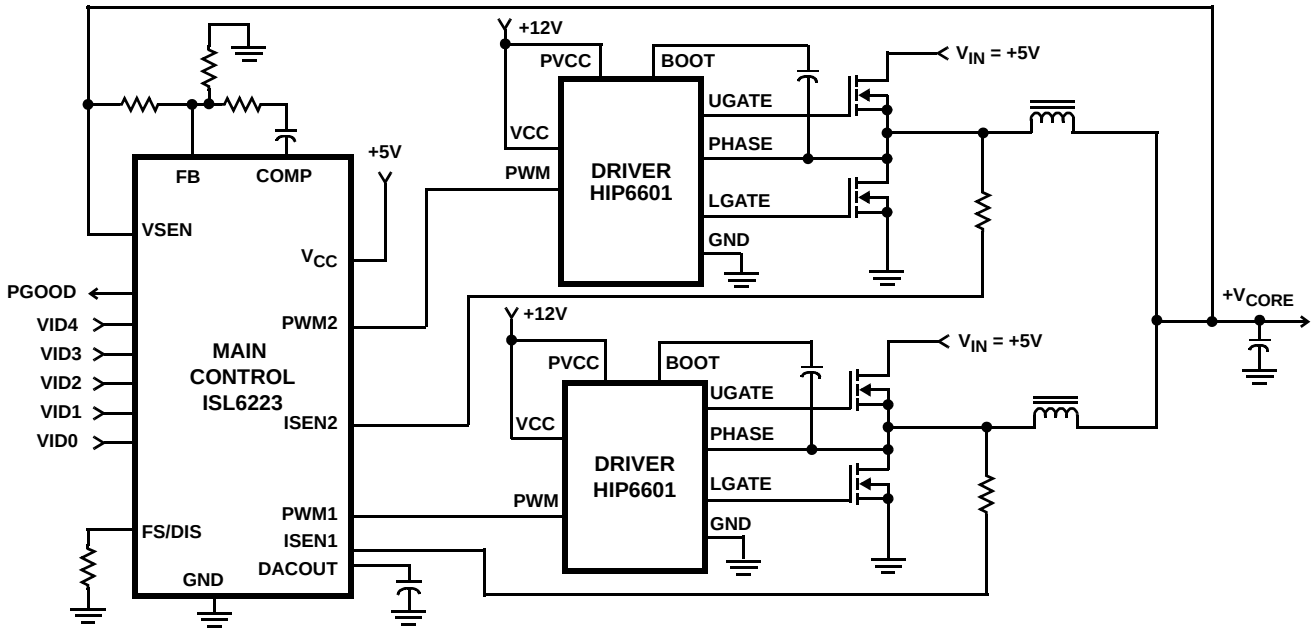
PGOOD (Pin 19)

Power good. This pin provides an open-drain logic-high signal when the microprocessor CORE voltage (VSEN pin) is within specified limits and Soft-Start has timed out.

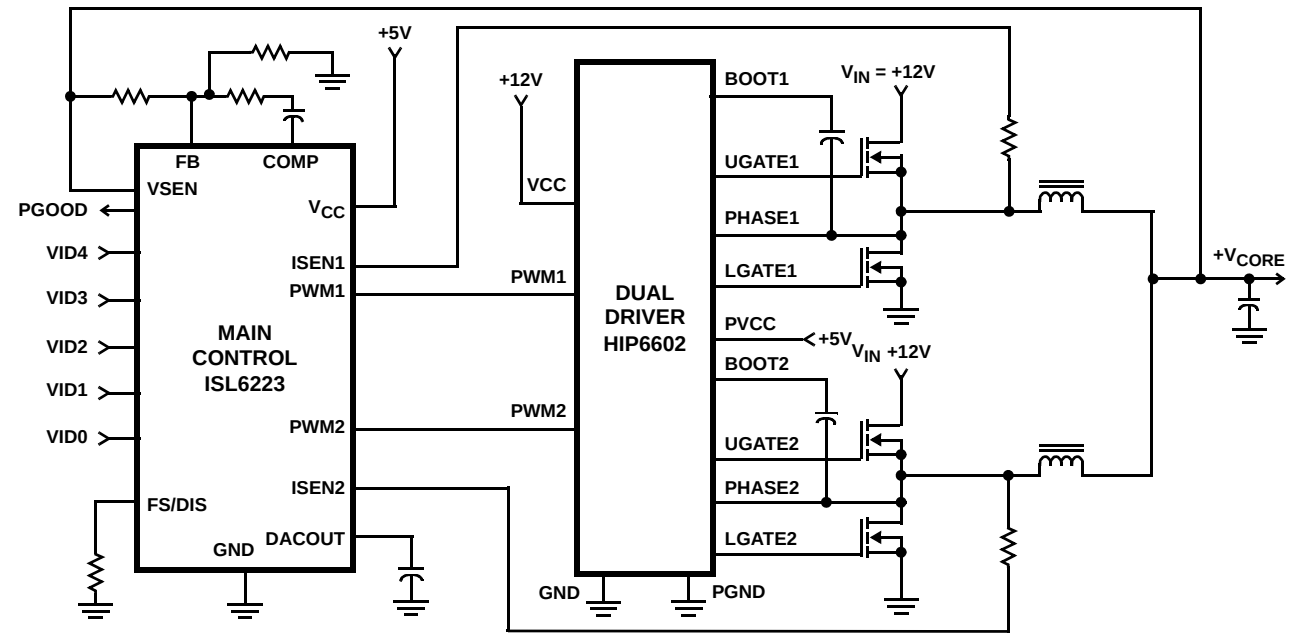
V_{CC} (Pin 20)

Bias supply. Connect this pin to a 5V supply.

Typical Application - Two Phase Converter Using HIP6601 Gate Drivers



Typical Application - Two Phase Converter Using a HIP6602 Gate Driver



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +7V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class 1

Recommended Operating Conditions

Supply Voltage . . . . . +5V ±5%
Ambient Temperature . . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SSOP Package	120

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, T_A = 0°C to 70°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY POWER					
Input Supply Current	R_T = 100kΩ, Active and Disabled Maximum Limit	-	10	15	mA
POR (Power-On Reset) Threshold	V_{CC} Rising	4.25	4.38	4.5	V
	V_{CC} Falling	3.75	3.88	4.00	V
REFERENCE AND DAC					
System Accuracy	Percent System Deviation from Programmed VID Codes	-1	-	1	%
DAC (VID0 - VID4) Input Low Voltage	DAC Programming Input Low Threshold Voltage	-	-	0.8	V
DAC (VID0 - VID4) Input High Voltage	DAC Programming Input High Threshold Voltage	2.0	-	-	V
VID Pull-Up	VIDx = 0V	5	12	30	µA
CHANNEL GENERATOR					
Frequency, F_{SW}	R_T = 100kΩ, ±1%	245	275	305	kHz
Adjustment Range	See Figure 11	0.05	-	1.5	MHz
Disable Voltage	Maximum Voltage at FS/DIS to Disable Controller. $I_{FS/DIS}$ = 1mA	-	-	1.0	V
ERROR AMPLIFIER					
DC Gain	R_L = 10k to GND	-	72	-	dB
Gain-Bandwidth Product	C_L = 100pF, R_L = 10k to GND	-	18	-	MHz
Slew Rate	C_L = 100pF, Load = ±400µA	-	5.3	-	V/µs
Maximum Output Voltage	R_L = 10k to GND, Load = 400µA	3.6	4.1	-	V
Minimum Output Voltage	R_L = 10k to GND, Load = -400µA	-	0.16	0.5	V
I_{SEN}					
Full Scale Input Current		-	50	-	µA
Overcurrent Trip Level		60	75	90	µA
POWER GOOD MONITOR					
Undervoltage Threshold	VSEN Rising	-	0.90	-	V
	VSEN Falling	-	0.88	-	V
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	0.18	0.4	V
PROTECTION					
Overvoltage Threshold	VSEN Rising	2.28	2.35	2.45	V
	VSEN Falling After Overvoltage	-	1.7	-	V

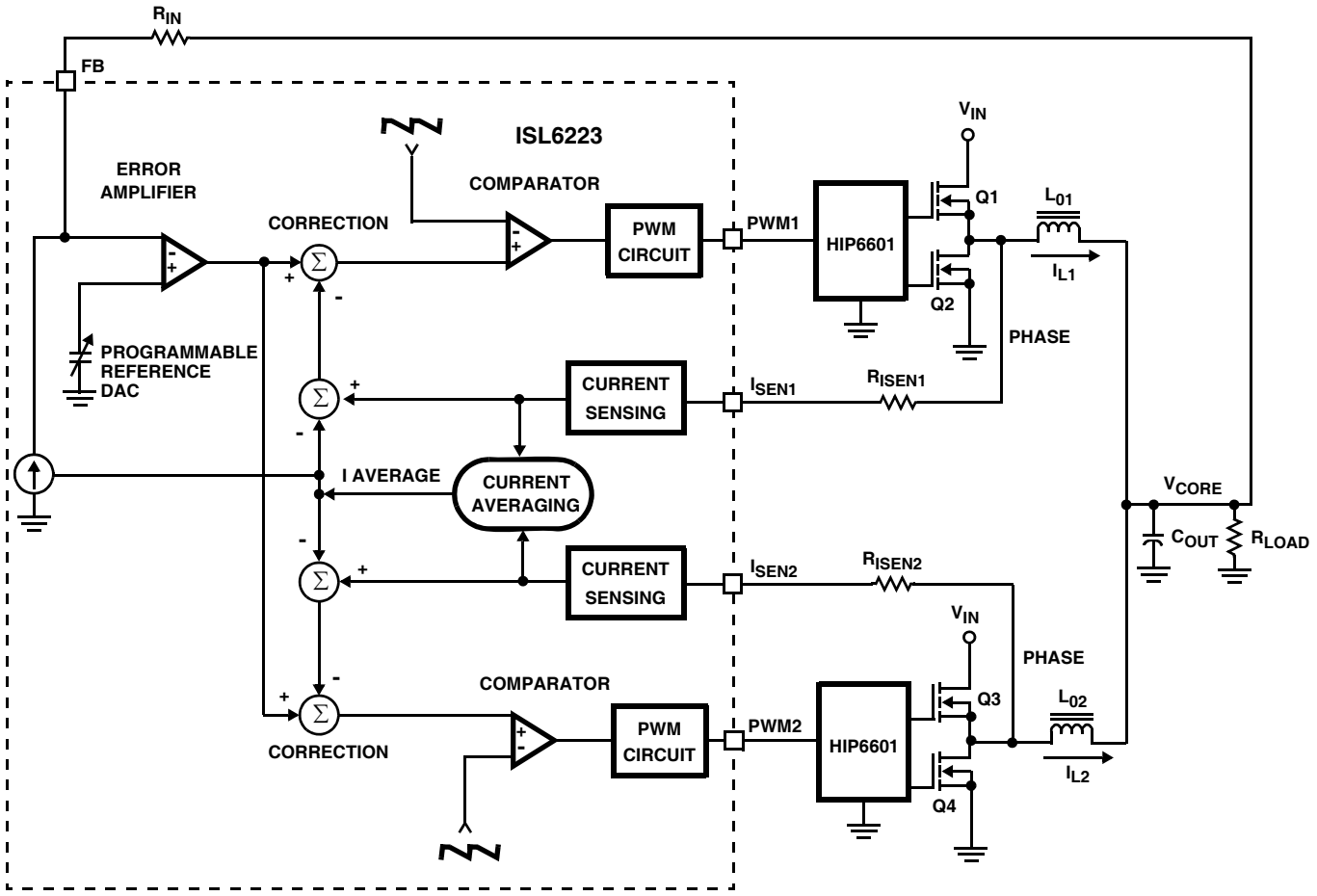


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THE ISL6223 VOLTAGE AND CURRENT CONTROL LOOPS FOR A TWO POWER CHANNEL REGULATOR

Operation

Figure 1 shows a simplified diagram of the voltage regulation and current control loops. Both voltage and current feedback are used to precisely regulate voltage and tightly control output currents, I_{L1} and I_{L2}, of the two power channels. The voltage loop comprises the Error Amplifier, Comparators, gate drivers and output MOSFETs. The Error Amplifier is essentially connected as a voltage follower that has an input, the Programmable Reference DAC and an output that is the CORE voltage.

Voltage Loop

Feedback from the CORE voltage is applied via resistor R_{IN} to the inverting input of the Error Amplifier. This signal can drive the Error Amplifier output either high or low, depending upon the CORE voltage. Low CORE voltage makes the amplifier output move towards a higher output voltage level. Amplifier output voltage is applied to the positive inputs of the Comparators via the Correction summing networks. Out-of-phase sawtooth signals are applied to the two Comparators inverting inputs. Increasing Error Amplifier voltage results in increased Comparator output duty cycle. This increased duty cycle signal is passed through the PWM CIRCUIT with no phase reversal and on to the HIP6601, again with no phase reversal for gate drive to the upper MOSFETs, Q1 and Q3. Increased duty cycle or ON time for the MOSFET transistors results in increased output voltage to compensate for the low output voltage sensed.

Current Loop

The current control loop works in a similar fashion to the voltage control loop, but with current control information applied individually to each channel's Comparator. The information used for this control is the voltage that is developed across $r_{DS(ON)}$ of each lower MOSFET, Q2 and Q4, when they are conducting. A single resistor converts and scales the voltage across the MOSFETs to a current that is applied to the Current Sensing circuit within the ISL6223. Output from these sensing circuits is applied to the current averaging circuit. Each PWM channel receives the difference current signal from the summing circuit that compares the average sensed current to the individual channel current. When a power channel's current is greater than the average current, the signal applied via the summing Correction circuit to the Comparator, reduces the output

pulse width of the Comparator to compensate for the detected “above average” current in that channel.

Droop Compensation

In addition to control of each power channel’s output current, the average channel current is also used to provide CORE voltage “droop” compensation. Average full channel current is defined as 50µA. By selecting an input resistor, R_{IN}, the amount of voltage droop required at full load current can be programmed. The average current driven into the FB pin results in a voltage increase across resistor R_{IN} that is in the direction to make the Error Amplifier “see” a higher voltage at the inverting input, resulting in the Error Amplifier adjusting the output voltage lower. The voltage developed across R_{IN} is equal to the “droop” voltage. See the “Current Sensing and Balancing” section for more details.

Applications and Convertor Start-Up

Each PWM power channel’s current is regulated. This enables the PWM channels to accurately share the load current for enhanced reliability. The HIP6601, HIP6602 or HIP6603 MOSFET driver interfaces with the ISL6223. For more information, see the HIP6601, HIP6602 or HIP6603 data sheets.

The ISL6223 controls the two PWM power channels 180° out of phase. Figure 2 shows the out of phase relationship between the two PWM channels.

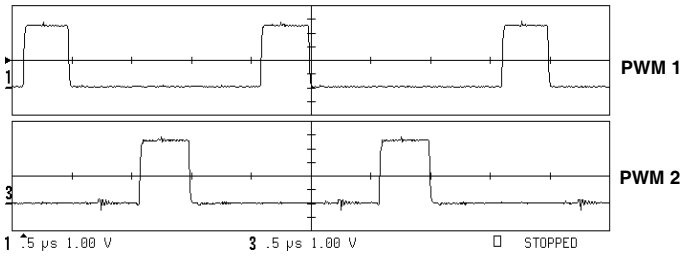


FIGURE 2. TWO PHASE PWM OUTPUT AT 500kHz

Power supply ripple frequency is determined by the channel frequency, F_{SW}, multiplied by the number of active channels. For example, if the channel frequency is set to 250kHz, the ripple frequency is 500kHz with two channels.

The IC monitors and precisely regulates the CORE voltage of a microprocessor. After initial start-up, the controller also provides protection for the load and the power supply. The following section discusses these features.

Initialization

The ISL6223 operates from a 5V power supply. Many functions are initiated by the rising supply voltage to the V_{CC} pin of the ISL6223. Oscillator, Sawtooth Generator, Soft-Start and other functions are initialized during this interval. These circuits are controlled by POR, Power-On Reset. During this interval, the PWM outputs are driven to a three state condition that makes these outputs essentially open. This state results in no gate drive to the output MOSFETs.

Once the V_{CC} voltage reaches 4.375V ($\pm$125mV), a voltage level to insure proper internal function, the PWM outputs are enabled and the Soft-Start sequence is initiated. If for any reason, the V_{CC} voltage drops below 3.875V ($\pm$125mV). The POR circuit shuts the converter down and again three states the PWM outputs.

Soft-Start

After the POR function is completed with V_{CC} reaching 4.375V, the Soft-Start sequence is initiated. Soft-Start, by its slow rise in CORE voltage from zero, avoids an overcurrent condition by slowly charging the discharged output capacitors. This voltage rise is initiated by an internal DAC that slowly raises the reference voltage to the error amplifier input. The voltage rise is controlled by the oscillator frequency and the DAC within the ISL6223, therefore, the output voltage is effectively regulated as it rises to the final programmed CORE voltage value.

For the first 64 PWM switching cycles, the DAC output remains inhibited and the PWM outputs remain three stated. From the 65th cycle and for another, approximately 300 cycles the PWM output remains low, clamping the lower output MOSFETs to ground, see Figure 3. The time variability is due to the Error Amplifier, Sawtooth Generator and Comparators moving into their active regions. After this short interval, the PWM outputs are enabled and increment the PWM pulse width from zero duty cycle to operational pulse width, thus allowing the output voltage to slowly reach the CORE voltage. The CORE voltage will reach its programmed value before the 4096 cycles, but the PGOOD output will not be initiated until the 4096th switching cycle.

The Soft-Start time or delay time, DT = $4096/F_{SW}$. For an oscillator frequency, F_{SW}, of 200kHz, the first 64 cycles or 320µs, the PWM outputs are held in a three state level as explained above. After this period and a short interval described above, the PWM outputs are initiated and the voltage rises in 20.16ms, for a total delay time DT of 20.48ms.

Figure 3 shows the start-up sequence as initiated by an enable (EN) switch, applied to the ISL6223. The start-up is enabled at the falling edge of the EN switch output.

Figure 4 shows the waveforms when the regulator is operating at 200kHz. Note that the Soft-Start duration is a function of the Channel Frequency as explained previously. Also note the pulses on the COMP terminal. These pulses are the current correction signal feeding into the comparator input (see the “Block Diagram” on page 2).

Figure 5 shows the regulator operating from a 12V battery supply. In this system, the battery voltage is available before any other voltages, including the 5V bias voltage V_{CC} for the controller IC. In this figure, note the slight rise in PGOOD as

the 5V supply rises. The PGOOD output stage is made up of NMOS and PMOS transistors. On the rising V_{CC}, the PMOS device becomes active slightly before the NMOS transistor pulls “down”, generating the slight rise in the PGOOD voltage.

Note that Figure 5 shows the 12V battery voltage available before the 5V supply to the ISL6223 has reached its threshold level. If conditions were reversed and the 5V supply was to rise first, the start-up sequence would be different. In this case, the ISL6223 will sense an overcurrent condition due to charging the output capacitors. The supply will then restart and go through the normal Soft-Start cycle.

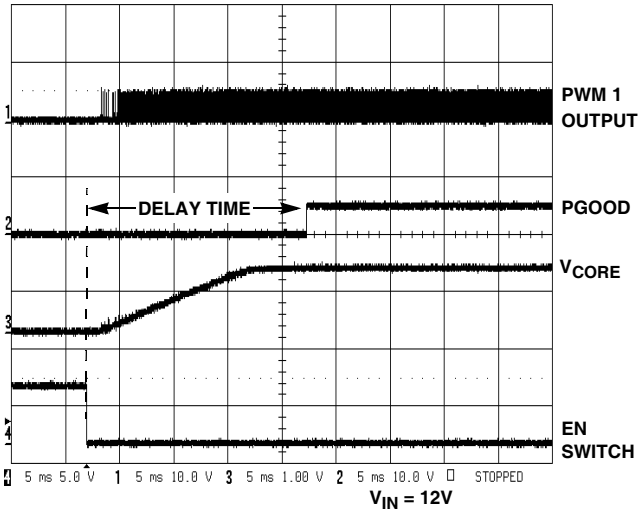


FIGURE 3. START-UP OF A SYSTEM OPERATING AT 200kHz

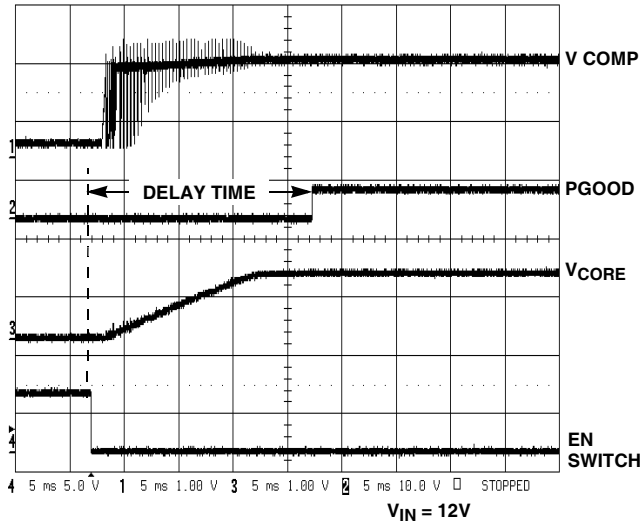


FIGURE 4. START-UP A SYSTEM OPERATING AT 200kHz

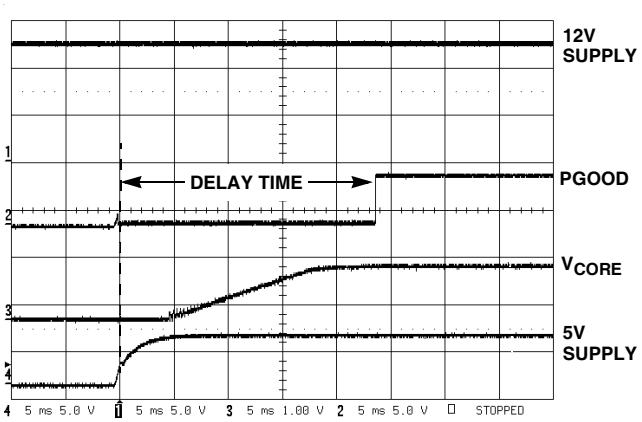


FIGURE 5. SUPPLY POWERED BY ATX SUPPLY

Fault Protection

The ISL6223 protects the microprocessor and the entire power system from damaging stress levels. Within the ISL6223 both Overvoltage and Overcurrent circuits are incorporated to protect the load and regulator.

Overvoltage

The VSEN pin is connected to the microprocessor CORE voltage. A CORE overvoltage condition is detected when the VSEN pin goes above 2.35V.

The overvoltage condition is latched, disabling normal PWM operation, and causing PGOOD to go low. The latch can only be reset by lowering and returning V_{CC} high to initiate a POR and Soft-Start sequence.

During a latched overvoltage, the PWM outputs will be driven either low or three state, depending upon the VSEN input. PWM outputs are driven low when the VSEN pin detects that the CORE voltage is above 2.35V. This condition drives the PWM outputs low, resulting in the lower or synchronous rectifier MOSFETs to conduct and shunt the CORE voltage to ground to protect the load.

If after this event, the CORE voltage falls below 1.7V, the PWM outputs will be three state. The HIP6601 family of drivers pass the three state information along, and shut off both upper and lower MOSFETs. This prevents “dumping” of the output capacitors back through the lower MOSFETs, avoiding a possibly destructive ringing of the capacitors and output inductors. If the conditions that caused the overvoltage still persist, the PWM outputs will be cycled between three state and V_{CORE} clamped to ground, as a hysteretic shunt regulator.

Undervoltage

The VSEN pin also detects when the CORE voltage falls below 0.9V level. This causes PGOOD to go low, but has no other effect on operation and is not latched. There is also hysteresis in this detection point.

Overcurrent

In the event of an overcurrent condition, the overcurrent protection circuit reduces the average current delivered to less than 25% of the current limit. When an overcurrent condition is detected, the controller forces all PWM outputs into a three state mode. This condition results in the gate driver removing drive to the output stages. The ISL6223 goes into a wait delay timing cycle that is equal to the Soft-Start ramp time. PGOOD also goes “low” during this time due to VSEN going below its threshold voltage. To lower the average output dissipation, the Soft-Start initial wait time is increased from 64 to 4096 cycles, then the Soft-Start ramp is initiated. At a PWM frequency of 200kHz, for instance, an overcurrent detection would cause a dead time of 20.48ms, then a ramp of 20.16ms.

At the end of the delay, PWM outputs are restarted and the Soft-Start ramp is initiated. If a short is present at that time, the cycle is repeated. This is the hiccup mode.

Figure 6 shows the supply shorted under operation and the hiccup operating mode described above. Note that due to the high short circuit current, overcurrent is detected before completion of the start-up sequence so the delay is not quite as long as the normal Soft-Start cycle.

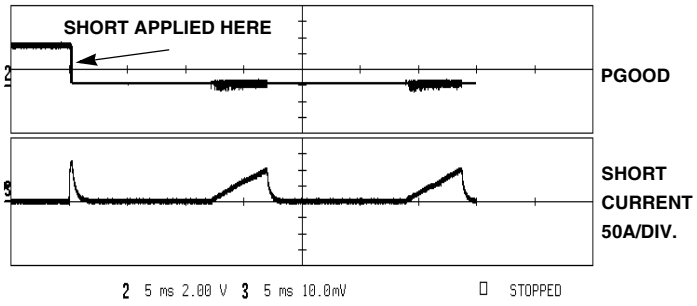


FIGURE 6. SHORT APPLIED TO SUPPLY AFTER POWER-UP

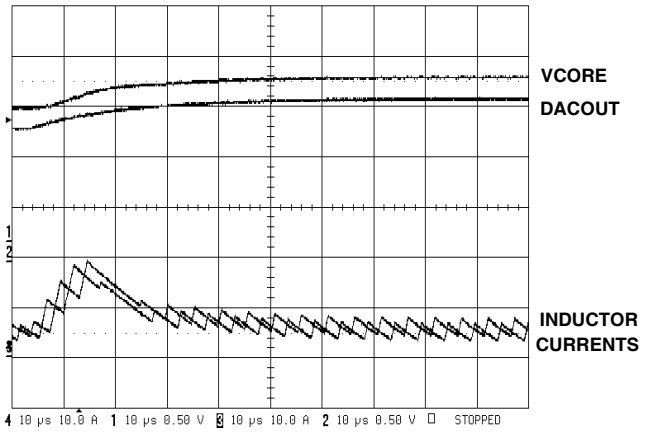


FIGURE 7. VID CHANGES FROM 1.3V TO 1.6V. THE LOAD CURRENT IS SET TO 10A.

DACOUT Pin

The internal DAC output is brought out to pin 11, DACOUT, in ISL6223. The typical output impedance of the DAC is 1.7kΩ. The DACOUT pin allows the user to connect a capacitor between this pin and the ground to form an RC filter to slow down the voltage transition at the non-inverting input of the error amplifier, when the VID code is being changed. Slower voltage transition reduces the inrush current to avoid tripping the overcurrent protection during the transition. Typical systems require the transition to be finished within 100µs, therefore, a time constant of 30µs to 40µs is a good tradeoff between the inrush current and the transition time. Connecting a 22nF capacitor to the DACOUT results in a time constant of 37µs for the RC filter. Figure 7 shows the waveforms for the VID changes from 1.3V to 1.6V. From top to bottom, the waveforms are the core voltage, the DACOUT, and the two inductor currents.

TABLE 1. VOLTAGE IDENTIFICATION CODES

VOLTAGE IDENTIFICATION CODE AT PROCESSOR PINS					VCC_{CORE} (V_{DC})
VID4	VID3	VID2	VID1	VID0	
1	1	1	1	1	Shutdown
1	1	1	1	0	0.925
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	1.100
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	1	Shutdown
0	1	1	1	0	1.300
0	1	1	0	1	1.350
0	1	1	0	0	1.400
0	1	0	1	1	1.450
0	1	0	1	0	1.500
0	1	0	0	1	1.550
0	1	0	0	0	1.600
0	0	1	1	1	1.650
0	0	1	1	0	1.700
0	0	1	0	1	1.750
0	0	1	0	0	1.800
0	0	0	1	1	1.850
0	0	0	1	0	1.900
0	0	0	0	1	1.950
0	0	0	0	0	2.000

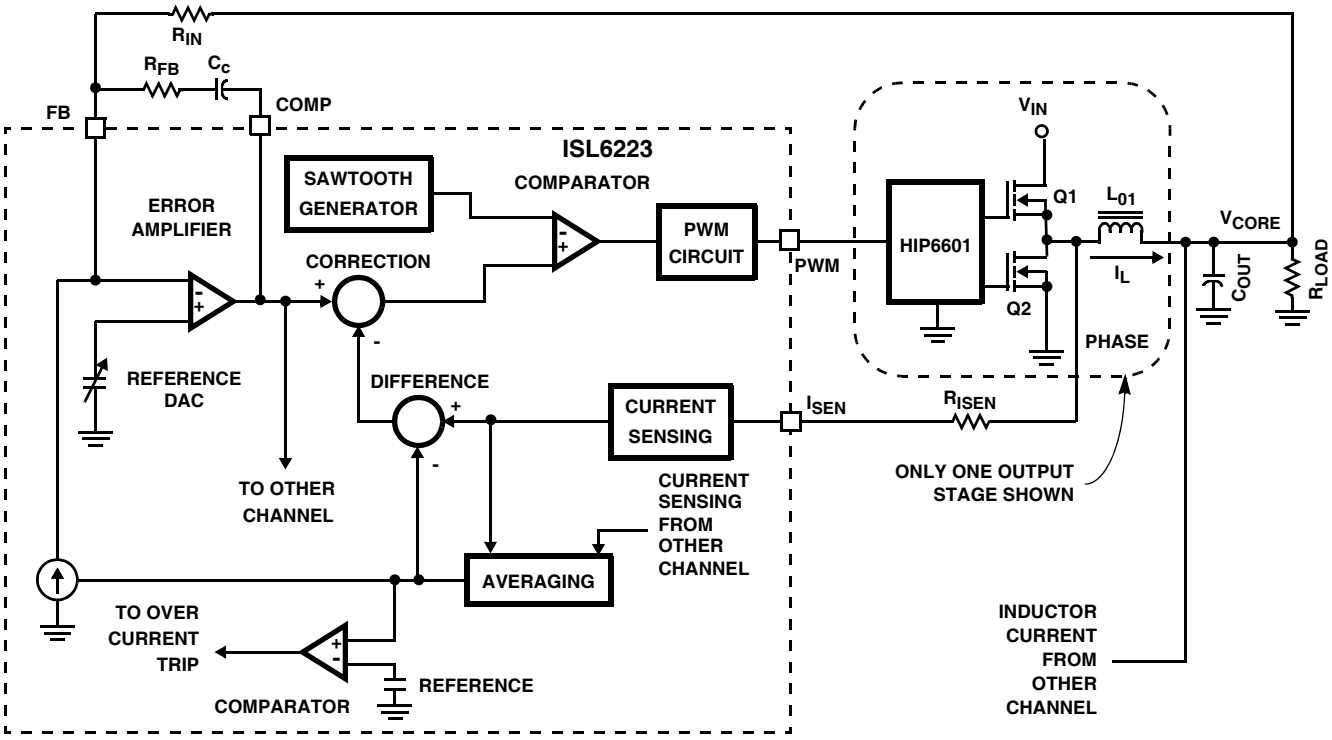


FIGURE 8. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM SHOWING CURRENT AND VOLTAGE SAMPLING

CORE Voltage Programming

The voltage identification pins (VID0, VID1, VID2, VID3 and VID4) set the CORE output voltage. Each VID pin is pulled to V_{CC} by an internal 12µA current source and accepts open-collector/open-drain/open-switch-to-ground or standard low-voltage TTL or CMOS signals.

Table 1 shows the nominal DAC voltage as a function of the VID codes. The power supply system is ±1% accurate over the operating temperature and voltage range.

Current Sensing and Balancing

Overview

The ISL6223 samples the on-state voltage drop across each synchronous rectifier FET, Q2, as an indication of the inductor current in that phase, see Figure 8. Neglecting AC effects (to be discussed later), the voltage drop across Q2 is simply $r_{DS(ON)}$(Q2) x inductor current (I_L). Note that I_L, the inductor current, is 1/2 of the total current (I_{LT}).

The voltage at Q2's drain, the PHASE node, is applied to the R_{ISEN} resistor to develop the I_{ISEN} current to the ISL6223 ISEN pin. This pin is held at virtual ground, so the current through R_{ISEN} is I_L x $r_{DS(ON)}$(Q2) / R_{ISEN}.

The I_{ISEN} current provides information to perform the following functions:

1. Detection of an overcurrent condition
2. Reduce the regulator output voltage with increasing load current (droop)
3. Balance the I_L currents in the two phases

Overcurrent, Selecting R_{ISEN}

The current detected through the R_{ISEN} resistor is averaged with the current detected in the other channel. The averaged current is compared with a trimmed, internally generated current, and used to detect an overcurrent condition.

The nominal current through the R_{ISEN} resistor should be 50µA at full output load current, and the nominal trip point for overcurrent detection is 150% of that value, or 75µA. Therefore:

$$R_{ISEN} = I_L \times r_{DS(ON)}(Q2) / 50\mu A \quad \text{(EQ. 1)}$$

For a full load of 25A per phase, and an $r_{DS(ON)}$ (Q2) of 4mΩ, R_{ISEN} = 2kΩ.

The overcurrent trip point would be 150% of 25A, or approximately 37.5A per phase. The R_{ISEN} value can be adjusted to change the overcurrent trip point, but it is suggested to stay within ±25% of nominal.

Droop, Selection of R_{IN}

The average of the currents detected through the R_{ISEN} resistors is also steered to the FB pin. There is no DC return path connected to the FB pin except for R_{IN}, so the average current creates a voltage drop across R_{IN}. This drop increases the apparent V_{CORE} voltage with increasing load current, causing the system to decrease V_{CORE} to maintain balance at

the FB pin. This is the desired “droop” voltage used to maintain V_{CORE} within limits under transient conditions.

With a high dv/dt load transient, typical of high performance microprocessors, the largest deviations in output voltage occur at the leading and trailing edges of the load transient. In order to fully utilize the output-voltage tolerance range, the output voltage is positioned in the upper half of the range when the output is unloaded and in the lower half of the range when the controller is under full load. This droop compensation allows larger transient voltage deviations and thus reduces the size and cost of the output filter components.

R_{IN} should be selected to give the desired “droop” voltage at the normal full load current 50µA applied through the R_{ISEN} resistor (or at a different full load current if adjusted as under “Overcurrent, Selecting R_{ISEN}” above).

$$R_{IN} = V_{DROOP}/50\mu A \quad \text{(EQ. 2)}$$

For a V_{DROOP} of 80mV, R_{IN} = 1.6kΩ

The AC feedback components, R_{FB} and Cc, are scaled in relation to R_{IN}.

Current Balancing

The detected currents are also used to balance the phase currents.

Each phase’s current is compared to the average of the two phase currents, and the difference is used to create an offset in that phase’s PWM comparator. The offset is in a direction to reduce the imbalance.

The balancing circuit can not make up for a difference in $r_{DS(ON)}$ between synchronous rectifiers. If a FET has a higher $r_{DS(ON)}$, the current through that phase will be reduced.

Figures 9 and 10 show the inductor current of a two phase system without and with current balancing.

Inductor Current

The inductor current in each phase of a multi-phase Buck converter has two components. There is a current equal to the load current divided by the number of phases (I_{LT} / n), and a sawtooth current (i_{PK-PK}), resulting from switching. The sawtooth component is dependent on the size of the inductors, the switching frequency of each phase, and the values of the input and output voltage. Ignoring secondary effects, such as series resistance, the peak to peak value of the sawtooth current can be described by Equation 3:

$$i_{P-P} = (V_{IN} \times V_{CORE} - V_{CORE}^2)/(L \times F_{SW} \times V_{IN}) \quad \text{(EQ. 3)}$$

Where:

V_{CORE} = DC value of the output or VID voltage
V_{IN} = DC value of the input or supply voltage
L = value of the inductor
F_{SW} = switching frequency

Example:

If V_{CORE} = 1.6V, V_{IN} = 12V, L = 1.3µH and F_{SW} = 250kHz; then i_{P-P} = 4.3A.

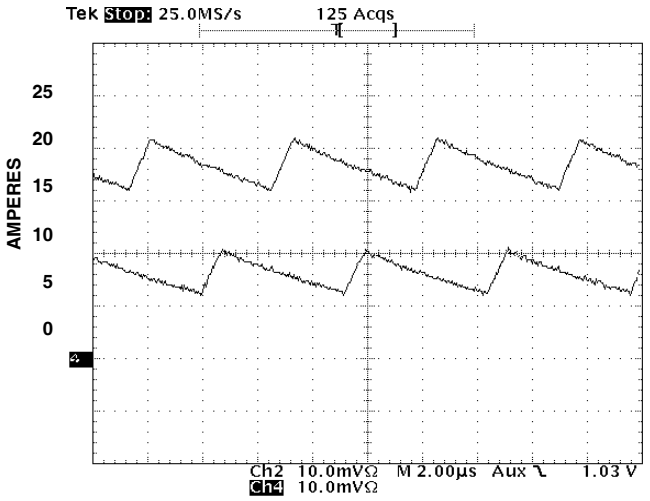


FIGURE 9. TWO CHANNEL MULTIPHASE SYSTEM WITH CURRENT BALANCING DISABLED

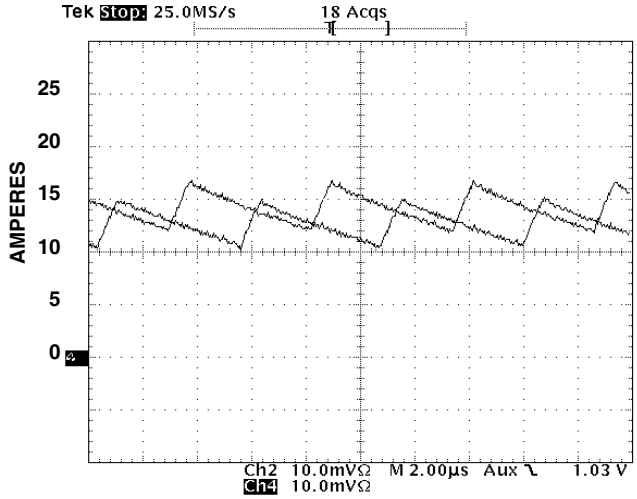


FIGURE 10. TWO CHANNEL MULTIPHASE SYSTEM WITH CURRENT BALANCING ENABLED

The inductor, or load current, flows alternately from V_{IN} through Q1 and from ground through Q2. The ISL6223 samples the on-state voltage drop across each Q2 transistor to indicate the inductor current in that phase. The voltage drop is sampled 1/3 of a switching period, $1/F_{SW}$, after Q1 is turned OFF and Q2 is turned on. Because of the sawtooth current component, the sampled current is different from the average current per phase. Neglecting secondary effects, the sampled current (I_{SAMPLE}) can be related to the load current (I_{LT}) by Equation 4:

$$I_{SAMPLE} = I_{LT}/n + (V_{IN} \times V_{CORE} - 3V_{CORE}^2)/(6L \times F_{SW} \times V_{IN}) \quad \text{(EQ. 4)}$$

Where:

I_{LT} = total load current
n = the number of channels

Example: Using the previously given conditions, if I_{LT} = 50A and n = 2; then I_{SAMPLE} = 25.49A.

As discussed previously, the voltage drop across each Q2 transistor at the point in time when current is sampled is $r_{DS(ON)}$ (Q2) x I_{SAMPLE}. The voltage at Q2's drain, the PHASE node, is applied through the R_{ISEN} resistor to the ISL6223 ISEN pin. This pin is held at virtual ground, so the current into ISEN is:

$$I_{SENSE} = I_{SAMPLE} \times r_{DS(ON)}(Q2) / R_{ISEN} \quad \text{(EQ. 5)}$$

$$R_{ISEN} = I_{SAMPLE} \times r_{DS(ON)}(Q2) / (50\mu A) \quad \text{(EQ. 6)}$$

Example: From the previous conditions, if I_{LT} = 50A, I_{SAMPLE} = 25.49A and $r_{DS(ON)}$ (Q2) = 4mΩ; then R_{ISEN} = 2.04k, $I_{CURRENT\ TRIP}$ = 150%, and Short circuit I_{LT} = 75A.

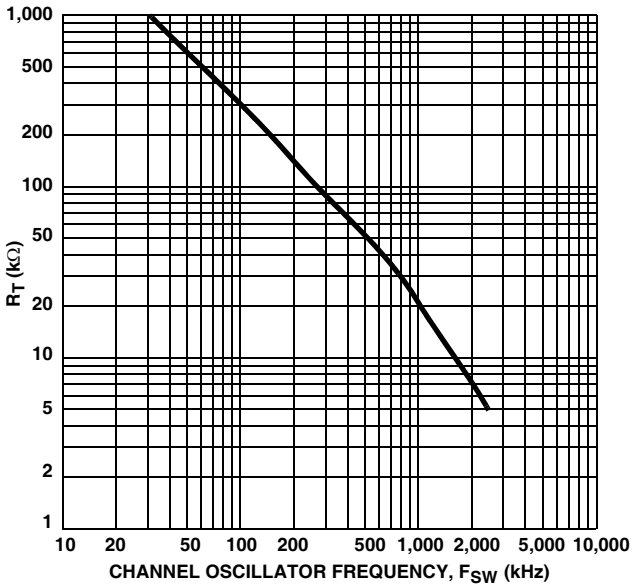


FIGURE 11. RESISTANCE R_T vs FREQUENCY

Channel Frequency Oscillator

The channel oscillator frequency is set by placing a resistor, R_T, to ground from the FS/DIS pin. Figure 11 is a curve showing the relationship between frequency, $F_{SW,}$ and resistor R_T. To avoid pickup by the FS/DIS pin, it is important to place this resistor next to the pin. If this pin is also used to disable the converter, it is also important to locate the pull-down device next to this pin.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes. Contact **Intersil** for evaluation board drawings of the component placement and printed circuit board.

There are two sets of critical components in a DC/DC converter using a ISL6223 controller and a HIP6601 gate driver. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches. Locate the output inductors and output capacitors between the MOSFETs and the load. Locate the gate driver close to the MOSFETs.

The critical small components include the bypass capacitors for VCC and PVCC on the gate driver ICs. Locate the bypass capacitor, C_{BP}, for the ISL6223 controller close to the device. It is especially important to locate the resistors associated with the input to the amplifiers close to their respective pins, since they represent the input to feedback amplifiers. Resistor R_T, that sets the oscillator frequency should also be located next to the associated pin. It is especially important to place the R_{SEN} resistor(s) at the respective terminals of the ISL6223.

A multi-layer printed circuit board is recommended. Figure 12 shows the connections of the critical components for one output channel of the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to inductor L_{O1} short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the driver IC to the MOSFET gate and source should be sized to carry at least one ampere of current.

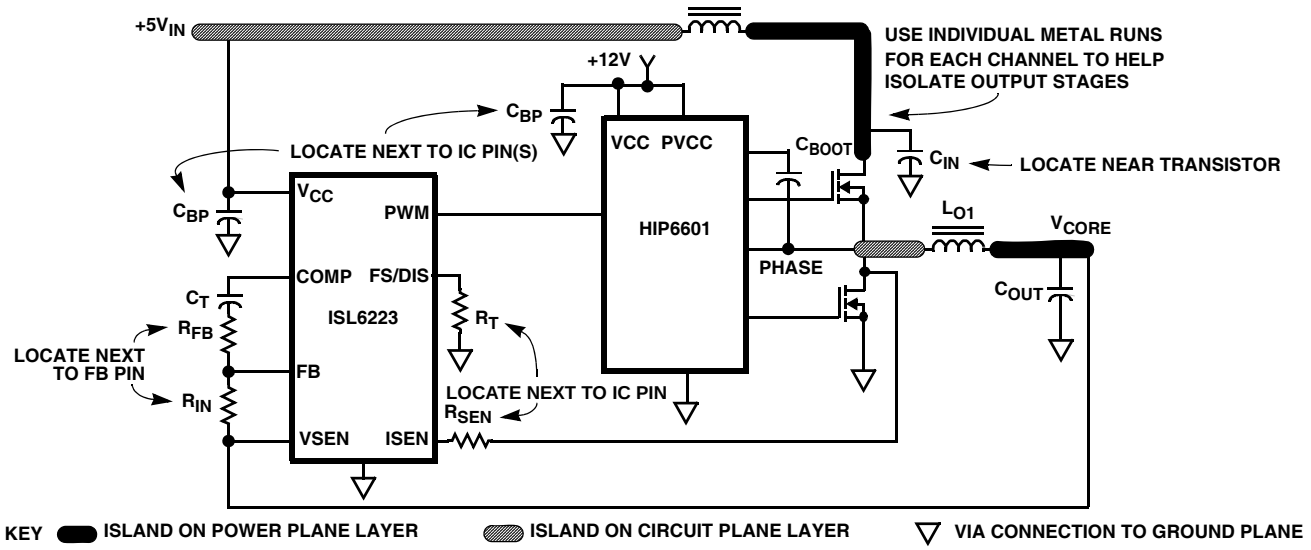


FIGURE 12. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Component Selection Guidelines

Output Capacitor Selection

The output capacitor is selected to meet both the dynamic load requirements and the voltage ripple requirements. The load transient for the microprocessor CORE is characterized by high slew rate (di/dt) current demands. In general, multiple high quality capacitors of different size and dielectric are paralleled to meet the design constraints.

Modern microprocessors produce severe transient load rates. High frequency capacitors supply the initially transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. In most cases, multiple capacitors of small case size perform better than a single large case capacitor.

Bulk capacitor choices include aluminum electrolytic, OS-Con, Tantalum and even ceramic dielectrics. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Consult the capacitor manufacturer and measure the capacitor's impedance with frequency to select a suitable component. For surface mount designs, solid tantalum capacitors or Panasonic Speciality Polymer (SP) capacitors can be used.

Output Inductor Selection

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Small inductors in a multi-phase converter reduces the response time without significant increases in total ripple current.

The output inductor of each power channel controls the ripple current. The control IC is stable for channel ripple current (peak-to-peak) up to twice the average current. A single channel's ripple current is approximately:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 7)}$$

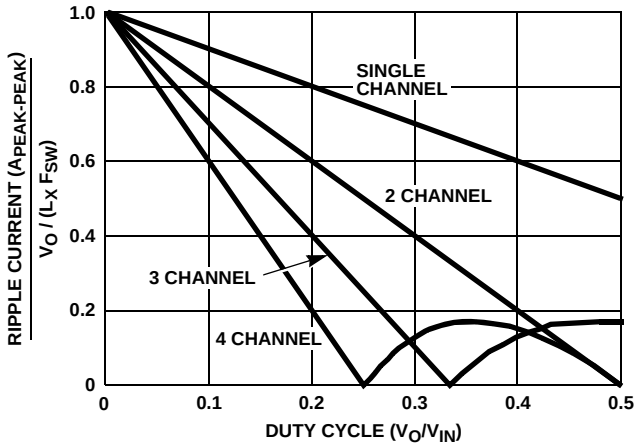


FIGURE 13. RIPPLE CURRENT vs DUTY CYCLE

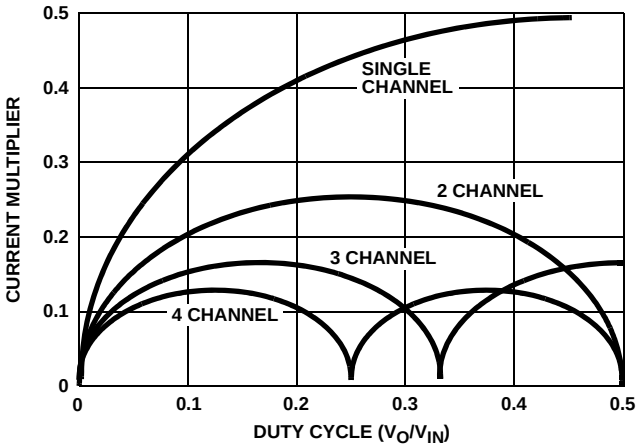


FIGURE 14. CURRENT MULTIPLIER vs DUTY CYCLE

The current from multiple channels tend to cancel each other and reduce the total ripple current. Figure 13 gives the total ripple current as a function of duty cycle, normalized to the parameter $(Vo)/(L \cdot F_S)$ at zero duty cycle. To determine the total ripple current from the number of channels and the duty cycle, multiply the y-axis value by $(Vo)/(LxF_{SW})$.

Small values of output inductance can cause excessive power dissipation. The ISL6223 is designed for stable operation for ripple currents up to twice the load current. However, for this condition, the RMS current is 115% above the value shown in the following MOSFET Selection and Considerations section. With all else fixed, decreasing the inductance could increase the power dissipated in the MOSFETs by 30%.

Input Capacitor Selection

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current required for a multi-phase converter can be approximated with the aid of Figure 14.

First determine the operating duty ratio as the ratio of the output voltage divided by the input voltage. Find the Current Multiplier from the curve with the appropriate power channels. Multiply the current multiplier by the full load output current. The resulting value is the RMS current rating required by the input capacitor.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors should be placed very close to the drain of the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For bulk capacitance, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors or Panasonic Speciality Polymer (SP) capacitors can be used. Caution must be exercised with regard to the capacitor surge current rating when using the Tantalum capacitors. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty factor (see Equations 8 and 9). The conduction losses are the main component of power dissipation for the lower MOSFETs, Q2 and Q4 of Figure 1. Only the upper MOSFETs, Q1 and Q3 have significant switching losses, since the lower device turns on and off into near zero voltage.

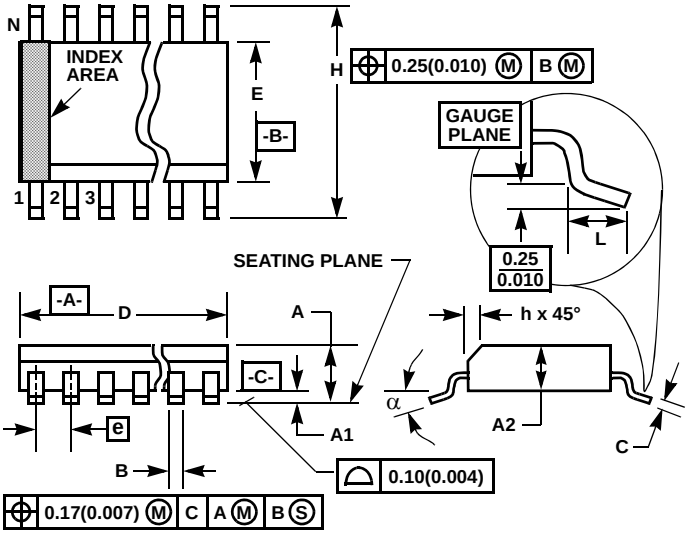
The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFETs body diode. The reverse-recovery loss can be a significant portion of the upper MOSFETs. The gate-charge losses are dissipated by the Driver IC and don't heat the MOSFETs. However, large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_{SW}}{2} \quad \text{(EQ. 8)}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 9)}$$

A diode, anode to ground, may be placed across Q2 and Q4 of Figure 1. These diodes function as a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFETs and the turn on of the upper MOSFETs. The diodes must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is usually acceptable to omit the diodes and let the body diodes of the lower MOSFETs clamp the negative inductor swing, but efficiency could drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M20.15

20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.56	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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