ABSOLUTE MAXIMUM RATINGS

IN to GND ....-0.3V to +28V
LDOH to IN ....+0.3V to -6V
LDOL to GND ....-0.3V to +6V
PDRV to GND .... (V_{LDOH} - 0.3V) to (V_{IN} + 0.3V)
NDRV to GND ....-0.3V to (V_{LDOL} + 0.3V)
TOFF, REF, SET, TERM, CC to GND ......-0.3V to (V_{LDOL} + 0.3V)
D0, D1 to GND ....-0.3V to +6V
CS+, CS- to GND ....-0.3V to +28V
PGND to GND..±0.3V

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.6mW/°C above +70°C)..................... 772mW
Package Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 1) ....103.7°C/W
Package Junction-to-Case Thermal Resistance θ_{JC})
(Note1) .... 37°C/W
Operating Temperature Range
MAX164_EEE ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) .... +300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal comsiderations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{OUT} = 6V, Circuit of Figure 1, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			5.5		26	V
Linear-Regulator Output Voltage, V_{IN} Referenced	V_{LDOH}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA		V_{IN} - 5.5	V_{IN} - 5.0	V_{IN} - 4.5	V
Linear-Regulator Output Voltage, Ground Referenced	V_{LDOL}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA		4.5	5.0	5.5	V
Full-Scale Current-Sense Threshold		MAX1640		142	150	158	mV
		MAX1641		147	150	153	
Quarter-Scale Current-Sense Threshold		MAX1640		36	42	48	mV
		MAX1641		34	37.5	41	
Current-Sense Line Regulation		V_{IN} = V_{OUT} + 0.5V to 26V			0.03		%/V
Output Current Compliance		V_{OUT} = 2V to 24V	MAX1640		0.1	0.4	%/V
			MAX1641		0.1		
Quiescent V_{IN} Supply Current		D0 or D1 = high			2	4	mA
		D0 = D1 = low (off mode)			500		µA
Output Current in Off Mode		D0 = D1 = low				1	µA
V_{LDOL} Undervoltage Lockout				4.05	4.20	4.35	V
Reference Voltage	V_{REF}			1.96	2.00	2.04	V
Reference Load Regulation		I_{REF} = 0 to 50µA			4	10	mV
V_{SET} Input Current						1	µA
FET Drive Output Resistance		PFET and NFET drive				12	Ω
Off-Time Range				1		10	µs
Off-Time Accuracy		R_{TOFF} = 62kΩ		1.7	2.2	2.7	µs
Pulse-Trickle Mode Duty-Cycle Period		D0 = low, D1 = high, R_{TOFF} = 100kΩ		27	33	40	ms
Pulse-Trickle Mode Duty Cycle (Note 2)		D0 = low, D1 = high, R_{TOFF} = 100kΩ			12.5		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{OUT} = 6V, Circuit of Figure 1, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Maximum Duty Cycle			100			%
Input Low Voltage	V_{IL}	D0, D1			0.8	V
Input High Voltage	V_{IH}	D0, D1	2.4			V
Input Leakage Current	I_{IN}	D0, D1			±1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{OUT} = 6V, Circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted.)

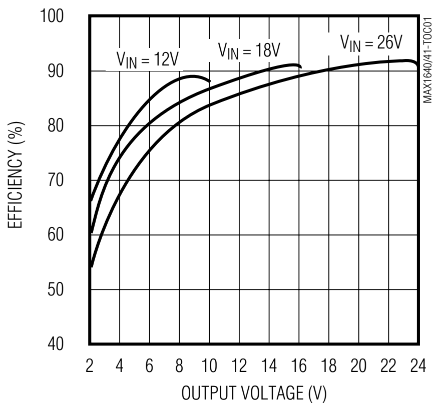
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		5.5		26	V
Linear-Regulator Output Voltage, V_{IN} Referenced	V_{LDOH}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA	V_{IN} - 5.5		V_{IN} - 4.5	V
Linear-Regulator Output Voltage, Ground Referenced	V_{LDOL}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA	4.5		5.5	V
Full-Scale Current-Sense Threshold		MAX1640	141		159	mV
		MAX1641	146		154	
Quarter-Scale Current-Sense Threshold		MAX1640	34		48	mV
		MAX1641	33		42	
Output Current Compliance		V_{OUT} = 2V to 24V (MAX1640)			0.4	%/V
Quiescent V_{IN} Supply Current		D0 or D1 = high			4	mA
Output Current in Off Mode		D0 = D1 = low			1	µA
V_{LDOL} Undervoltage Lockout			4.0		4.4	V
Reference Voltage	V_{REF}		1.94		2.06	V
Reference Load Regulation		I_{REF} = 0 to 50µA			10	mV
V_{SET} Input Current					1	µA
FET Drive Output Resistance					12	Ω
Off-Time Range			1.5		8	µs
Off-Time Accuracy		R_{TOFF} = 62kΩ	1.5		2.5	µs
Pulse-Trickle Mode Duty-Cycle Period		D0 = low, D1 = high, R_{TOFF} = 50kΩ	25		42	ms
PWM Maximum Duty Cycle			100			%
Input Low Voltage	V_{IL}	D0, D1			0.8	V
Input High Voltage	V_{IH}	D0, D1	2.4			V
Input Leakage Current	I_{IN}	D0, D1			±1	µA

Note 2: This ratio is generated by a 1:8 clock divider and is not an error source for current calculations.

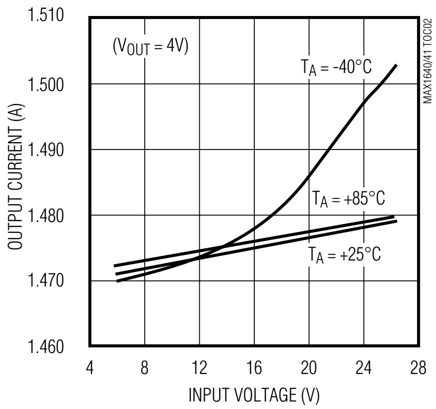
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

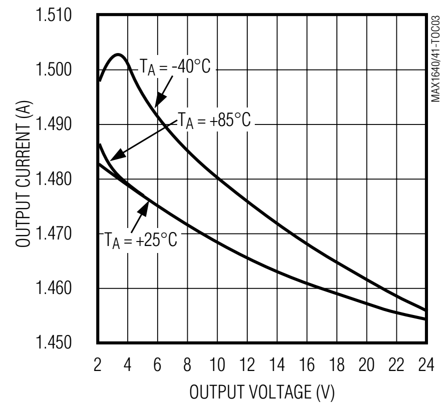
EFFICIENCY vs. OUTPUT VOLTAGE



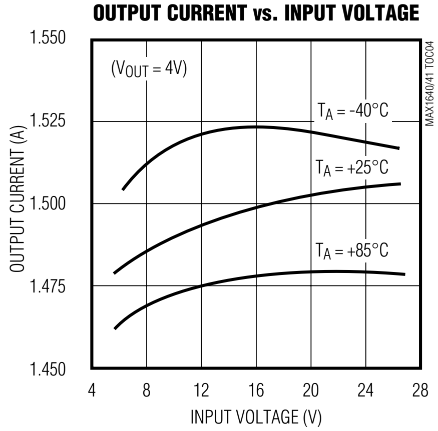
MAX1640
OUTPUT CURRENT vs. INPUT VOLTAGE



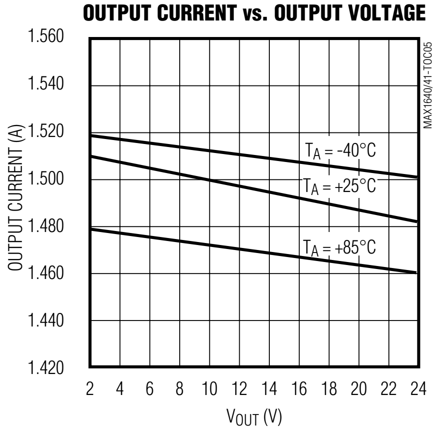
MAX1640
OUTPUT CURRENT vs. OUTPUT VOLTAGE



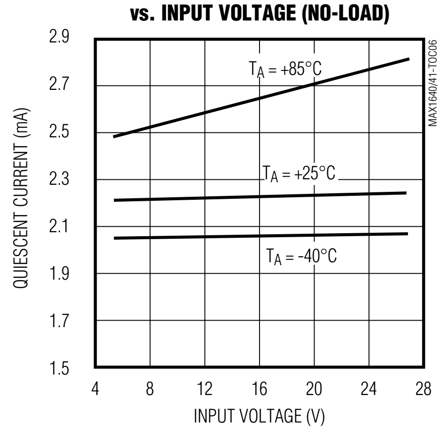
MAX1641
OUTPUT CURRENT vs. INPUT VOLTAGE



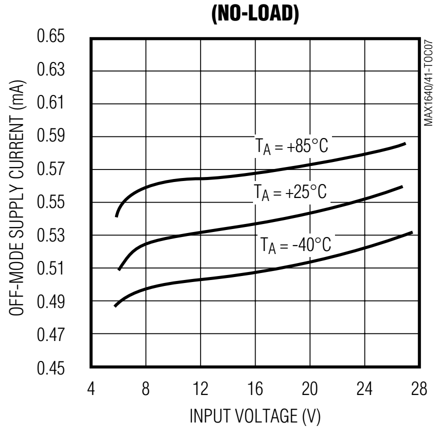
MAX1641
OUTPUT CURRENT vs. OUTPUT VOLTAGE



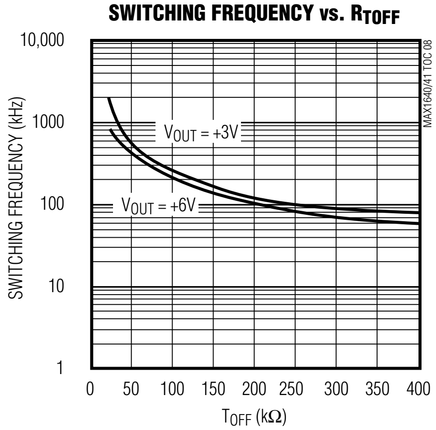
QUIESCENT CURRENT
vs. INPUT VOLTAGE (NO-LOAD)



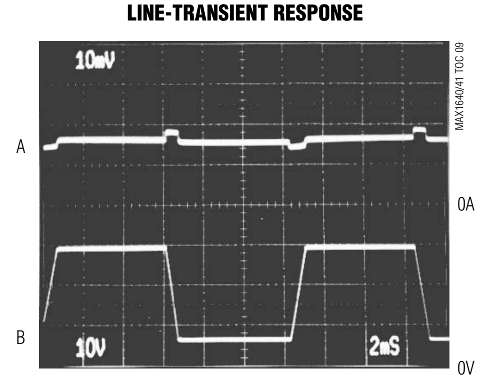
OFF-MODE SUPPLY CURRENT
(NO-LOAD)



SWITCHING FREQUENCY vs. R_{TOFF}



LINE-TRANSIENT RESPONSE

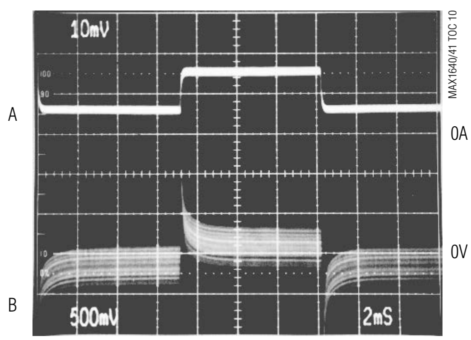


V_{LOAD} = 3V 2ms/div
A: OUTPUT CURRENT, D1 = D0 = 1 1A/div
B: INPUT VOLTAGE, 10V/div

Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

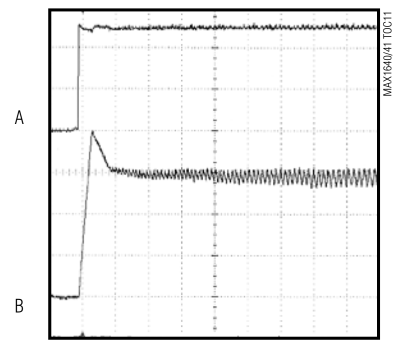
CURRENT-MODE CHANGE RESPONSE TIME



2ms/div

V_{IN} = 12V, V_{SET} = 1V, R_{LOAD} = 4Ω, NO OUTPUT CAPACITOR
A: OUTPUT CURRENT, D0 = D1 = 0 1A/div
B: LOAD VOLTAGE, AC coupled, 500mV/div

EXITING OFF MODE



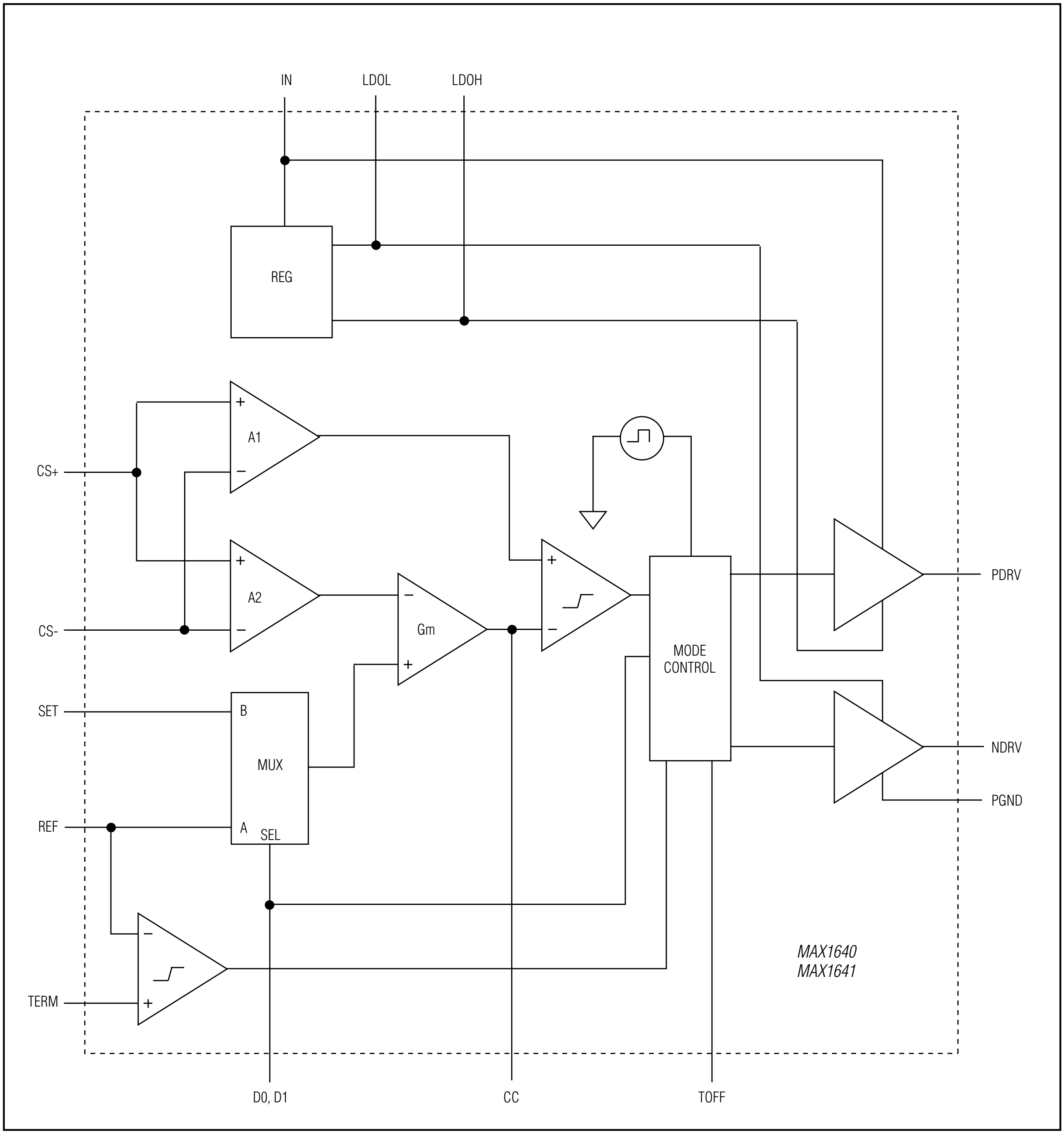
20µs/div

V_{IN} = 12V, R_{LOAD} = 4Ω
A: D0 = D1 = 1 2V/div
B: OUTPUT CURRENT, 0.5A/div

Pin Description

PIN	NAME	FUNCTION
1	LDOL	Internal, Ground-Referenced Low-Dropout Linear Regulator Output. Bypass LDOL with a 0.1µF capacitor in parallel with a 4.7µF capacitor to GND.
2	TOFF	Off-Time Select Input. A resistor (R_{TOFF}) connected from TOFF to GND programs the off-time for the hysteretic PWM step-down converter. This resistor also sets the period in duty-cycle mode. See *Duty-Cycle Mode and Programming the Off-Time*.
3, 4	D1, D0	Digital Inputs. Select mode of operation (Table 1).
5	CC	Constant-Current Loop Compensation Input. Bypass CC with a 0.01µF capacitor to GND.
6	REF	Reference Voltage Output (V_{REF} = 2V). Bypass REF with a 0.1µF capacitor to GND.
7	SET	Current Select Input. Program the desired current level by applying a voltage at SET between 0V and V_{REF}, ($I = V_{SET} / 13.3R_{SENSE}$). See Figure 2.
8	TERM	Maximum Output Voltage Termination Input. When V_{TERM} exceeds the reference voltage, the comparator resets the internal PWM latch, shutting off the external P-channel FET.
9	GND	Ground
10	CS-	Negative Current-Sense Comparator Input
11	CS+	Positive Current-Sense Comparator Input
12	PGND	High-Current Ground Return for the output drivers
13	NDRV	Gate Drive for an optional N-channel FET synchronous rectifier
14	PDRV	Gate Drive for the P-channel FET
15	LDOH	Internal, Input-Referenced Low-Dropout Linear Regulator Output. Bypass LDOH with a 0.33µF capacitor to IN.
16	IN	Power-Supply Input. Input of the internal, low-dropout linear regulators.

Functional Diagram



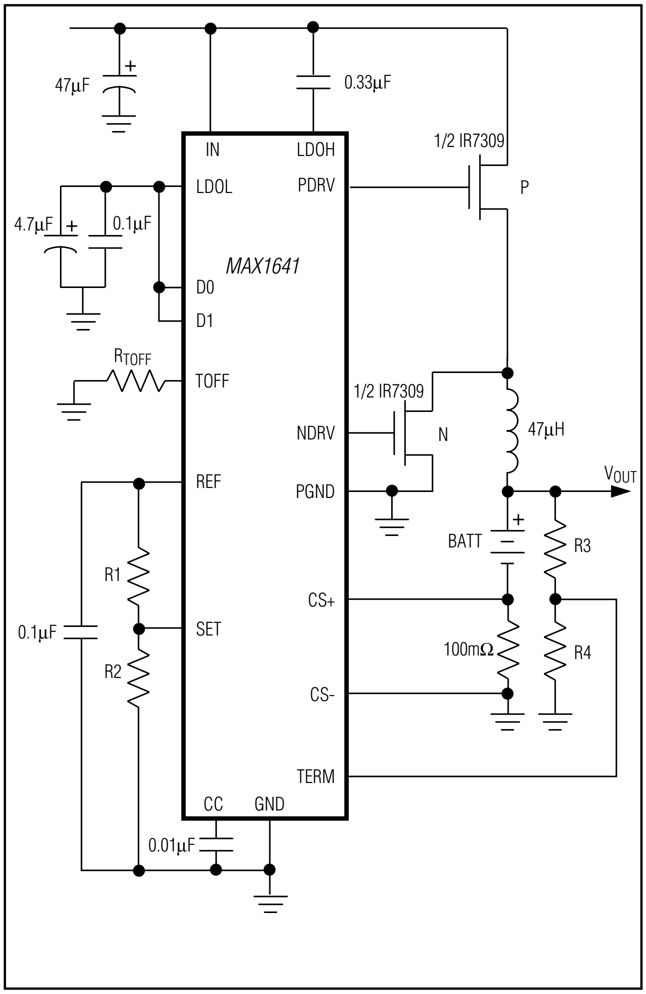


Figure 1a. Standard Application Circuit

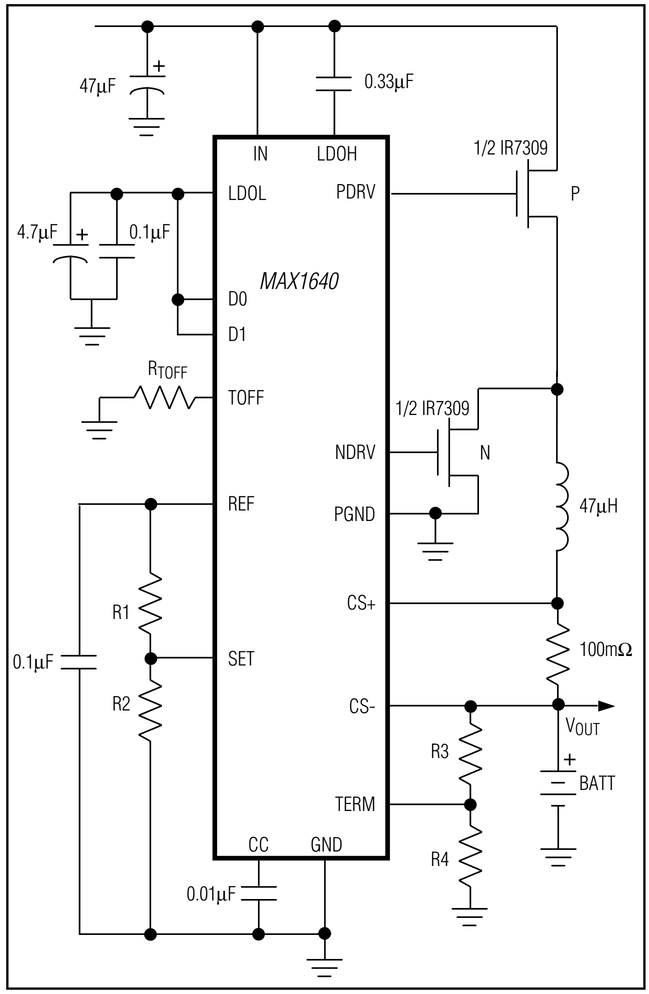


Figure 1b. Standard Application Circuit

Detailed Description

The MAX1640/MAX1641 switch-mode current sources utilize a hysteretic, current-mode, step-down pulse-width-modulation (PWM) topology with constant off-time. Internal comparators control the switching mechanism. These comparators monitor the current through a sense resistor (R_{SENSE}) and the voltage at TERM. When inductor current reaches the current limit [(V_{CS+} - V_{CS-}) / R_{SENSE}], the P-channel FET turns off and the N-channel FET synchronous rectifier turns on. Inductor energy is delivered to the load as the current ramps down. This ramp rate depends on R_{TOFF} and inductor values. When off-time expires, the P-channel FET turns back on and the N-channel FET turns off.

Two digital inputs, D0 and D1, select between four possible current levels (Table 1). In pulse-trickle mode, the part operates for 12.5% of the period set by R_{TOFF}, resulting in a lower current for pulse-trickle charging. See the *Functional Diagram*. Figures 1a and 1b show the standard application circuits.

Charge Mode: Programming the Output Currents

The sense resistor, R_{SENSE}, sets two charging current levels. Choose between these two levels by holding D0 high, and toggling D1 either high or low (Table 1). The fast-charge current level equals V_{CS} / R_{SENSE} where V_{CS} is the full-scale current-sense voltage of 150mV. Alternatively, calculate this current by V_{REF} / ($13.3R_{SENSE}$). The top-off current equals V_{SET} / ($13.3R_{SENSE}$). A resistor-divider from REF to GND programs the voltage at SET (Figure 2).

The voltage at SET is given by:

$$R1 = R2 (V_{REF} / V_{SET} - 1); 10k\Omega < R2 < 300k\Omega$$

where V_{REF} = 2V and V_{SET} is proportional to the desired output current level.

Table 1. Selecting Output Current Levels

D1	DO	MODE	OUTPUT CURRENT (A)
0	0	OFF	0
0	1	Top-Off	V_{SET} / (13.3R_{SENSE})
1	0	Pulse-Trickle	V_{SET} / (13.3R_{SENSE}) 12.5% duty cycle
1	1	Fast Charge	V_{REF} / (13.3R_{SENSE})

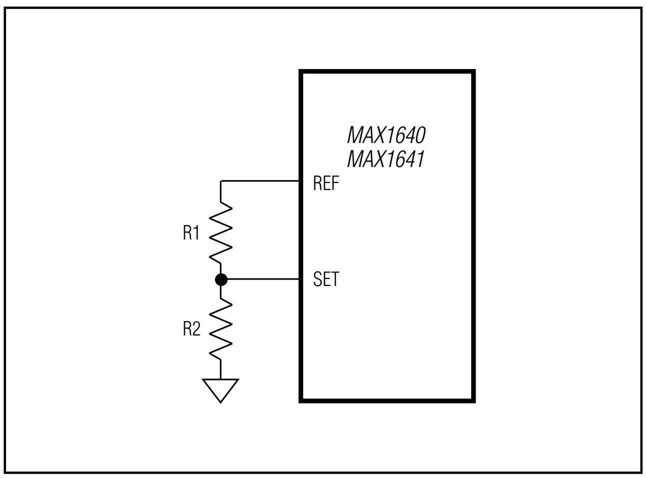


Figure 2. Adjusting the Output Current Level

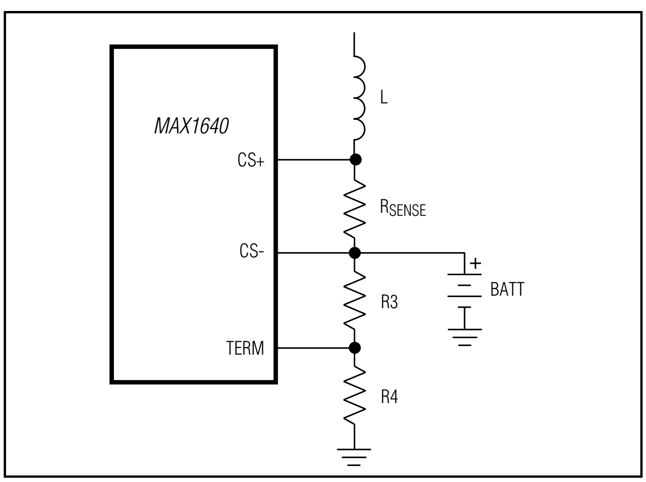


Figure 3a. Setting the Maximum Output Voltage Level

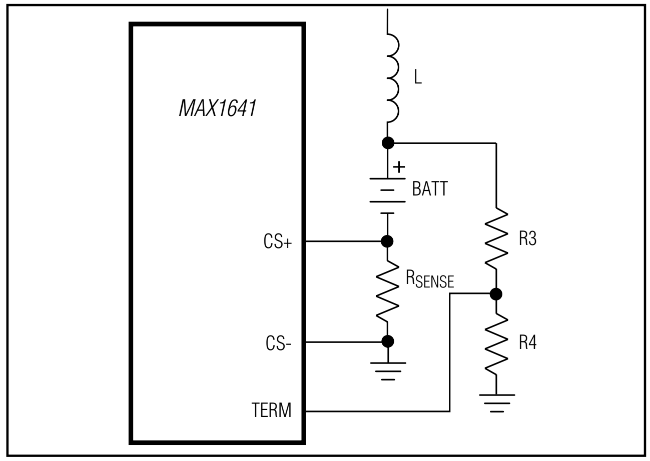


Figure 3b. Setting the Maximum Output Voltage Level

The MAX1640/MAX1641 are specified for V_{SET} between 0V and V_{REF}. For $V_{SET} > V_{REF}$, output current increases linearly (with reduced accuracy) until it clamps at $V_{SET} \approx 4V$.

Pulse-Trickle Mode: Selecting the Pulse-Trickle Current

Pulling D0 low and D1 high selects pulse-trickle mode. This current equals V_{SET} / (13.3R_{SENSE}) and remains on for 12.5% of the period set by R_{TOFF}. Pulse-trickle current maintains full charge across the battery and can slowly charge a cold battery before fast charging commences.

$$PERIOD = 3.2 \times 10^{-7} \times R_{TOFF} (sec)$$

Off Mode: Turning Off the Output Current

Pulling D0 and D1 low turns off the P-channel FET and hence the output current flow. This mode also controls end of charge and protects the battery against excessive temperatures.

Setting the Maximum Output Voltage Level

The maximum output voltage should be programmed to a level higher than the output/battery voltage (I_{LOAD} x R_{LOAD}). An external resistor-divider between the output and ground (Figure 3) sets the voltage at TERM. Once the voltage at TERM exceeds the reference, the internal comparator turns off the P-channel FET, terminating current flow. Select R4 in the 10kΩ to 500kΩ range. R3 is given by:

$$R3 = R4 ((V_{OUT} / V_{TERM}) - 1)$$

where V_{TERM} = 2V and V_{OUT} is the desired output voltage.

Programming the Off-Time

When programming the off-time, consider such factors as maximum inductor current ripple, maximum output voltage, inductor value, and inductor current rating. The output current ripple is less than the inductor current ripple and depends heavily on the output capacitor's size.

Perform the following steps to program the off-time:

1) Select the maximum output current ripple. I_R(A)
2) Select the maximum output voltage. V_{OUT}(MAX)(V)
3) Calculate the inductor value range as follows:

   $L_{MIN} = (V_{OUTMAX} \times 1\mu s) / I_R$

   $L_{MAX} = (V_{OUTMAX} \times 10\mu s) / I_R$
4) Select an inductor value in this range.
5) Calculate t_{OFF} as follows:

$$t_{OFF} = \frac{L \times I_R}{V_{OUTMAX}}$$

6) Program t_{OFF} by selecting R_{TOFF} from:

$$R_{TOFF} = (29.3 \times 10^9) \times t_{OFF}$$

7) Calculate the switching frequency by:

$$fs = 1 / (t_{ON} + t_{OFF})$$

   where $t_{ON} = (I_R \times L) / (V_{IN} - V_{OUT})$ and $I_R = (V_{OUT} \times t_{OFF}) / L$. L is the inductor value, V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_R is the output peak-to-peak current ripple.

Note that R_{TOFF} sets both the off-time and the pulse-trickle charge period.

Reference

The on-chip reference is laser trimmed for a precise 2V at REF. REF can source no more than 50µA. Bypass REF with a 0.1µF capacitor to ground.

Constant-Current Loop: AC Loop Compensation

The constant-current loop's output is brought out at CC. To reduce noise due to variations in switching currents, bypass CC with a 1nF to 100nF capacitor to ground. A large capacitor value maintains a constant average output current but slows the loop response to changes in switching current. A small capacitor value speeds up the loop response to changes in switching current, generating increased ripple at the output. Select C_{CC} to optimize the ripple vs. loop response.

Synchronous Rectification

Synchronous rectification reduces conduction losses in the rectifier by shunting the Schottky diode with a low-resistance MOSFET switch. In turn, efficiency increases by about 3% to 5% at heavy loads. To prevent cross-conduction or "shoot-through," the synchronous rectifier turns on shortly after the P-channel power MOSFET turns off. The synchronous rectifier remains off for 90% of the off-time. In low-cost designs, the synchronous rectifier FET may be replaced by a Schottky diode.

Table 2. Component Manufacturers

COMPONENT	MANUFACTURER	
Inductor	Sumida	CDRH125 series
	Coilcraft	D03316P series
	Coiltronics	UP2 series
MOSFETs	International Rectifier	IRF7309
	Siliconix	S14539DY
Sense Resistor	Dale	WSL-2010 series
	IRC	LR2010-01 series
Capacitors	AVX	TPS series
	Sprague	595D series
Rectifier	Motorola	MBAR5340t3
		IN5817-IN5822
	Nihon	NSQ03A04

Component Selection

External Switching Transistors

The MAX1640/MAX1641 drive an enhancement-mode P-channel MOSFET and a synchronous-rectifier N-channel MOSFET (Table 2).

When selecting a P-channel FET, some important parameters to consider are on-resistance ($r_{DS(ON)}$), maximum drain-to-source voltage (V_{DS} max), maximum gate-to-source voltage (V_{GS} max), and minimum threshold voltage (V_{TH} min).

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. Switching losses affect the upper MOSFET only (P-channel), since the Schottky rectifier or the N-FET body diode clamps the switching node before the synchronous rectifier turns on.

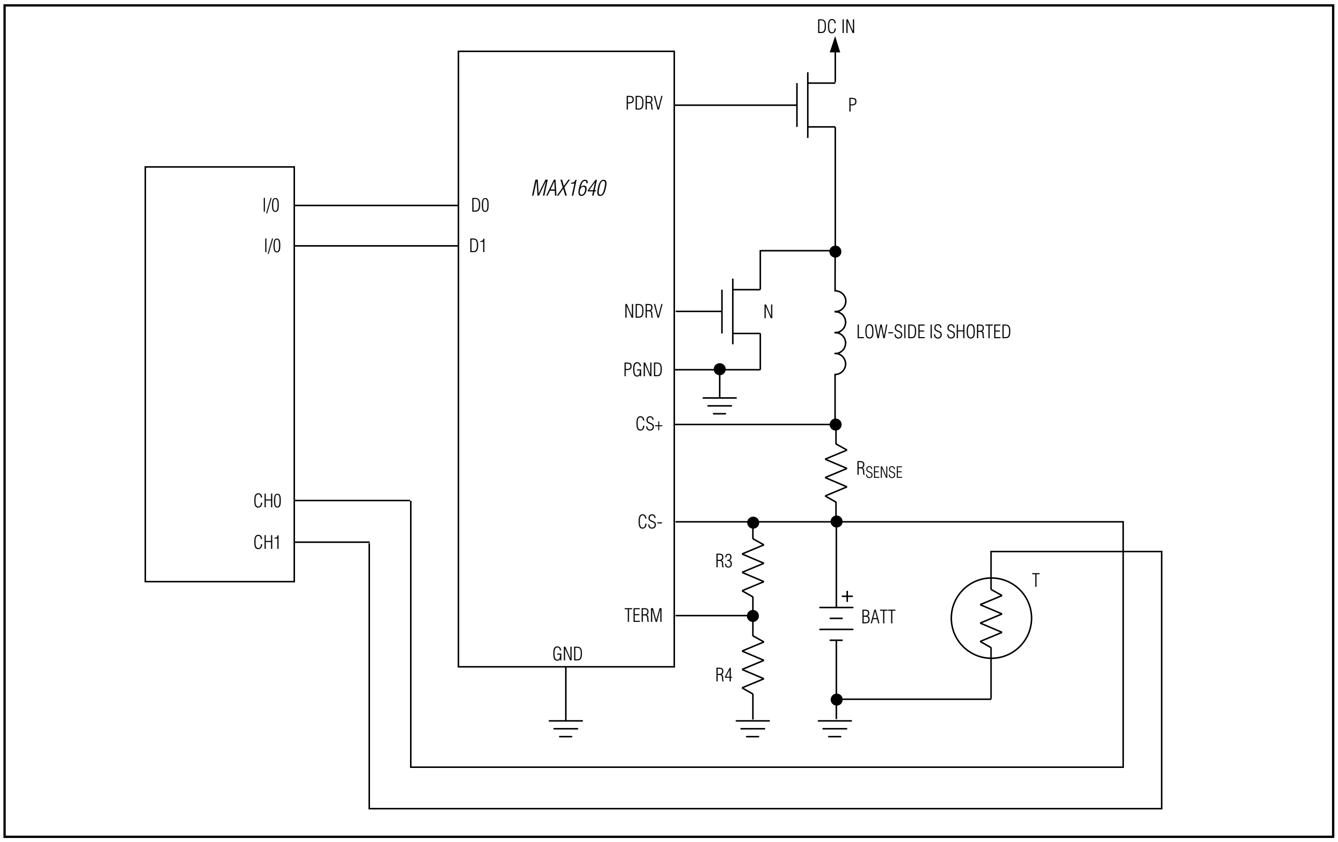


Figure 4. Microcontroller Battery Charger

Rectifier Diode

If an N-channel MOSFET synchronous rectifier is not used, a Schottky rectifier is needed. The MAX1640/MAX1641's high switching frequency demands a high-speed rectifier (Table 2). Schottky diodes such as the 1N5817–1N5822 are recommended. Make sure the Schottky diode's average current rating exceeds the peak current limit and that its breakdown voltage exceeds the output voltage (V_{OUT}). For high-temperature applications, Schottky diodes may be inadequate due to their high leakage current; high-speed silicon diodes such as the MUR105 or EC11FS1 can be used instead. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantage of high leakage current. If the application uses an N-channel MOSFET synchronous rectifier, a parallel Schottky diode is usually unnecessary except with very high charge current (> 3 amps). Best efficiency is achieved with both an N-channel MOSFET and a Schottky diode.

Inductor Value

Refer to the section *Programming the Off-Time* to select the proper inductor value. There is a trade-off between inductor value, off-time, output current ripple, and switching frequency.

Applications Information

All-Purpose Microcontroller Battery Charger: NiCd, NiMH

In applications where a microcontroller is available, the MAX1640/MAX1641 can be used as a low-cost battery charger (Figure 4). The controller takes over fast charge, pulse-trickle charge, charge termination, and other smart functions. By monitoring the output voltage at V_{OUT}, the controller initiates fast charge (set D0 and D1 high), terminates fast charge and initiates top-off (set D0 high and D1 low), enters trickle charge (set D0 low and D1 high), or shuts off and terminates current flow (set D0 and D1 low).

Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. High-current ground paths should be connected in a star configuration to PGND. These traces should be wide to reduce resistance and as short as possible to reduce stray inductance. All low-current ground paths should be connected to GND. Place the input bypass capacitor as close as possible to IN. See the MAX1640 EV kit for layout example.

Chip Information

PROCESS: BiCMOS

Package Information

(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QSOP	E16+1	21-0055

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	5/09	Added lead-free package to *Ordering Information*, corrected R3 equation, updated *Pin Description* and figure references	1–8, 10, 11

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000