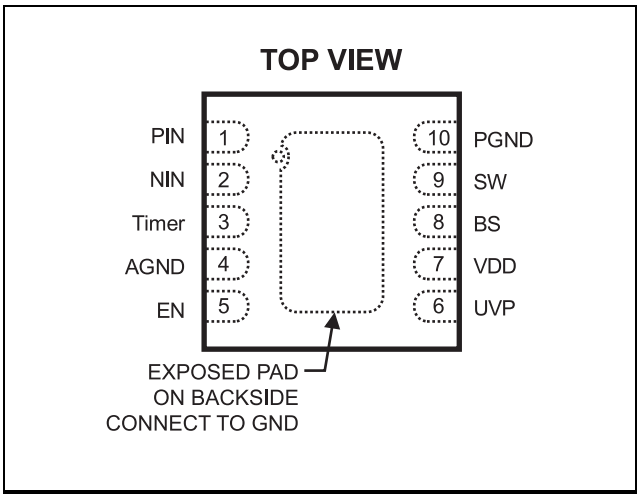
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP7747DQ	QFN10 (3mm x 3mm)	AAZ	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP7747DQ–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP7747DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 40V
BS Voltage ..... V_{SW} – 0.3V to V_{SW} + 6.5V
Enable Voltage V_{EN} ..... -0.3V to +6V
V_{UVP}, V_{SW}, V_{PIN}, V_{NIN} ..... -1V to V_{DD} + 1V
AGND to PGND ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 2.5W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD} ..... 9.5V to 36V
Operating Junct. Temp. (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

3x3 QFN10	50	12	°C

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5, 6)

V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Standby Current		V_{EN} = 0V, NIN=PIN=Float		70		μA
Quiescent Current	I_Q	SW=Low		1.5	3.0	mA
Output Drivers						
SW On Resistance		Sourcing and Sinking		0.25		Ω
Short Circuit Current		Sourcing and Sinking		4.5		A
Inputs						
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.0		V
EN Enable Input Current		V_{EN} = 5V		5		μA
External Undervoltage Detection	V_{UVP}			4		V
External Undervoltage Detection Dysteresis Voltage	V_{Hys}			0.3		V
Thermal Shutdown						
Thermal Shutdown Trip Point		T_J Rising		150		°C
Thermal Shutdown Hysteresis				30		°C

Note:

5) The device is not guaranteed to function outside its operating rating.

6) Electrical Characteristics are for the IC only with no external components except bypass capacitors.

OPERATING SPECIFICATIONS (7)

Circuit of Figure 3, V_{DD} = 24V, Gain=8.25V/V; V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Standby Current		V_{EN} = 0V			90		µA
Quiescent Current		Switching, no load			13		mA
Power Output		f = 1kHz, THD+N = 10%, 4Ω Load			19.3		W
		f = 1kHz, THD+N = 10%, 8Ω Load			10.6		W
THD+ Noise		P_{OUT} = 1W, f = 1kHz, 4Ω Load			0.06		%
		P_{OUT} = 1W, f = 1kHz, 8Ω Load			0.02		%
Efficiency		f = 1kHz, P_{OUT} = 19.3W, 4Ω Load			91		%
		f = 1kHz, P_{OUT} = 10.6W, 8Ω Load			96		%
Maximum Power Bandwidth					20		kHz
Dynamic Range					97		dB
Noise Floor		A-Weighted			103		µV
Power Supply Rejection		V_{CC}=24V, Gain=8.25V/V, V_{RIPPLE}=200mV_{PP} C_R=100µF	f = 1kHz		-59		dB
			f = 217Hz		-59		dB

Note:

7) Operating Specifications are for the IC in Typical Application circuit (Figure 3).

PIN FUNCTIONS

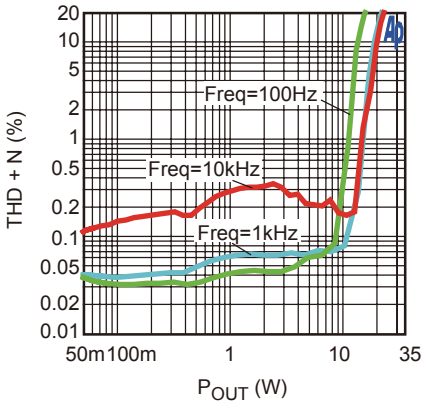
Pin #	Name	Description
1	PIN	Internal analog reference (VDD/2), connect a bypass capacitor from PIN to AGND (10µF).
2	NIN	Amplifier Negative Input. Drive the input signal and close the feedback loop at NIN.
3	Timer	Internal timer input. A capacitor from Timer to AGND sets the internal timer and controls the slew rate of start up source current.
4	AGND	Analog Ground. Connect AGND to PGND at a single point.
5	EN	Enable Input. Drive EN high to turn on the amplifier, low to turn it off.
6	UVP	Under-voltage protection reference input
7	VDD	Power Supply Input.
8	BS	High-Side MOSFET Bootstrap Input. A capacitor from BS to SW supplies the gate drive current to the internal high-side MOSFET.
9	SW	Switched Power Output. Connect the LC filter between SW and the output coupling capacitor.
10	PGND	Power Ground. Connect PGND to AGND at a single point.
	Exposed Pad	Connect exposed pad to GND plane for proper thermal performance.

TYPICAL PERFORMANCE CURVES

Circuit of Figure 3, V_{EN}=5V, A_V=8.25V/V, T_A = +25°C, unless otherwise noted.

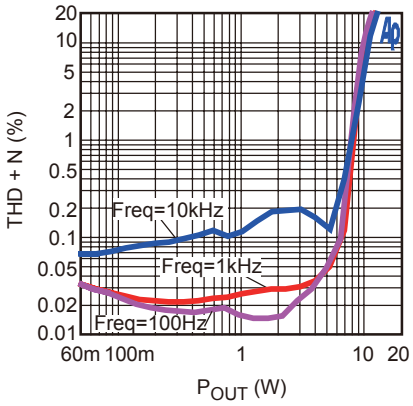
THD+N vs. Pout

V_{DD}=24V, R_{LOAD}=4Ω



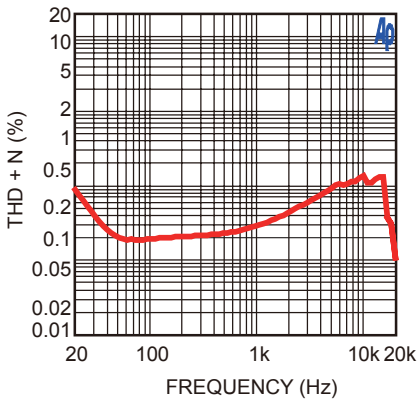
THD+N vs. Pout

V_{DD}=24V, R_{LOAD}=8Ω



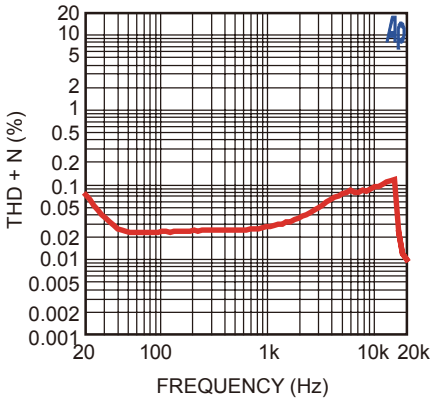
THD+N vs. Frequency

V_{DD}=24V, R_{LOAD}=4Ω, P_{OUT}=1W



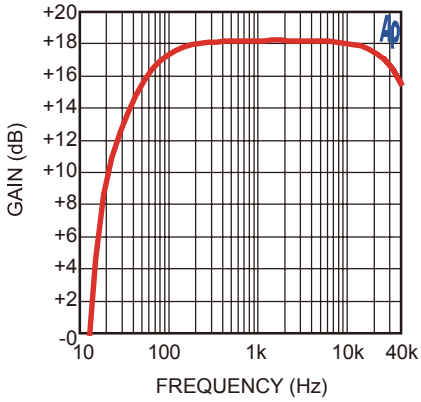
THD+N vs. Frequency

V_{DD}=24V, R_{LOAD}=8Ω, P_{OUT}=1W



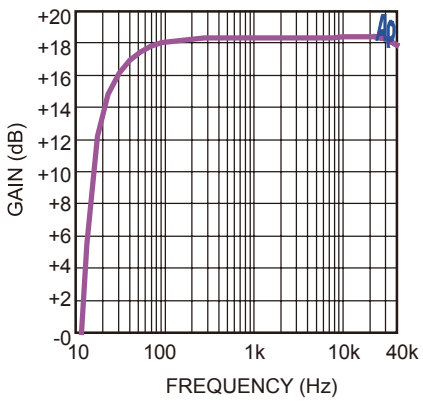
Frequency Response

V_{DD}=24V, R_{LOAD}=4Ω



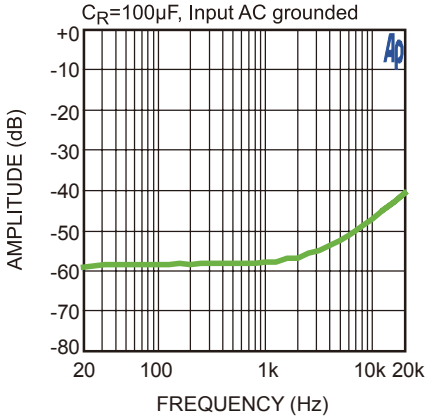
Frequency Response

V_{DD}=24V, R_{LOAD}=8Ω



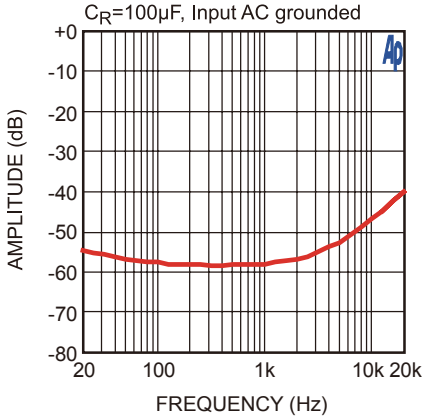
Power Supply Rejection Ratio

V_{DD}=24V, R_{LOAD}=4Ω, V_{RIPPLE}=0.3V_{PP}, C_R=100µF, Input AC grounded



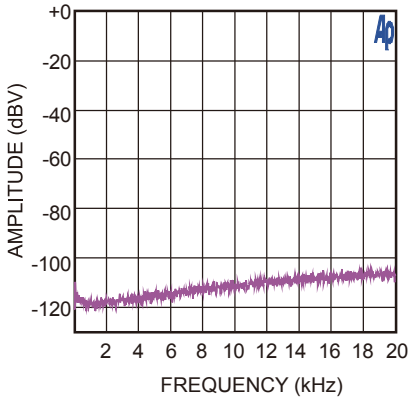
Power Supply Rejection Ratio

V_{DD}=24V, R_{LOAD}=8Ω, V_{RIPPLE}=0.3V_{PP}, C_R=100µF, Input AC grounded



FFT Noise Floor

V_{DD}=24V, R_{LOAD}=4Ω

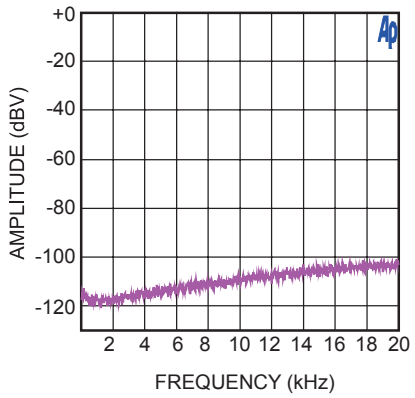


TYPICAL PERFORMANCE CURVES *(continued)*

Circuit of Figure 3, V_{EN}=5V, A_V=8.25V/V, T_A = +25°C, unless otherwise noted.

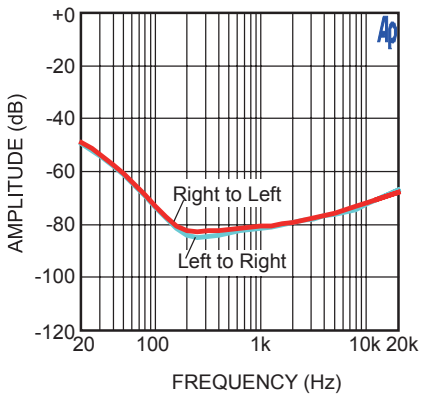
FFT Noise Floor

V_{DD}=24V, R_{LOAD}=8Ω



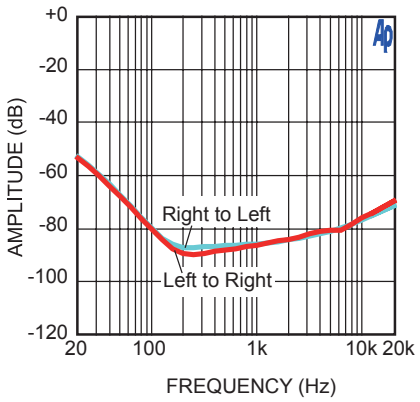
Cross Talk

V_{DD}=24V, R_{LOAD}=4Ω, P_{OUT}=5W



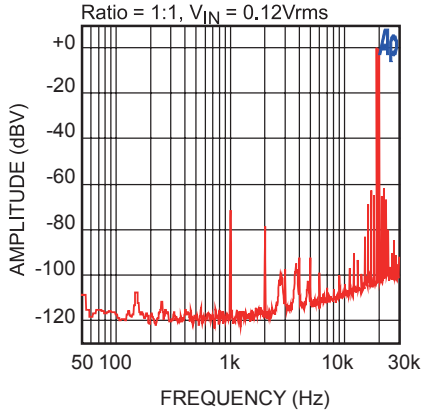
Cross Talk

V_{DD}=24V, R_{LOAD}=8Ω, P_{OUT}=5W



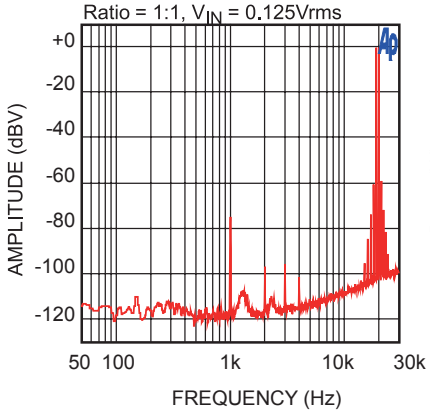
IHF-IMD

V_{DD} = 24V, R_{LOAD} =4Ω,
Test Tones: 19kHz and 20kHz,
Ratio = 1:1, V_{IN} = 0.12Vrms



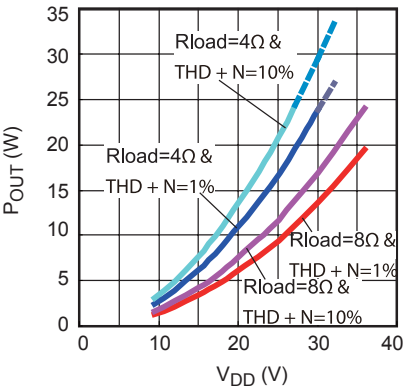
IHF-IMD

V_{DD} = 24V, R_{LOAD} =8Ω,
Test Tones: 19kHz and 20kHz,
Ratio = 1:1, V_{IN} = 0.125Vrms



P_{OUT} vs. V_{DD}

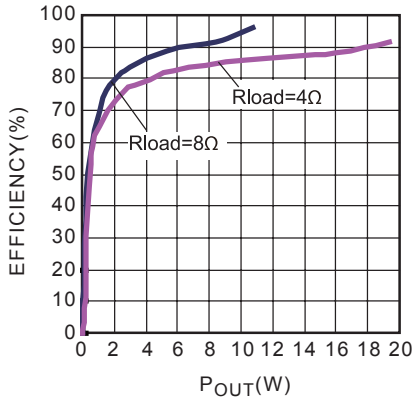
Input Signal Frequency =1kHz



Note: Dashed Lines represent thermally limited regions.

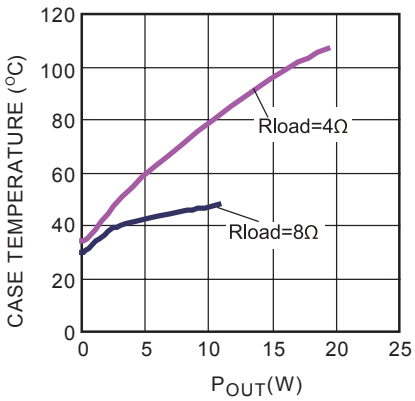
Efficiency vs. P_{OUT}

V_{DD} = 24V,
Input Signal Frequency=1kHz



Thermal Rise vs. P_{OUT}

V_{DD} = 24V,
Input Signal Frequency=1kHz



BLOCK DIAGRAM

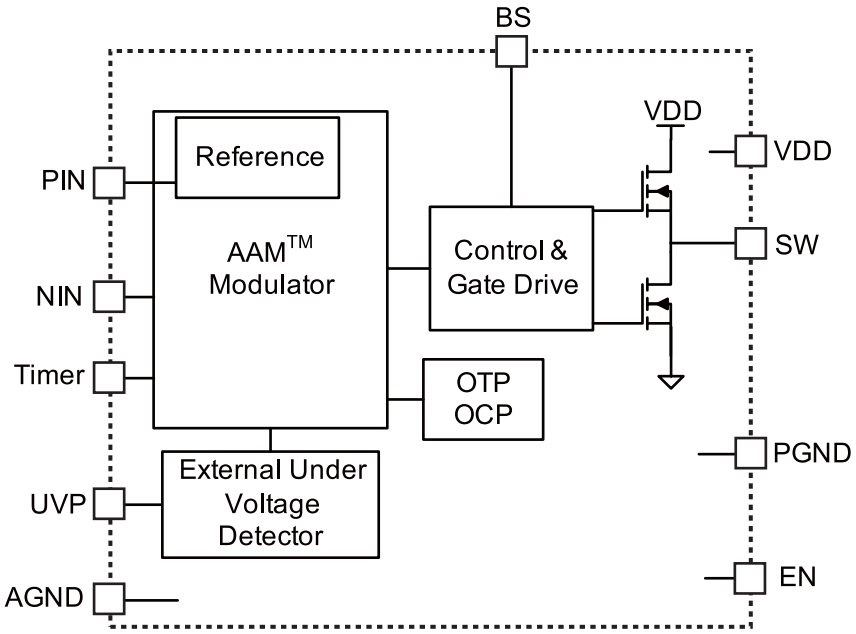


Figure1—Function Block Diagram

OPERATION

The MP7747 is a single-ended Class D audio amplifier. It uses the Monolithic Power Systems patented Analog Adaptive Modulation™ to convert the audio input signal into pulses. These pulses drive an internal high-current output stage and, when filtered through an external inductor-capacitor filter, reproduce the input signal across the load. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared to Class A, B or A/B amplifiers while maintaining high fidelity and low distortion.

The amplifier uses differential input to the modulator. PIN is the positive input and NIN is the negative input. PIN is set to half the DC power supply input voltage (V_{DD}/2) by the internal circuit, so the common mode voltage of the input NIN should be set to half the DC power supply input voltage (V_{DD}/2). The input capacitor C_{IN} couple the AC signal at the input.

The amplifier voltage gain is set by the combination of the input resister R_{IN} and the feedback resistor R_{FB} and is calculated by the equation:

$$AV = \frac{-R_{FB}}{R_{IN}}$$

The output driver stage uses two 250mΩ N-Channel MOSFETs to deliver the pulses to the LC output filter which in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than the source by the bootstrap capacitor between SW and BS. While the output is driven low, the bootstrap capacitor is charged from V_{DD} through an internal circuit on the MP7747. The gate of the high-side MOSFET is driven high from the voltage at BS, forcing the MOSFET gate to a voltage higher than V_{DD} and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

Pop Elimination

The capacitor C_{OUT} blocks the DC signal and pass only AC signals to the load. To insure that the amplifier passes low frequency signals, the time constant of C_{OUT}*R_{LOAD} needs to be long. However, when EN is asserted, the capacitor charges over a long period and in a normal amplifier can result in a turn on and turn off "pop."

The MP7747 integrates a source current function to charge the AC coupling capacitor Cout and Cin at the start up moment. The start up source current slew rate is adjustable by selecting different capacitance of timer capacitor Ctimer. The larger the Ctimer capacitance is, the smaller the start up current slew rate is. The recommended 2.2μF capacitor Ctimer results in a start up current slew rate of approximately 20mA/350ms which would help to minimize the turn on pop.

After driving EN pin low, output SW will be set to high impedance immediately which would help to eliminate the turn off pop.

Short Circuit/Overload Protection

The MP7747 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are measured and if the current exceeds the 4.5A short circuit current limit, both MOSFETs are turned off. The MP7747 then restarts with the same start up sequence that is used for normal starting to prevent a pop from occurring after a short circuit condition is removed.

Mute/Enable Function

The MP7747 EN input is an active high enable control. To enable the MP7747, drive EN with a 2.0V or greater voltage. To disable the amplifier, drive it below 0.4V. While the MP7747 is disabled, the VDD operating current is less than 100μA and the output driver MOSFETs are turned off.

Programmable UVP

MP7747 integrate programmable UVP function, which can be used to shutdown the MP7747 to escape the pop, by controlling the UVP node voltage. The corresponding circuit is shown in the followed figure 2. If the UVP pin is NC, the default VDD UVP voltage (rising threshold) is 8.4V since there is internal voltage divided circuit.

The VDD UVP voltage (rising threshold) can be flexibly adjusted by controlling UVP pin voltage. The recommended VDD shutdown voltage is from 9.5V to power supply. As shown in the figure 2, if external resistor RH and RL is low enough (e.g. RH, RL < 50kΩ) compared with internal 500kΩ and 550kΩ resistor, the VDD shutdown voltage (rising threshold) can be calculated by the equation:

$$V_{VDD\_shutdown} = 4 * \frac{(R_H + R_L)}{R_L}$$

The hysteresis voltage can be calculated by the equation：

$$V_{hysteresis} = 0.3 * \frac{R_H + R_L}{R_L}$$

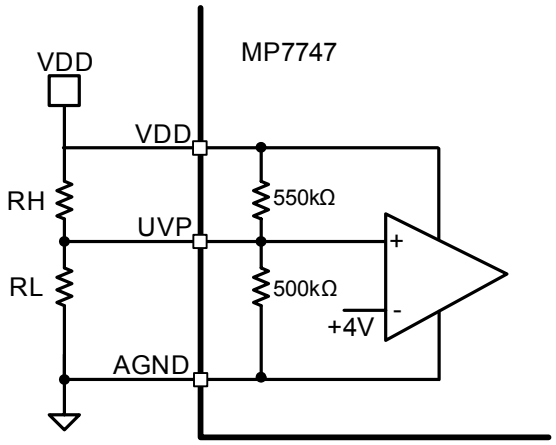


Figure 2—UVP Block Diagram

APPLICATION INFORMATION

COMPONENT SELECTION

The MP7747 uses a minimum number of external components to complete a stereo Class D audio amplifier. The circuit of Figure 3 should be suitable for most applications, and use the following sections to determine how to customize the amplifier for a particular application.

Setting the Voltage Gain

The maximum output voltage swing is limited by the power supply. To achieve the maximum power out of the MP7747 amplifier, set the gain such that the maximum input signal results in the maximum output voltage swing.

The maximum output voltage swing is $\pm V_{DD}/2$. For a given input signal voltage, where $V_{IN}(pk)$ is the peak input voltage, the maximum voltage gain is:

$$A_V(MAX) = \frac{V_{DD}}{2 \times V_{IN}(pk)}$$

This voltage gain setting results in the peak output voltage approaching it's maximum for the maximum input signal. In some cases the amplifier is allowed to overdrive slightly, allowing the THD to increase at high power levels, and so a higher gain than A_V (max) is required.

Setting the Switching Frequency

The idle switching frequency (the switching frequency when no audio input is present) is a function of several variables: the supply voltage V_{DD}, the timing capacitor C_{INT} and the feedback resistor R_{FB}. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple and increasing the output noise and distortion. Higher switching frequencies result in more power loss. The optimum quiescent switching frequency is approximately 600kHz to 700kHz. Refer to the Operating Specifications for recommended values.

Table 1—Switching Frequency vs. V_{DD}, Timing Capacitor and Feedback Resistor (see Figure 3)

Gain (V/V)	Gain (dB)	R_{FB} (kΩ)	R_{IN} (kΩ)	C_{INT}	F_{SW}	V_{DD} (V)
3.9	11.8	39	10	6.8nF	580kHz	12
8.2	18.3	82	10	3.3nF	580kHz	12
8.3	18.4	39	4.7	6.8nF	580kHz	12
12.0	21.6	120	10	2.2nF	530kHz	12
17.4	24.8	82	4.7	3.3nF	580kHz	12
25.5	28.1	120	4.7	2.2nF	530kHz	12
5.6	15.0	56	10	8.2nF	610kHz	24
8.2	18.3	82	10	5.6nF	650kHz	24
11.9	21.5	56	4.7	8.2nF	610kHz	24
12.0	21.6	120	10	4.7nF	540kHz	24
17.4	24.8	82	4.7	5.6nF	650kHz	24
25.5	28.1	120	4.7	4.7nF	540kHz	24
33.0	30.4	330	10	1.8nF	630kHz	24

Choosing the LC Filter

The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker.

The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from SW. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The quality factor (Q) of the LC filter is important. If this is too low, output noise will increase, if this is too high, then peaking may occur at high signal frequencies reducing the passband flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4Ω or 8Ω). The Q is calculated as:

$$Q = \frac{R_{LOAD}}{\omega_0 \times L} = \frac{R_{LOAD}}{2\pi \times f_0 \times L}$$

ω_0 is the characteristic frequency in radians per second and f_0 is in Hz. Use an LC filter with Q between 0.7 and 1.

The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron, or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used for multi-channel designs, make sure that the start windings of each inductor line up (all starts going toward SW pin, or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

Output Coupling Capacitor

The output AC coupling capacitor C_{OUT} serves to block DC voltages and thus passes only the amplified AC signal from the LC filter to the load. The combination of the coupling capacitor, C_{OUT} and the load resistance results in a first-order high-pass filter. The value of C_{OUT} should be selected such that the required minimum frequency is still allowed to pass. The output corner frequency (-3dB point), f_{OUT}, can be calculated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}}$$

Set the output corner frequency (f_{OUT}) at or below the minimum required frequency.

The output coupling capacitor carries the full load current, so a capacitor should be chosen such that its ripple current rating is greater than the maximum load current. Low ESR aluminum electrolytic capacitors are recommended.

Input Coupling Capacitor

The input coupling capacitor C_{IN} is used to pass only the AC signal at the input. In a typical system application, the source input signal is typically centered around the circuit ground, while the MP7747 input is at half the power supply voltage (V_{DD}/2). The input coupling capacitor transmits the AC signal from the source to the MP7747 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

Timer Capacitor

The start up source current slew rate is adjustable by selecting different capacitance of timer capacitor C_{TIMER}. The larger the C_{TIMER} capacitance is, the smaller the start up current slew rate is. It is recommended to use the C_{TIMER} which capacitance is larger than 312nF, so the start up current slew rate would be smaller than 20mA/50ms which would help to eliminate the turn on pop. The recommended 2.2μF capacitor C_{TIMER} results in a start up current slew rate of approximately 20mA/350ms.

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. The higher the power supply voltage, the more power can be delivered to a given load resistance, however if the power source voltage exceeds the maximum voltage of 36V, the MP7747 may sustain damage. The power supply rejection of the MP7747 is excellent (typically -60dB), however noise at the power supply can get to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with a smaller 1μF ceramic capacitor at the MP7747 V_{DD} supply pins.

PCB Layout

The circuit layout is critical for optimum performance and low output distortion and noise. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 4 for references.

1) Place the following components as close to the MP7747 as possible:

Bootstrap Cap

C_{BS} is used to supply the gate drive current to the internal high-side MOSFET. Place the C_{BS} as close to pins 8 (BS) and 9 (SW) as possible.

Power Supply Bypass

C_{BYP} carries the transient current for the switching power stage. To prevent overstressing of the MP7747 and excessive noise at the output, place C_{BYP} as close to pins 7 (VDD) and 10 (PGND) as possible.

Integrated Capacitors

C_{INT} is used to set the amplifier switching frequencies and are typically on the order of a few nF. Place the C_{INT} as close to pins 1 (PIN) and 2 (NIN) as possible to reduce distortion and noise.

Reference Bypass Capacitors

C_R filters the ½ VDD reference voltages. Place C_R as close to the IC as possible to improve power supply rejection and reduce distortion and noise at the output.

2) The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Please keep the filter capacitor close to the inductor.

3) When laying out the PCB, use two separate ground planes, analog ground (AGND) and power ground (PGND), and connect the two grounds together at a single point (usually around the bulk bypass capacitor) to prevent noise injection into the amplifier input to reduce distortion.

4) Keep the sensitive feedback signal trace on the input side and shield the trace with the AGND plane. Make sure that any traces carrying the switch node (SW) voltages are separated far from any input signal traces. If it is required to run the SW trace near the input, shield the input with a ground plane between the traces. If multiple amplifiers are used on a single board, make sure that each channel is physically separated to prevent crosstalk. Make sure that all inductors used on a single circuit board have the same orientation.

If multiple amplifiers are used on a single board, make sure that the power supply is routed from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of the Class D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of the EMI due to the amplifier switching can be minimized.

The power inductors are a potential source of radiated emissions. For the best EMI performance, use toroidal inductors, since the magnetic field is well contained inside the core. However toroidal inductors can be expensive to wind. For a more economical solution, use shielded gapped ferrite or shielded ferrite bobbin core inductors. These inductors typically do not contain the field as well toroidal inductors, but usually can achieve a better balance of good EMI performance with low cost.

The size of high-current loops that carry rapidly changing currents needs to be minimized. To do this, make sure that the V_{DD} bypass capacitors are as close to the MP7747 as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

TYPICAL APPLICATION CIRCUIT

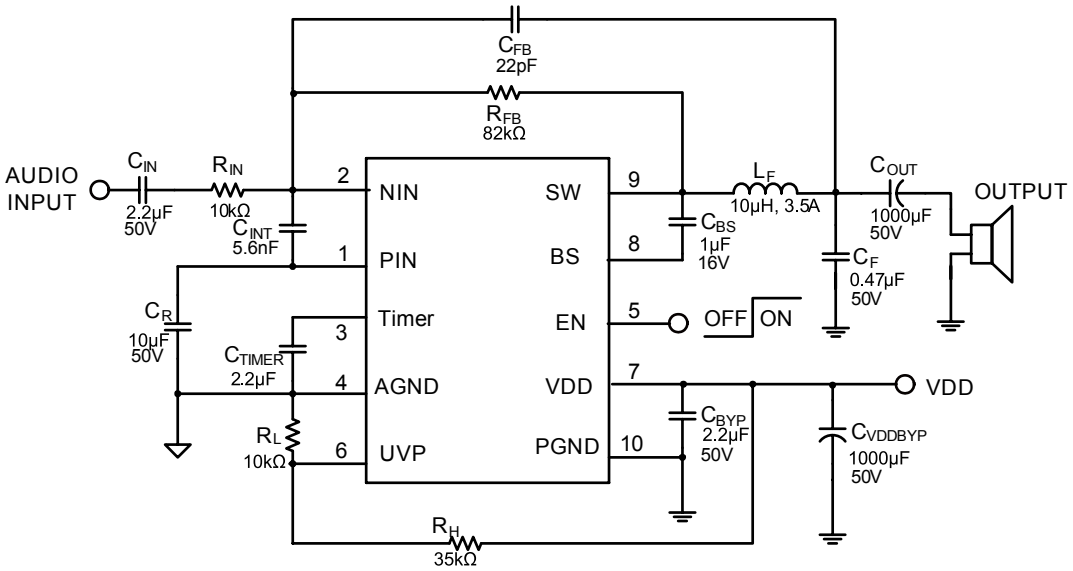
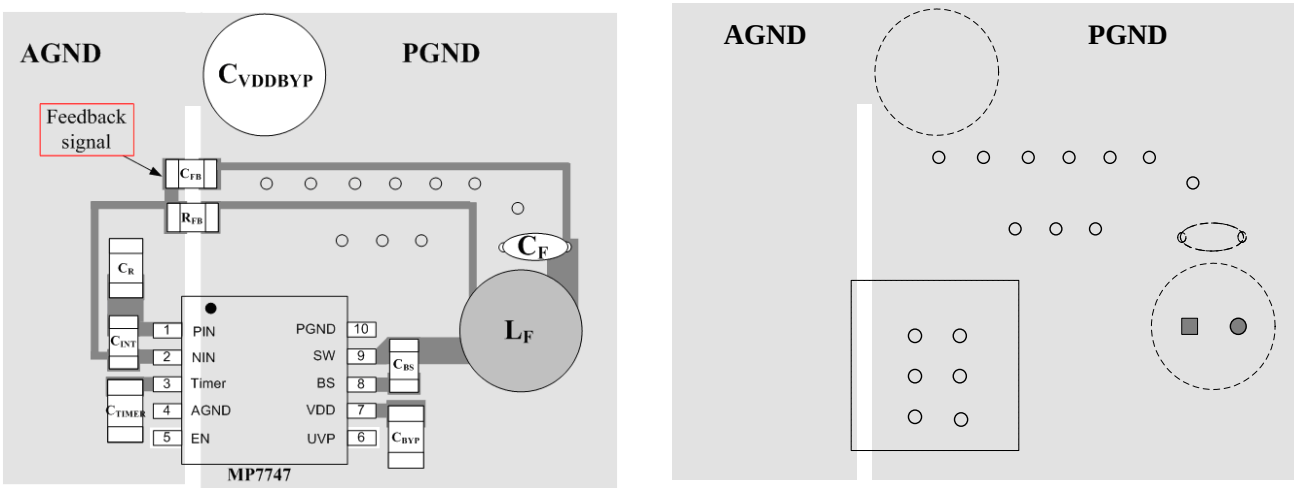


Figure 3— 24V VDD Mono Typical Application Circuit

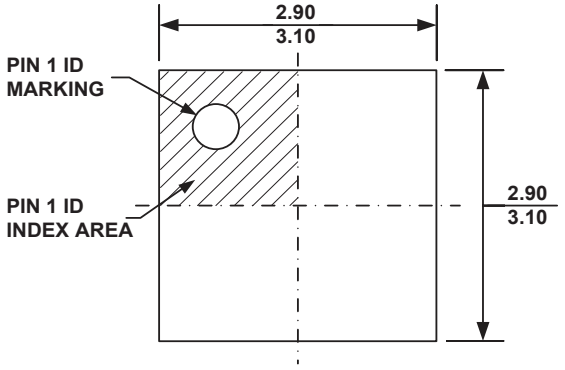


Top **Bottom**

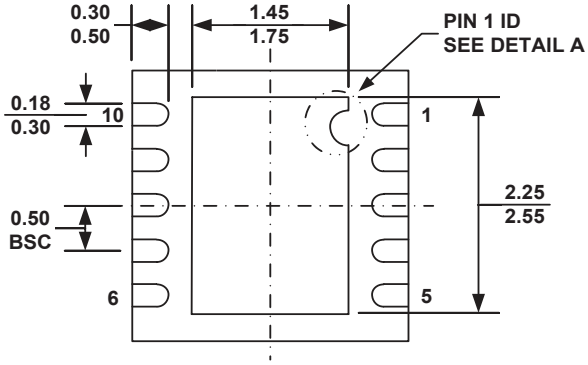
Figure 4—Reference PCB Layout

PACKAGE INFORMATION

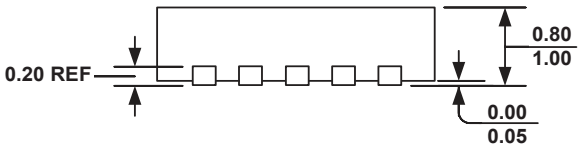
QFN10



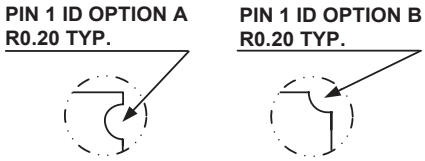
TOP VIEW



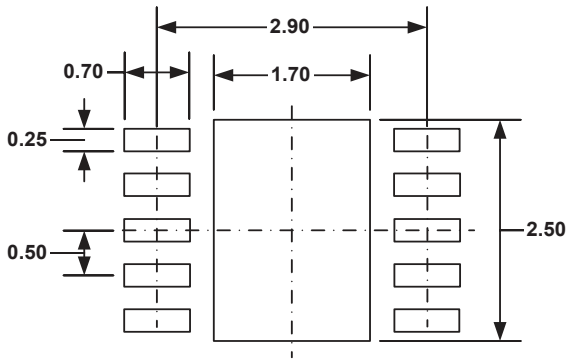
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Monolithic Power Systems (MPS):

MP7747DQ-LF-P MP7747DQ-LF-Z