

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 200\ \mu\text{Adc}$)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ($V_{DD} = 26\text{ Vdc}$, $I_D = 600\ \text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\ \text{Adc}$)	$V_{DS(on)}$	—	0.24	—	Vdc

Dynamic Characteristics

Reverse Transfer Capacitance (1) ($V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.5	—	pF
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Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 600\ \text{mA}$, $P_{out} = 60\ \text{W CW}$, $f = 1990\ \text{MHz}$

Power Gain	G_{ps}	14	15	17	dB
Drain Efficiency	η_D	48	50	—	%
Input Return Loss	IRL	—	-12	-9	dB
P_{out} @ 1 dB Compression Point	P1dB	60	65	—	W

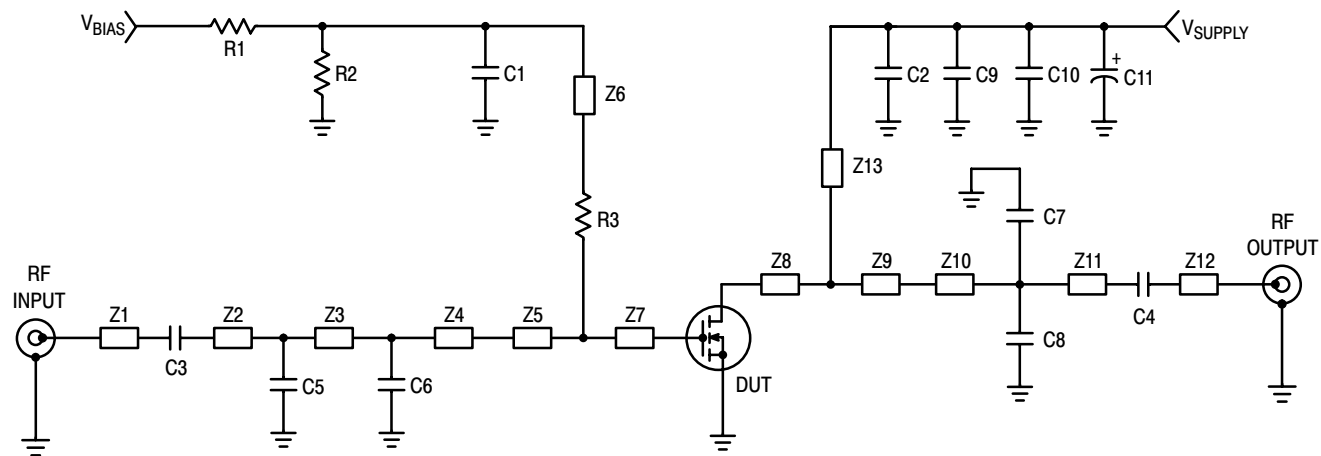
Typical GSM EDGE Performances (In Freescale Broadband Test Fixture, 50 ohm system) $V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 450\ \text{mA}$, $P_{out} = 25\ \text{W Avg.}$, 1805-1880 MHz or 1930-1990 MHz, EDGE Modulation

Power Gain	G_{ps}	—	15.5	—	dB
Drain Efficiency	η_D	—	32	—	%
Error Vector Magnitude	EVM	—	2	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-76	—	dBc

Typical CW Performances (In Freescale Broadband Test Fixture, 50 ohm system) $V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 600\ \text{mA}$, $P_{out} = 60\ \text{W}$, 1805-1880 MHz or 1930-1990 MHz

Power Gain	G_{ps}	—	15	—	dB
Drain Efficiency	η_D	—	50	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point, CW	P1dB	—	65	—	W

1. Part is internally matched both on input and output.



- | | | | |
|--------|----------------------------|------|--|
| Z1 | 0.250" x 0.083" Microstrip | Z9 | 0.485" x 1.000" Microstrip |
| Z2* | 0.950" x 0.083" Microstrip | Z10* | 0.500" x 0.083" Microstrip |
| Z3* | 0.250" x 0.083" Microstrip | Z11* | 0.895" x 0.083" Microstrip |
| Z4* | 0.315" x 0.083" Microstrip | Z12 | 0.250" x 0.083" Microstrip |
| Z5 | 0.365" x 1.000" Microstrip | Z13 | 0.200" x 0.080" Microstrip |
| Z6 | 0.680" x 0.080" Microstrip | PCB | Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$ |
| Z7, Z8 | 0.115" x 1.000" Microstrip | | |
- * Variable for tuning

Figure 1. MRF6S18060NR1(NBR1) Test Circuit Schematic — 1900 MHz

Table 6. MRF6S18060NR1(NBR1) Test Circuit Component Designations and Values — 1900 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C5	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C6	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
C7, C8	1 pF Chip Capacitors	ATC100B1R0BT500XT	ATC
C9, C10	10 μ F Chip Capacitors	C5750X5R1H106MT	TDK
C11	220 μ F, 63 V Electrolytic Capacitor, Radial	2222 - 136 - 68221	Vishay
R1, R2	10 k Ω , 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

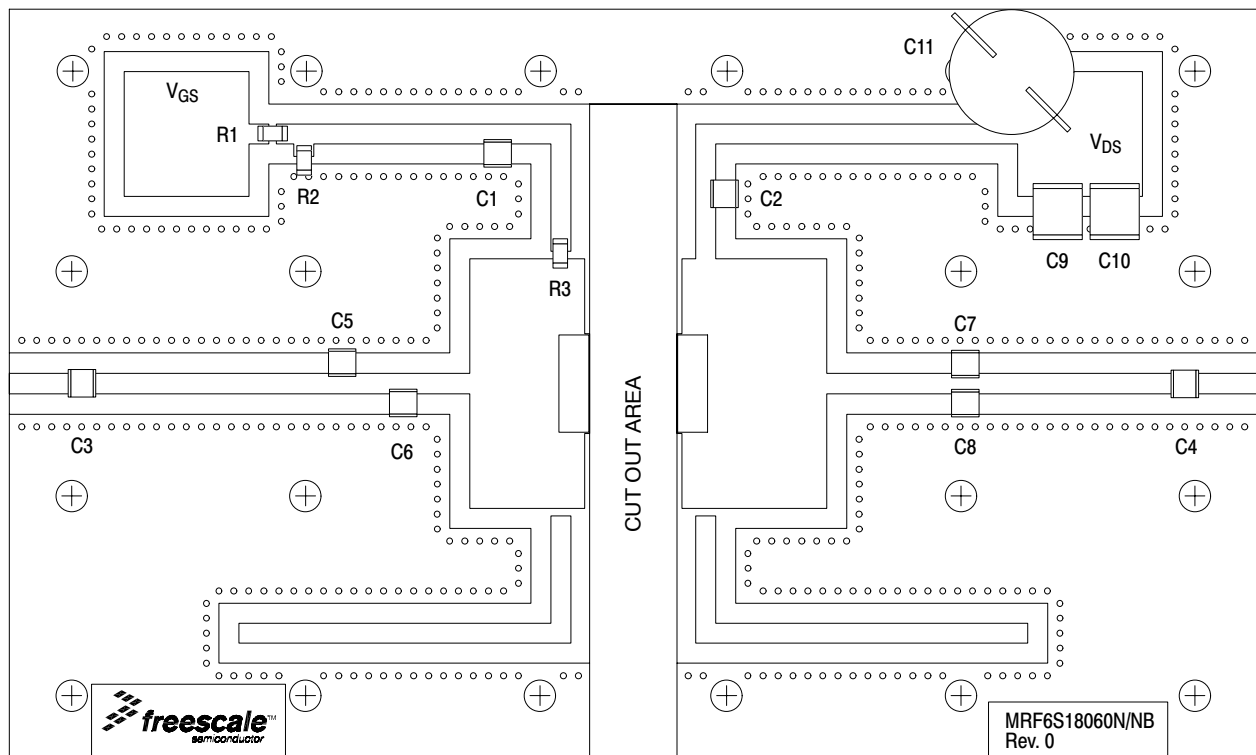


Figure 2. MRF6S18060NR1(NBR1) Test Circuit Component Layout — 1900 MHz

TYPICAL CHARACTERISTICS — 1900 MHz

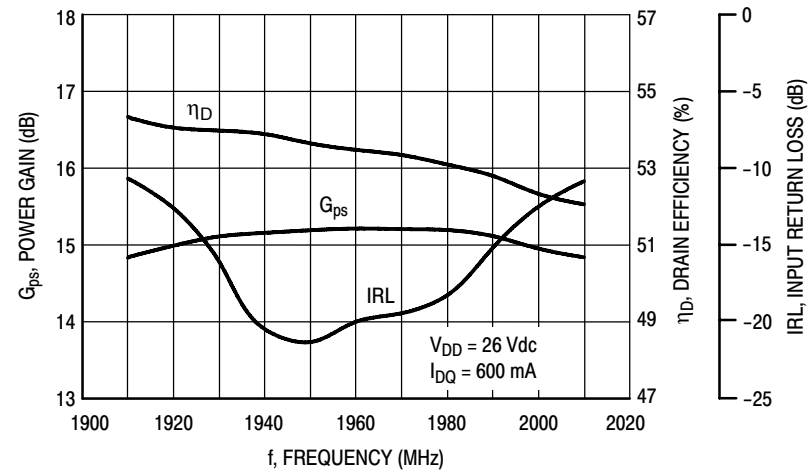


Figure 3. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ $P_{out} = 60$ Watts

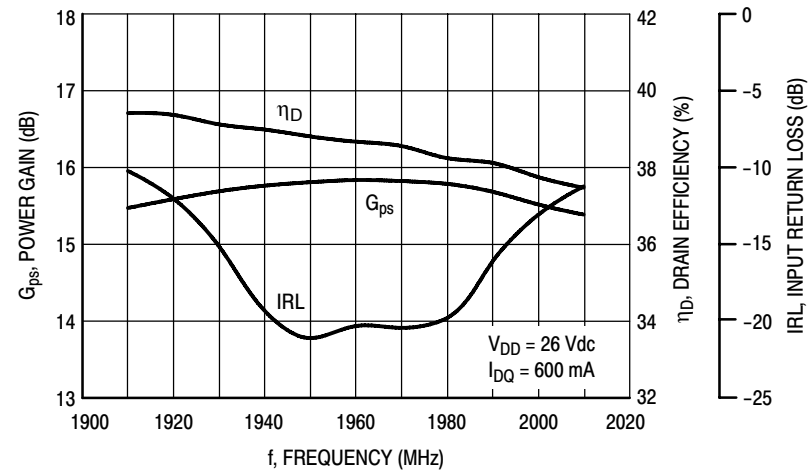


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ $P_{out} = 30$ Watts

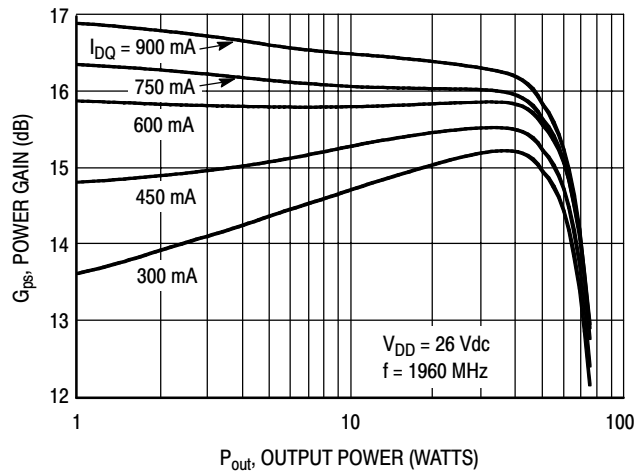


Figure 5. Power Gain versus Output Power

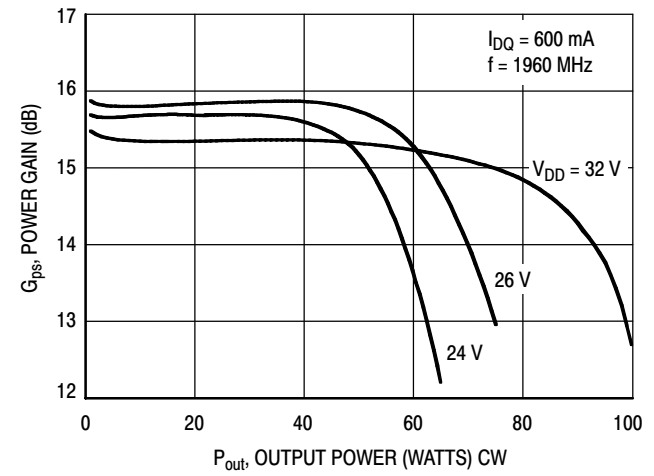


Figure 6. Power Gain versus Output Power

TYPICAL CHARACTERISTICS — 1900 MHz

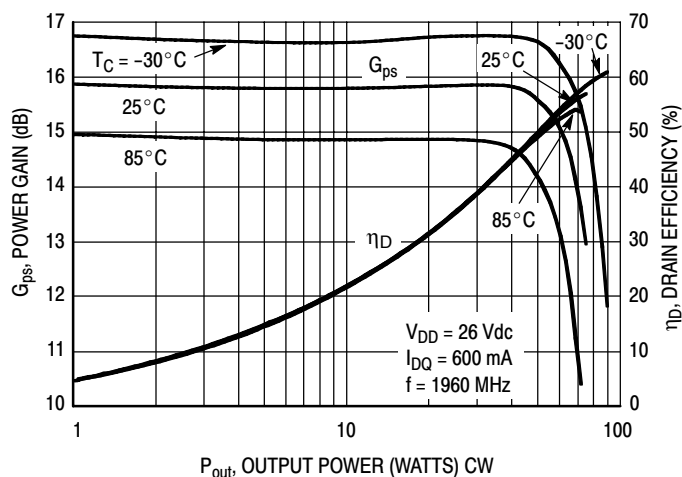


Figure 7. Power Gain and Drain Efficiency versus CW Output Power

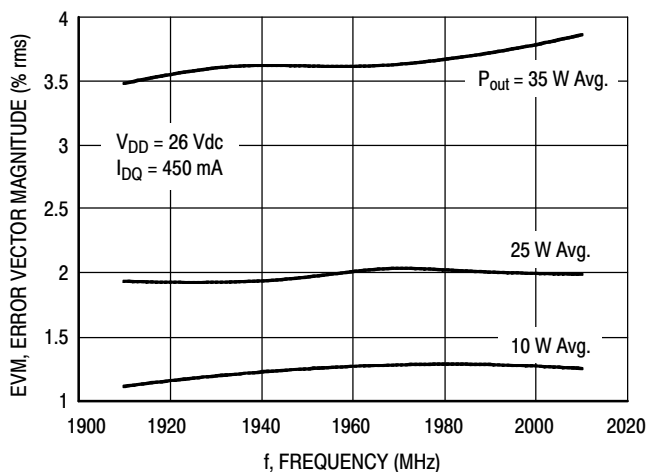


Figure 8. EVM versus Frequency

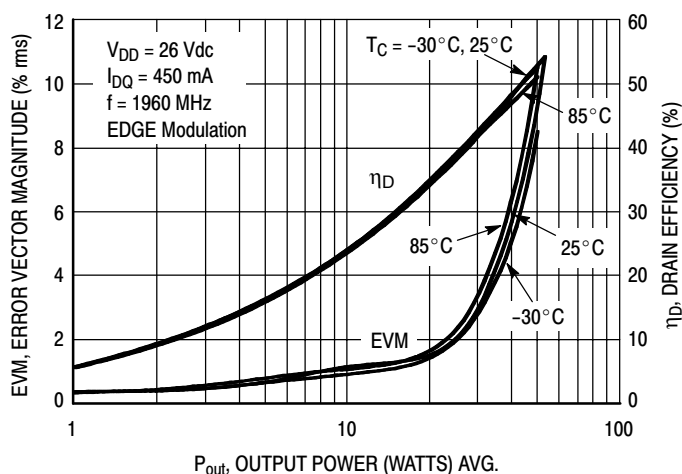


Figure 9. EVM and Drain Efficiency versus Output Power

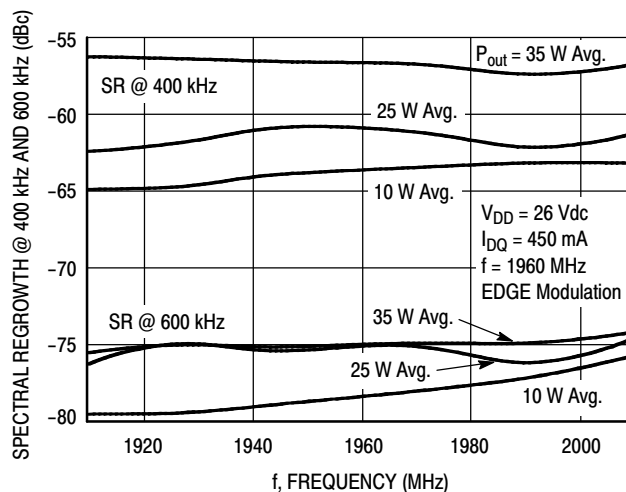


Figure 10. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

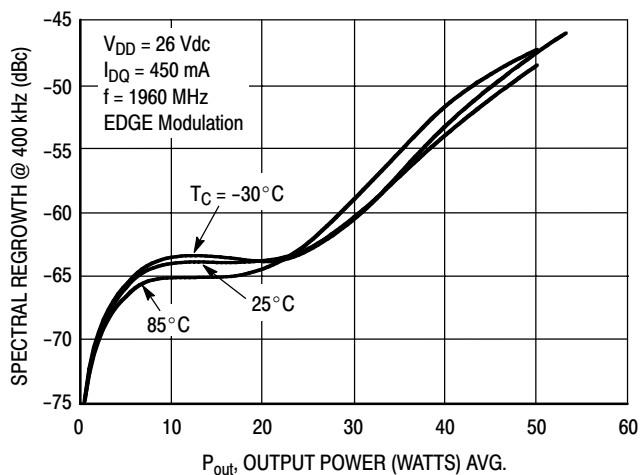


Figure 11. Spectral Regrowth at 400 kHz versus Output Power

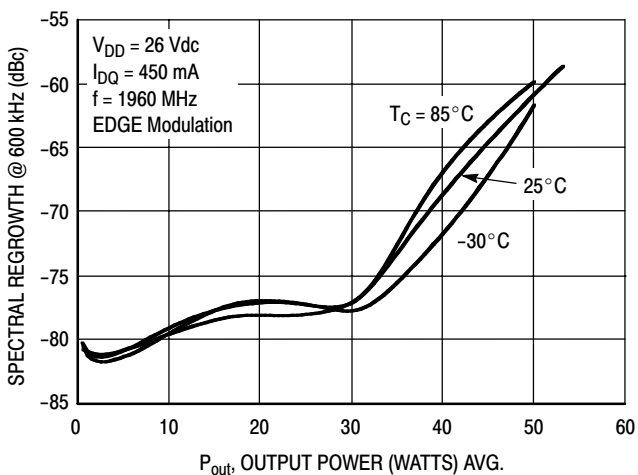
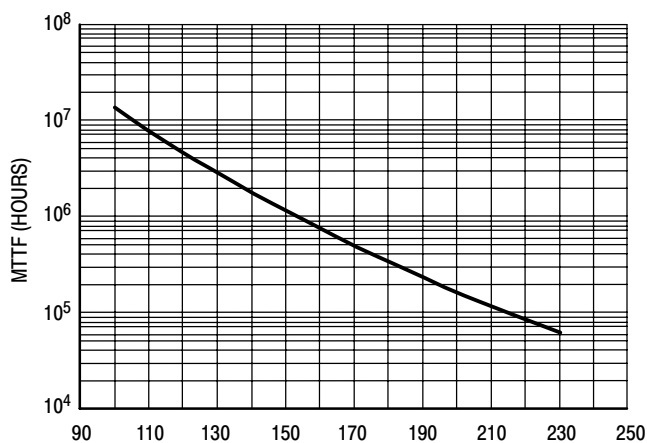


Figure 12. Spectral Regrowth at 600 kHz versus Output Power

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28$ Vdc, $P_{out} = 60$ W CW, and $\eta_D = 50\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF Factor versus Junction Temperature

GSM TEST SIGNAL

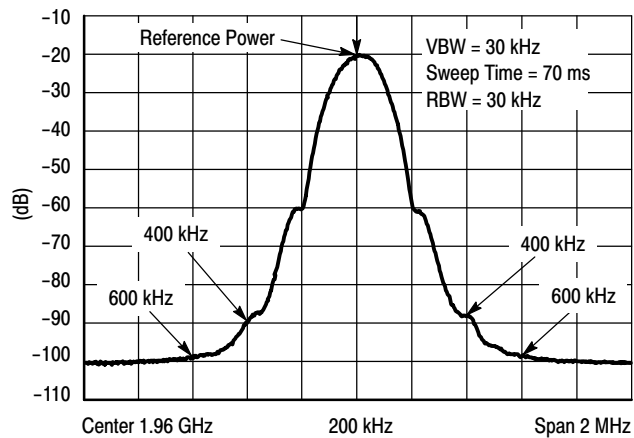
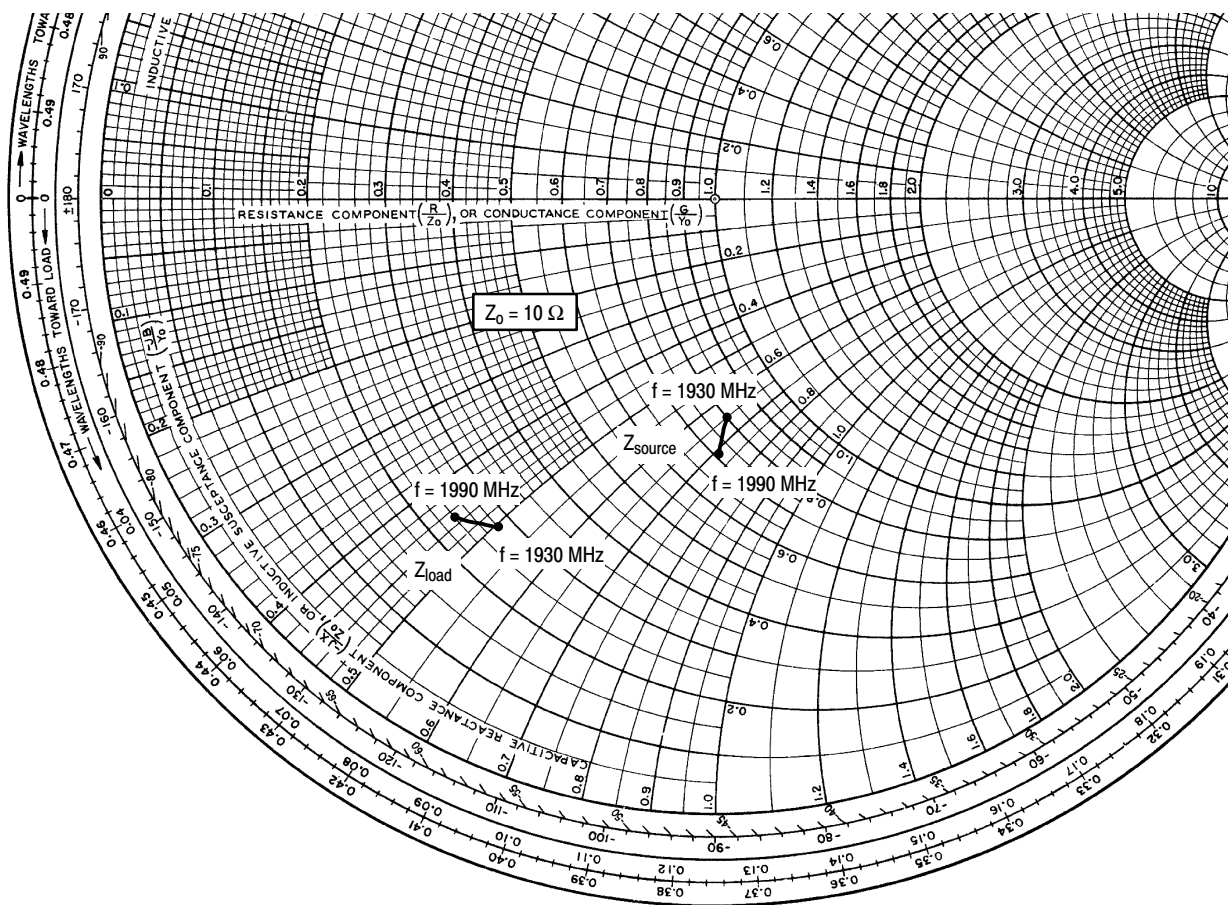


Figure 14. EDGE Spectrum



$V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 600 \text{ mA}$, $P_{out} = 60 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	8.00 - j6.48	2.83 - j5.13
1960	7.57 - j6.82	2.63 - j4.84
1990	7.06 - j7.06	2.44 - j4.54

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

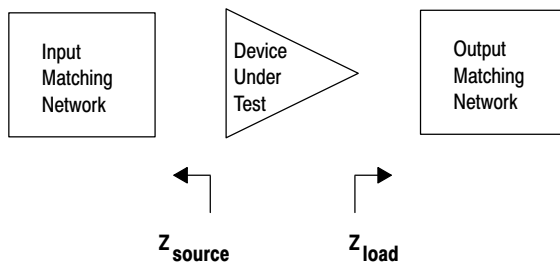


Figure 15. Series Equivalent Source and Load Impedance — 1900 MHz

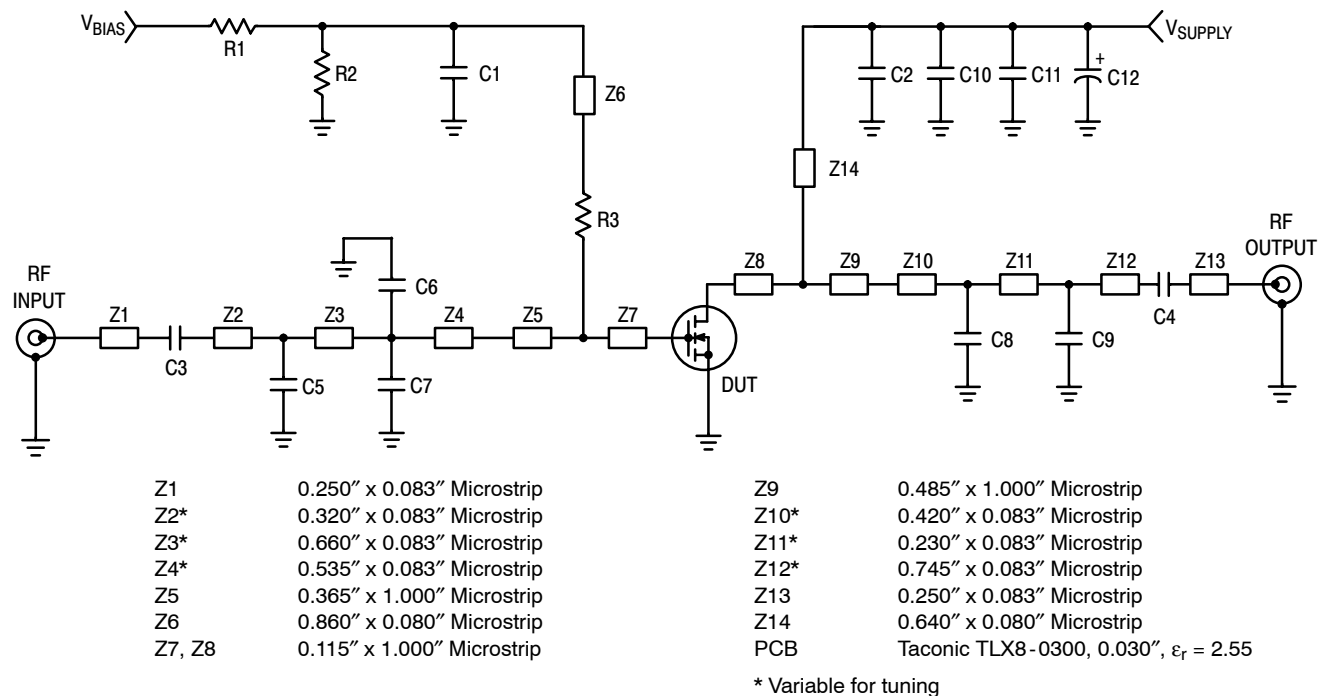


Figure 16. MRF6S18060NR1(NBR1) Test Circuit Schematic — 1800 MHz

Table 7. MRF6S18060NR1(NBR1) Test Circuit Component Designations and Values — 1800 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C5	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C6, C9	0.5 pF Chip Capacitors	ATC100B0R5BT500XT	ATC
C7	2.2 pF Chip Capacitor	ATC100B2R2BT500XT	ATC
C8	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C10, C11	10 μ F Chip Capacitors	C5750X5R1H106MT	TDK
C12	220 μ F, 63 V Electrolytic Capacitor, Radial	2222-136-68221	Vishay
R1, R2	10 k Ω , 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

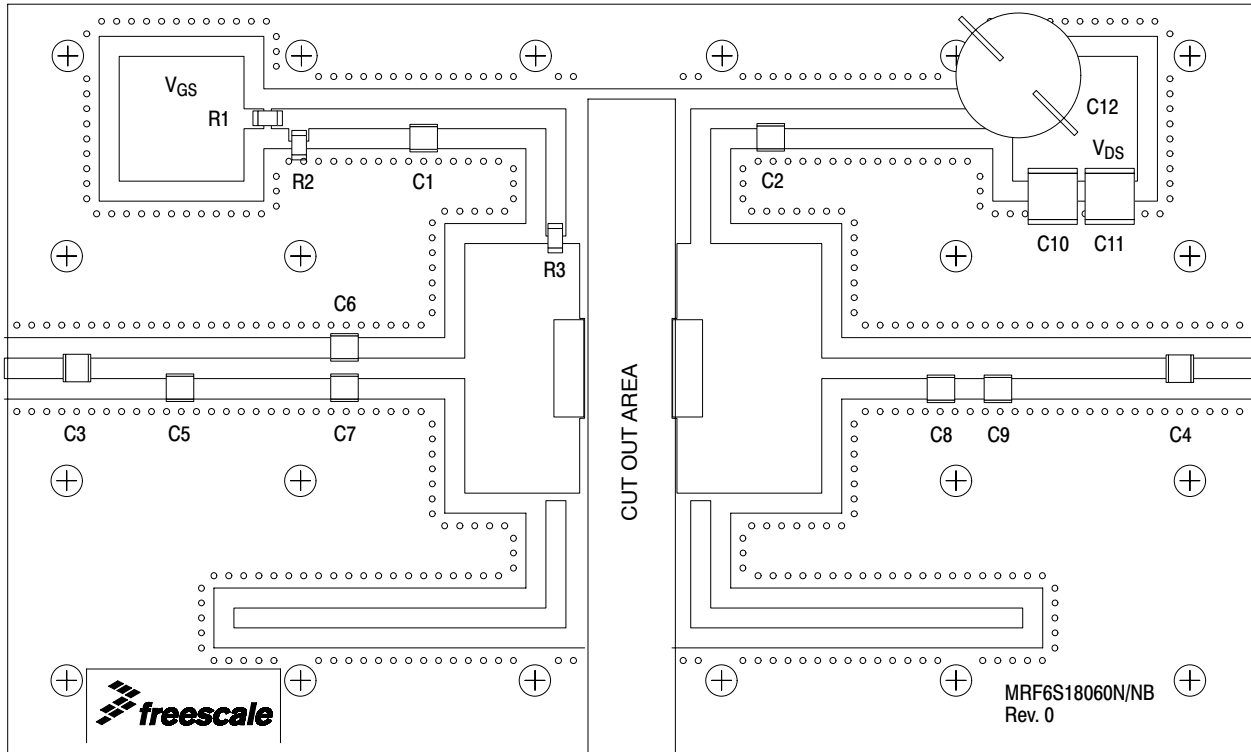


Figure 17. MRF6S18060NR1(NBR1) Test Circuit Component Layout — 1800 MHz

TYPICAL CHARACTERISTICS — 1800 MHz

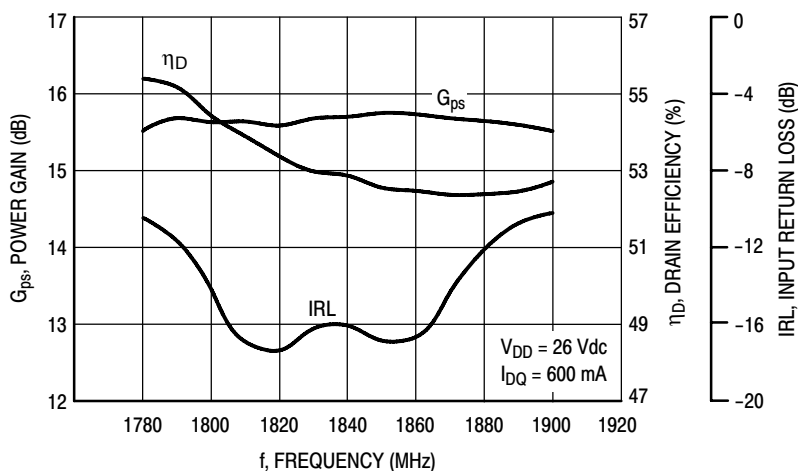


Figure 18. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ $P_{out} = 60$ Watts

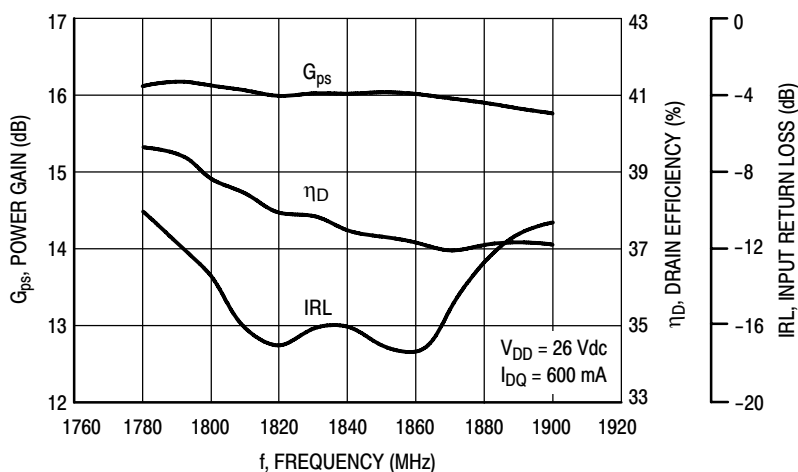


Figure 19. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ $P_{out} = 30$ Watts

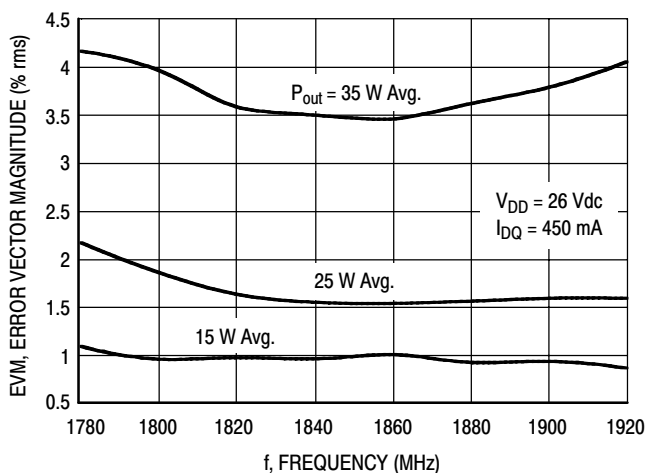


Figure 20. EVM versus Frequency

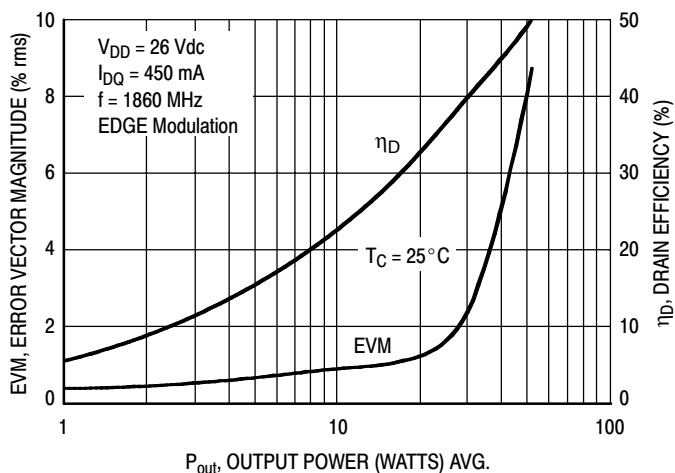


Figure 21. EVM and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS — 1800 MHz

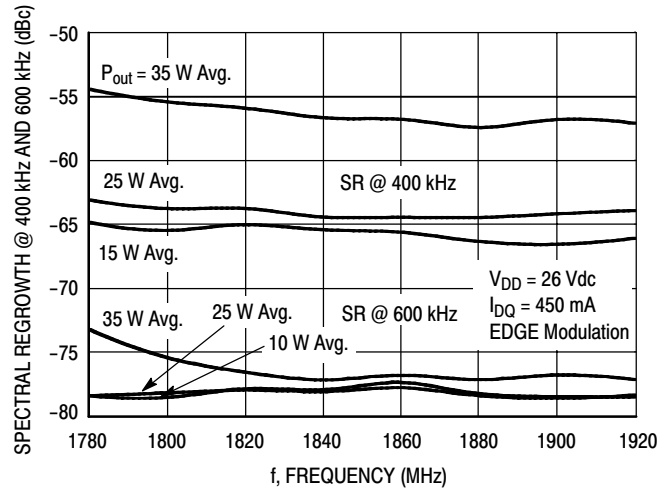


Figure 22. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

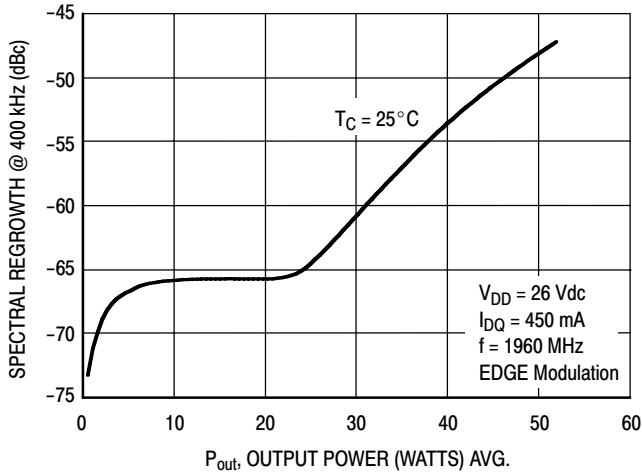


Figure 23. Spectral Regrowth at 400 kHz versus Output Power

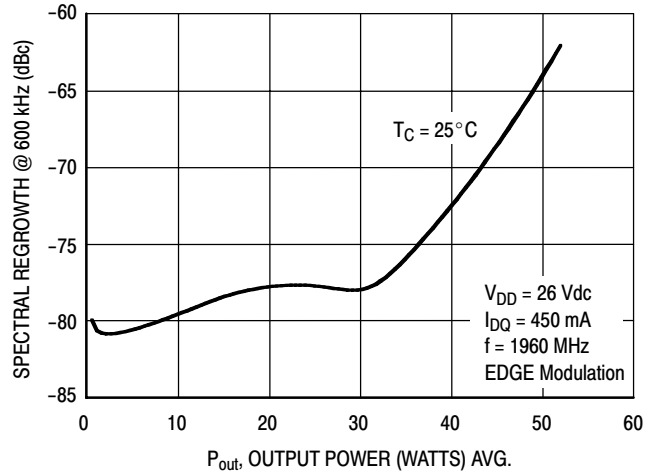
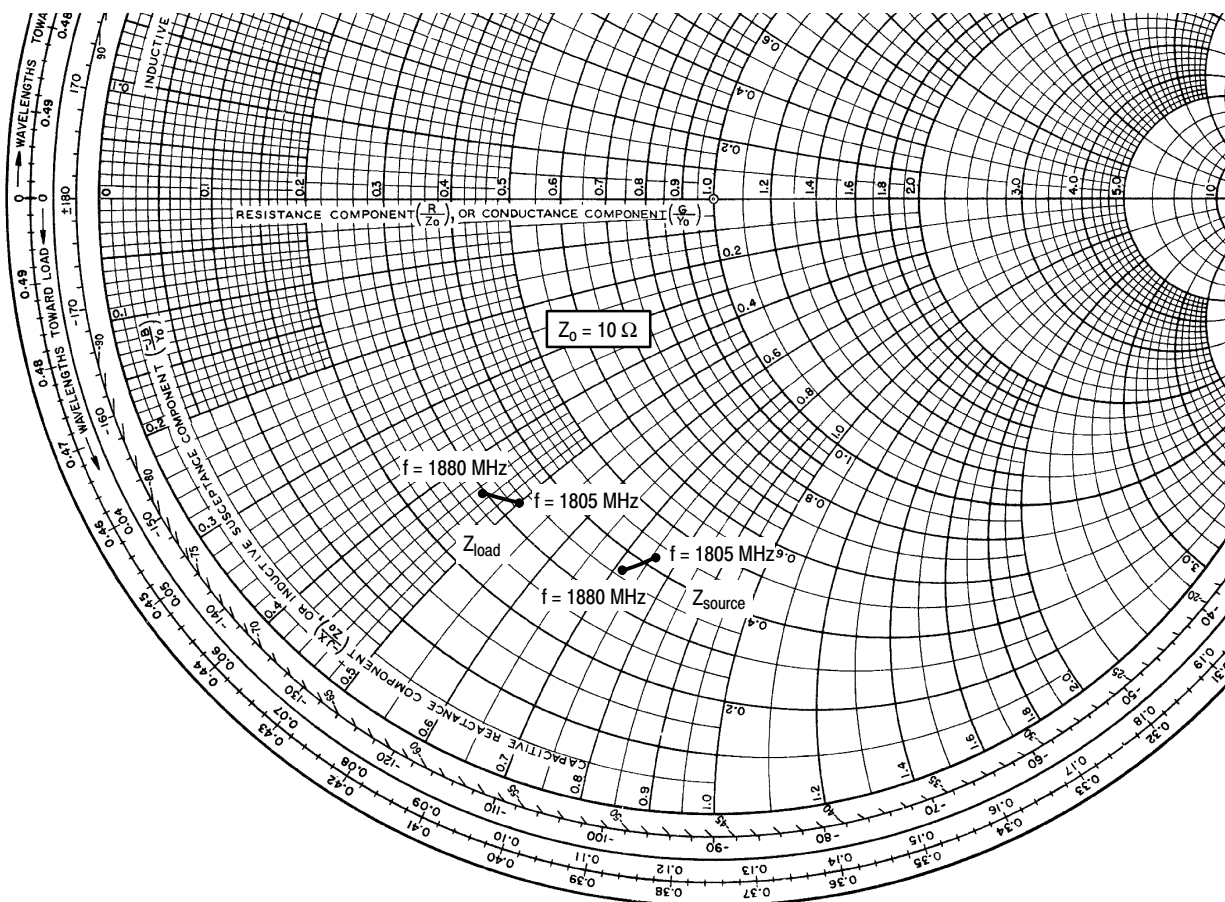


Figure 24. Spectral Regrowth at 600 kHz versus Output Power



$V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 600 \text{ mA}$, $P_{out} = 65 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1805	$4.16 - j7.56$	$3.29 - j4.91$
1840	$3.89 - j7.40$	$3.10 - j4.69$
1880	$3.56 - j7.21$	$2.88 - j4.45$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

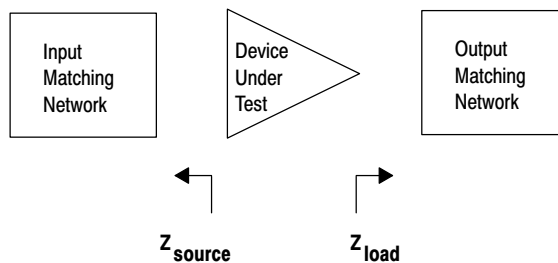
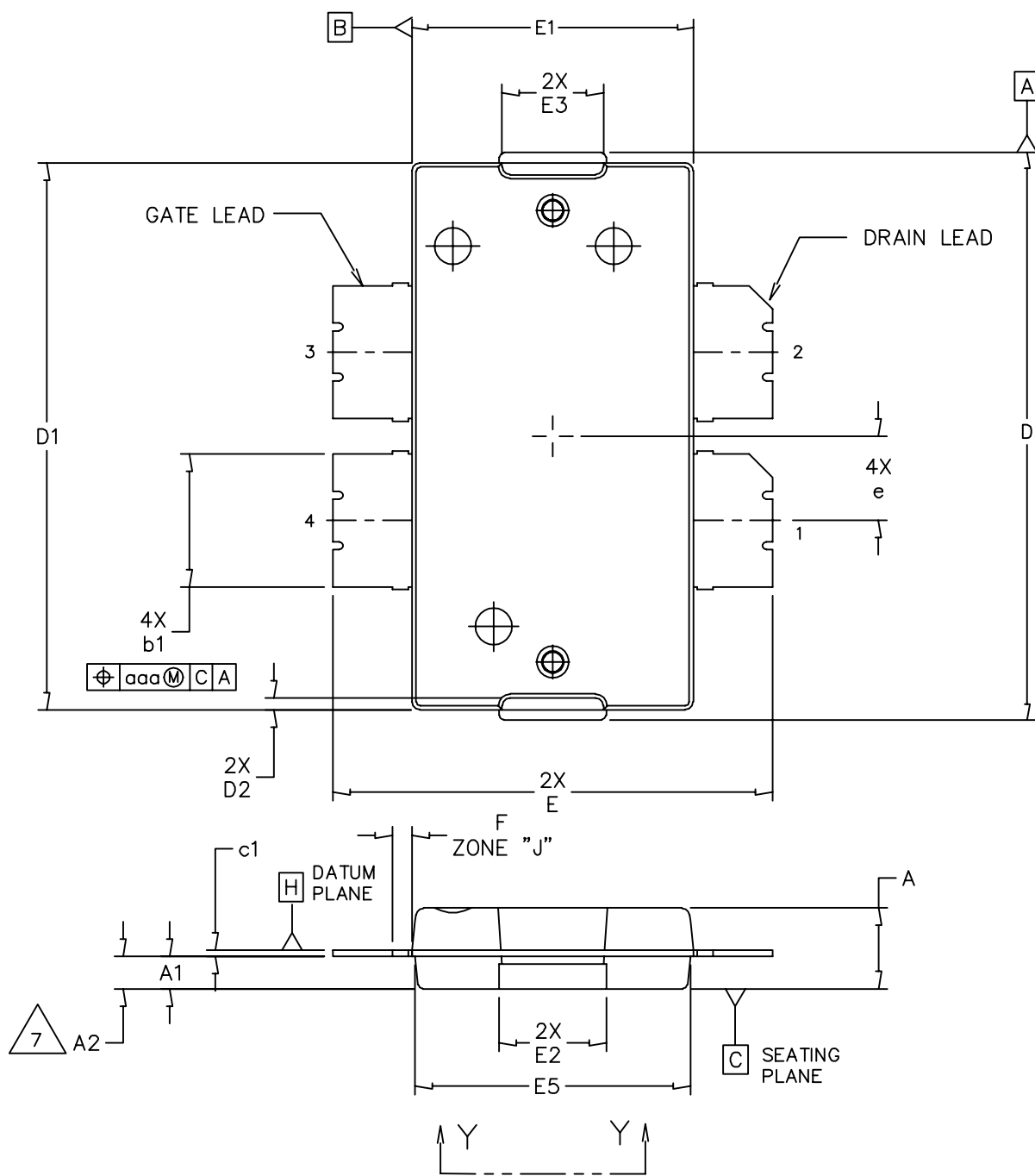
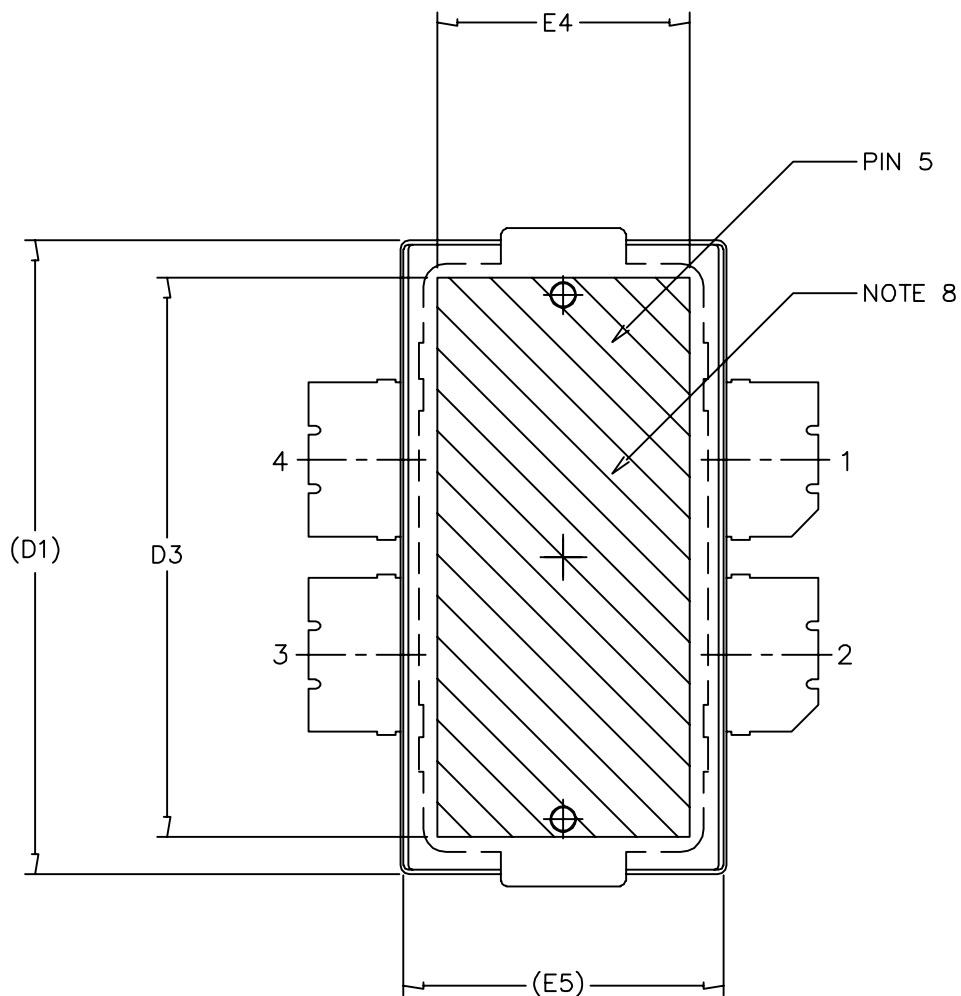


Figure 25. Series Equivalent Source and Load Impedance — 1800 MHz

PACKAGE DIMENSIONS



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TITLE: TO-270 4 LEAD, WIDE BODY		DOCUMENT NO: 98ASA10577D		REV: D	
		CASE NUMBER: 1486-03		13 AUG 2007	
		STANDARD: NON-JEDEC			



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		CASE NUMBER: 1486-03	13 AUG 2007
		STANDARD: NON-JEDEC	

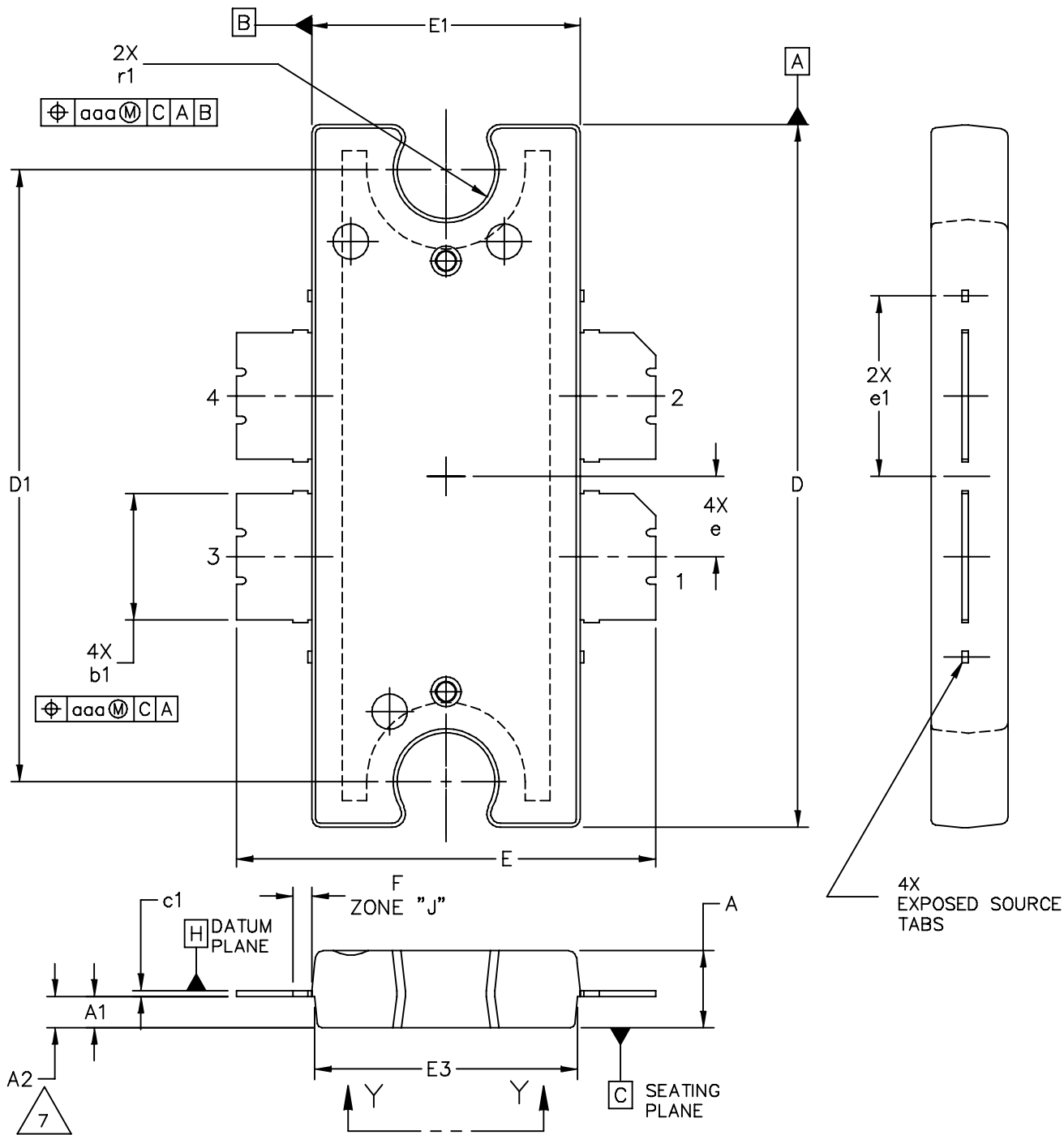
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

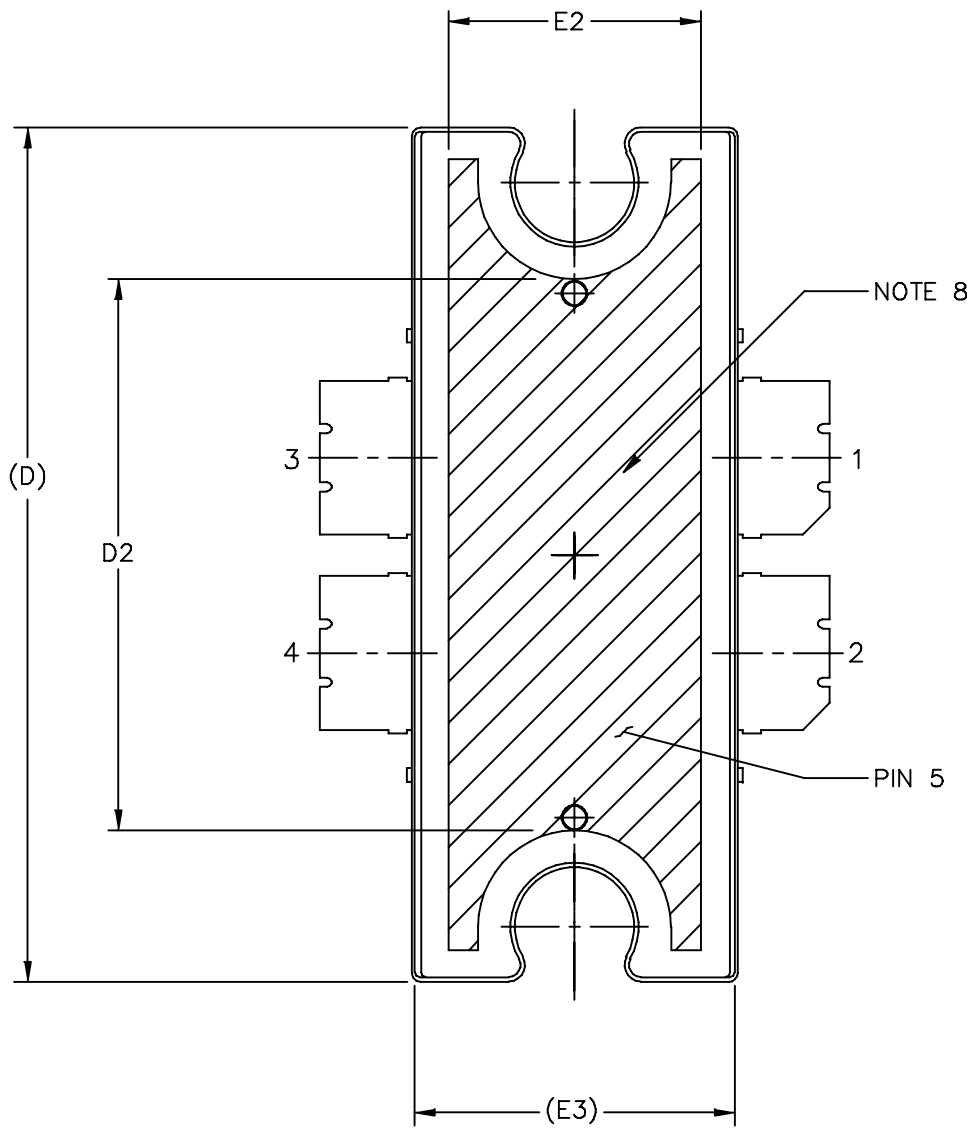
STYLE 1:

PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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					CASE NUMBER: 1486-03			13 AUG 2007	
					STANDARD: NON-JEDEC				



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		CASE NUMBER: 1484-04		31 AUG 2007	
		STANDARD: NON-JEDEC			



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TITLE: TO-272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E	
	CASE NUMBER: 1484-04	31 AUG 2007	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:

PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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			CASE NUMBER: 1484-04		31 AUG 2007
			STANDARD: NON-JEDEC		

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
4	Dec. 2008	<ul style="list-style-type: none"> • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2 • Removed Total Device Dissipation from Max Ratings table as data was redundant (information already provided in Thermal Characteristics table), p. 1 • Changed Storage Temperature Range in Max Ratings table from -65 to +175 to -65 to +150 for standardization across products, p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table, related “Continuous use at maximum temperature will affect MTTF” footnote added and changed 200°C to 225°C in Capable Plastic Package bullet, p. 1 • Corrected V_{DS} to V_{DD} in the RF test condition voltage callout for $V_{GS(Q)}$, and added “Measured in Functional Test”, On Characteristics table, p. 2 • Removed Forward Transconductance from On Characteristics table as it no longer provided usable information, p. 2 • Updated Part Numbers in Tables 6, 7, Component Designations and Values, to latest RoHS compliant part numbers, p. 3, 9 • Removed lower voltage tests from Fig. 6, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 5 • Replaced Fig. 13, MTTF versus Junction Temperature with updated graph. Removed Amps² and listed operating characteristics and location of MTTF calculator for device, p. 7 • Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 14-16. Added pin numbers 1 through 4 on Sheet 1. • Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 17-19. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations. • Added Product Documentation and Revision History, p. 20

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