8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND ....-0.3V to +6V
DV_{DD} to DGND..-0.3V to +6V
AGND to DGND..-0.3V to +0.3V
CH0–CH7, I.C. to AGND (MAX1316/MAX1317/MAX1318)...±6.0V
CH0–CH7, I.C. to AGND (MAX1320/MAX1321/MAX1322).±16.5V
CH0–CH7, I.C. to AGND (MAX1324/MAX1325/MAX1326).±16.5V
INTCLK/$\overline{EXTCLK}$ to AGND.......................-0.3V to (AV_{DD} + 0.3V)
$\overline{EOC}$, $\overline{EOLC}$, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ to DGND.........-0.3V to (DV_{DD} + 0.3V)
CONVST, CLK, SHDN,
ALLON to DGND..................................-0.3V to (DV_{DD} + 0.3V)
MSV, REF_{MS}, REF to AGND.....................-0.3V to (AV_{DD} + 0.3V)
REF+, COM, REF- to AGND.....................-0.3V to (AV_{DD} + 0.3V)
D0–D13 to DGND ....-0.3V to (DV_{DD} + 0.3V)
Maximum Current into Any Pin Except AV_{DD}, DV_{DD},
AGND, DGND..±50mA
Continuous Power Dissipation
LQFP (derate 22.7mW/°C above +70°C)...................1818mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF II 0.1µF, C_{COM} = 2.2µF II 0.1µF, C_{MSV} = 2.2µF II 0.1µF (unipolar devices, MAX1316/MAX1317/MAX1318), MSV = AGND (bipolar devices, MAX1320/MAX1321/MAX1322/MAX1324/MAX1325/MAX1326), f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		14			Bits
Integral Nonlinearity	INL	(Note 2)		±0.8	±2.0	LSB
Differential Nonlinearity	DNL	No missing codes (Note 2)		±0.5	±1	LSB
Offset Error		Unipolar devices			±40	LSB
		Bipolar devices			±40	
Offset Drift		Unipolar devices		-4		ppm/°C
		Bipolar devices		-4		
Channel Offset Matching		Unipolar devices between all channels		35	80	LSB
		Bipolar devices between all channels		25	60	
Gain Error		(Note 3)		±8	±40	LSB
Channel Gain-Error Matching		Between all channels			25	LSB
Gain Temperature Coefficient				3		ppm/°C
DYNAMIC PERFORMANCE (at f_{IN} = 100kHz, -0.4dB FS)						
Signal-to-Noise Ratio	SNR	Unipolar	74.5	76		dB
		Bipolar	75	76.5		
Signal-to-Noise and Distortion Ratio	SINAD	Unipolar	74.5	76		dB
		Bipolar	75	76.5		
Spurious-Free Dynamic Range	SFDR		83	93		dBc
Total Harmonic Distortion	THD			-90	-83	dBc
Channel-to-Channel Isolation			83			dB
ANALOG INPUTS (CH0–CH7)						
Input Voltage Range		MAX1316/MAX1317/MAX1318	0		+5	V
		MAX1320/MAX1321/MAX1322	-5		+5	
		MAX1324/MAX1325/MAX1326	-10		+10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF II 0.1µF, C_{COM} = 2.2µF II 0.1µF, C_{MSV} = 2.2µF II 0.1µF (unipolar devices, MAX1316/MAX1317/MAX1318), MSV = AGND (bipolar devices, MAX1320/MAX1321/MAX1322/MAX1324/MAX1325/MAX1326), f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current (Note 4)		MAX1316/MAX1317/MAX1318	V_{IN} = +5V		0.54	0.72	mA
			V_{IN} = 0V	-0.157	-0.12		
		MAX1320/MAX1321/MAX1322	V_{IN} = +5V		0.29	0.39	
			V_{IN} = -5V	-1.16	-0.87		
		MAX1324/MAX1325/MAX1326	V_{IN} = +10V		0.56	0.74	
			V_{IN} = -10V	-1.13	-0.85		
Input Resistance (Note 4)		MAX1316/MAX1317/MAX1318			7.58		kΩ
		MAX1320/MAX1321/MAX1322			8.66		
		MAX1324/MAX1325/MAX1326			14.26		
Input Capacitance					15		pF
TRACK/HOLD							
External-Clock Throughput Rate (Note 5)		One channel			526		ksps
		Two channels			455		
		Four channels			357		
		Eight channels			250		
Internal-Clock Throughput Rate (Note 5)		One channel (INTCLK/$\overline{EXTCLK}$ = AV_{DD})			526		ksps
		Two channels (INTCLK/$\overline{EXTCLK}$ = AV_{DD})			455		
		Four channels (INTCLK/$\overline{EXTCLK}$ = AV_{DD})			357		
		Eight channels (INTCLK/$\overline{EXTCLK}$ = AV_{DD})			250		
Small-Signal Bandwidth					10		MHz
Full-Power Bandwidth					10		MHz
Aperture Delay					16		ns
Aperture Jitter					50		ps_{RMS}
Aperture-Delay Matching					100		ps
INTERNAL REFERENCE							
REF_{MS} Voltage	V_{REFMS}			2.475	2.500	2.525	V
REF Voltage	V_{REF}			2.475	2.500	2.525	V
REF Temperature Coefficient					30		ppm/°C
EXTERNAL REFERENCE (REF_{MS} AND REF EXTERNALLY DRIVEN)							
Input Current				-250		+250	µA
REF_{MS} Input Voltage Range	V_{REFMS}	Unipolar devices		2.0	2.5	3.0	V
REF Voltage Input Range	V_{REF}			2.0	2.5	3.0	V
REF Input Capacitance					15		pF
REF_{MS} Input Capacitance					15		pF
DIGITAL INPUTS (D0–D7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK, SHDN, ALLON, CONVST)							
Input-Voltage High	V_{IH}			0.7 x DV_{DD}			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ‖ 0.1µF, C_{COM} = 2.2µF ‖ 0.1µF, C_{MSV} = 2.2µF ‖ 0.1µF (unipolar devices, MAX1316/MAX1317/MAX1318), MSV = AGND (bipolar devices, MAX1320/MAX1321/MAX1322/MAX1324/MAX1325/MAX1326), f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage Low	V_{IL}				0.3 x DV_{DD}	V
Input Hysteresis				15		mV
Input Capacitance	C_{IN}			15		pF
Input Current	I_{IN}	V_{IN} = 0V or DV_{DD}			±1	µA
CLOCK-SELECT INPUT (INTCLK/$\overline{EXTCLK}$)						
Input-Voltage High			0.7 x AV_{DD}			V
Input-Voltage Low					0.3 x AV_{DD}	V
DIGITAL OUTPUTS (D0–D13, $\overline{EOC}$, $\overline{EOLC}$)						
Output-Voltage High	V_{OH}	I_{SOURCE} = 0.8mA	DV_{DD} - 0.6			V
Output-Voltage Low	V_{OL}	I_{SINK} = 1.6mA			0.4	V
Tri-State Leakage Current		$\overline{RD}$ ≥ V_{IH} or $\overline{CS}$ ≥ V_{IH}		0.06	1	µA
Tri-State Output Capacitance		$\overline{RD}$ ≥ V_{IH} or $\overline{CS}$ ≥ V_{IH}		15		pF
POWER SUPPLIES						
Analog-Supply Voltage	AV_{DD}		4.75		5.25	V
Digital-Supply Voltage	DV_{DD}		2.70		5.25	V
Analog-Supply Current	I_{AVDD}	All channels selected		46	56	mA
Digital-Supply Current	I_{DVDD}	C_{LOAD} = 100pF, all channels selected (Note 6)		1	1.6	mA
Shutdown Current (Note 7)	I_{AVDD}	V_{SHDN} = DV_{DD}, V_{CH} = float			10	µA
	I_{DVDD}	$V_{\overline{RD}}$ = $V_{\overline{WR}}$ = DV_{DD}, V_{SHDN} = DV_{DD}		0.1	2	
Power-Supply Rejection Ratio	PSRR	AV_{DD} = +4.75V to +5.75V (Note 8)		50		dB

TIMING CHARACTERISTICS (Figures 3, 4, 5, 6 and 7) (Tables 1, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time-to-First-Conversion Result	t_{CONV}	Internal clock		1.6	1.8	µs
		External clock, Figure 6		16		Clock cycles
Time-to-Next-Conversion Result	t_{NEXT}	Internal clock		0.3	0.36	µs
		External clock, Figure 6		3		Clock cycles
CONVST Pulse-Width Low (Acquisition Time)	t_{ACQ}	(Note 9)	0.16		100	µs
$\overline{CS}$ Pulse Width	t_2		30			ns
$\overline{RD}$ Pulse-Width Low	t_3		30			ns
$\overline{RD}$ Pulse-Width High	t_4		30			ns
$\overline{WR}$ Pulse-Width Low	t_5		30			ns
$\overline{CS}$ to $\overline{WR}$	t_6			(Note 10)		ns
$\overline{WR}$ to $\overline{CS}$	t_7			(Note 10)		ns
$\overline{CS}$ to $\overline{RD}$	t_8			(Note 10)		ns
$\overline{RD}$ to $\overline{CS}$	t_9			(Note 10)		ns
Data-Access Time ($\overline{RD}$ Low to Valid Data)	t_{10}				30	ns
Bus-Relinquish Time ($\overline{RD}$ High)	t_{11}				30	ns
$\overline{EOC}$ Pulse Width	t_{12}	Internal clock	80			ns
		External clock, Figure 6		1		Clock cycles
Input-Data Setup Time	t_{14}		10			ns
Input-Data Hold Time	t_{15}		10			ns
External-Clock Period	t_{16}		0.08		10.00	µs
External-Clock High Period	t_{17}	Logic sensitive to rising edges	20			ns
External-Clock Low Period	t_{18}	Logic sensitive to rising edges	20			ns
External-Clock Frequency		(Note 11)	0.1		12.5	MHz
Internal-Clock Frequency				10		MHz
CONVST High to CLK Edge	t_{19}		20	(Note 12)		ns
$\overline{EOC}$ Low to $\overline{RD}$	t_{20}			0		ns

Note 1: For the MAX1316/MAX1317/MAX1318, V_{IN} = 0 to +5V. For the MAX1320/MAX1321/MAX1322, V_{IN} = -5V to +5V. For the MAX1324/MAX1325/MAX1326, V_{IN} = -10V to +10V.

Note 2: All channel performance is guaranteed by correlation to a single channel test.

Note 3: Offset nulled.

Note 4: The analog input resistance is terminated to an internal bias point. Calculate the analog input current using:

$$I_{CH\_} = \frac{V_{CH\_} - V_{BIAS}}{R_{CH\_}}$$

for V_{CH} within the input voltage range.

Note 5: Throughput rate is given per channel. Throughput rate is a function of clock frequency (f_{CLK} = 10MHz). See the *Data Throughput* section for more information.

Note 6: All analog inputs are driven with an FS 100kHz sine wave.

TIMING CHARACTERISTICS (Figures 3, 4, 5, 6 and 7) (Tables 1, 3) (continued)

Note 7: Shutdown current is measured with analog input floating. The large amplitude of the maximum shutdown current specification is due to automatic test equipment limitations.

Note 8: Defined as the change in positive full scale caused by ±5% variation in the nominal supply voltage.

Note 9: CONVST must remain low for at least the acquisition period. The maximum acquisition time is limited by internal capacitor droop.

Note 10: $\overline{CS}$-to-$\overline{WR}$ and $\overline{CS}$-to-$\overline{RD}$ pins are internally AND together. Setup and hold times do not apply.

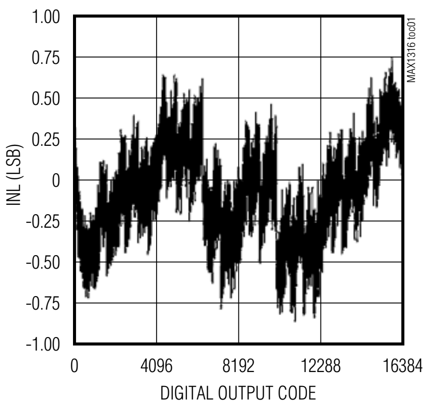
Note 11: Minimum clock frequency is limited only by the internal T/H droop rate. Limit the time between the falling edge of CONVST to the falling edge of EOLC to a maximum of 0.25ms.

Note 12: To avoid T/H droop degrading the sampled analog input signals, the first clock pulse should occur within 10µs of the rising edge of CONVST, and have a minimum clock frequency of 100kHz.

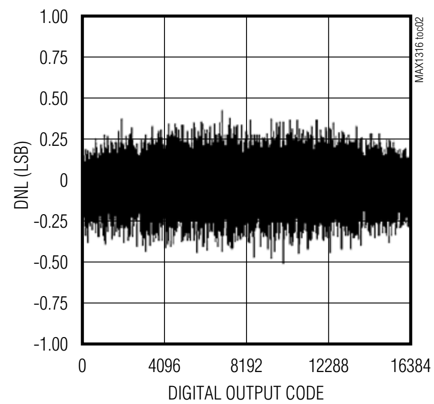
Typical Operating Characteristics

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits* section, f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = +25°C, unless otherwise noted.)

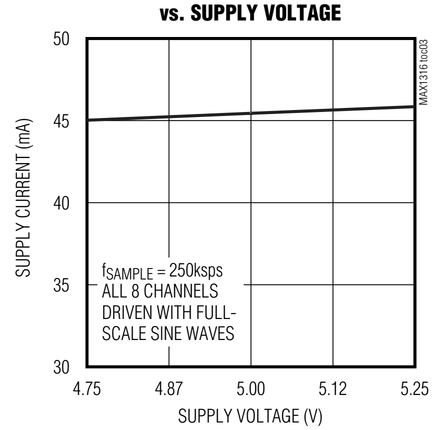
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



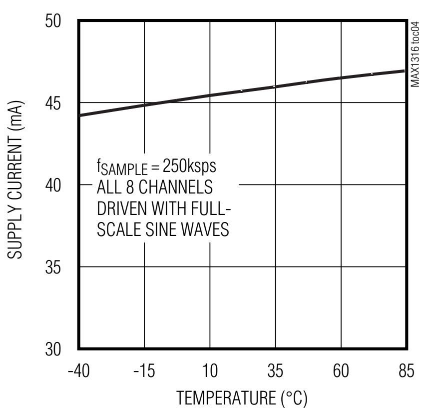
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



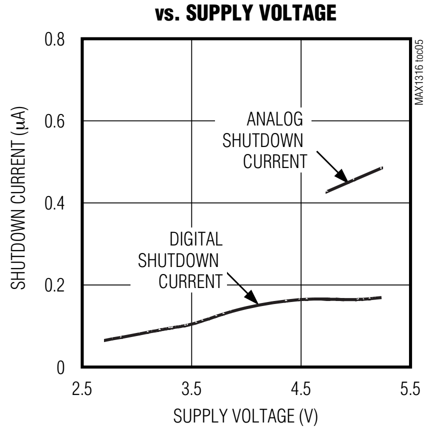
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



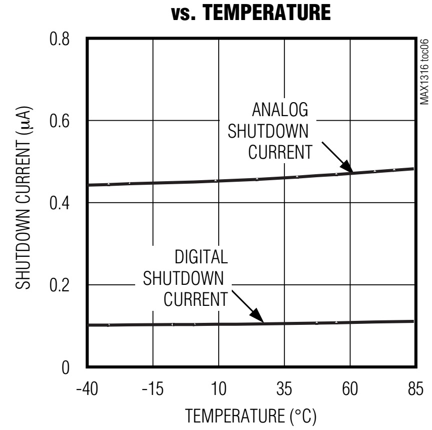
ANALOG SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



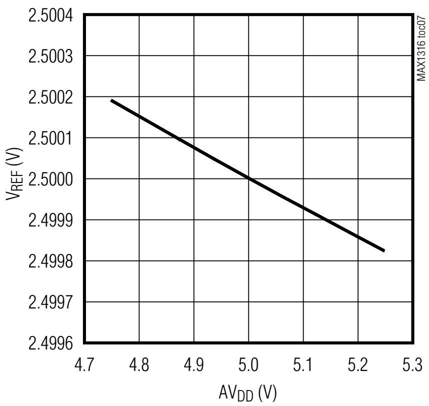
SHUTDOWN CURRENT vs. TEMPERATURE



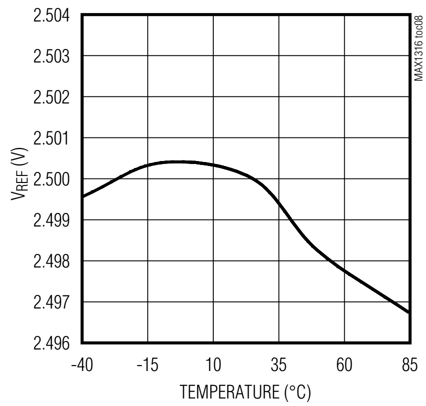
Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits* section, f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = +25°C, unless otherwise noted.)

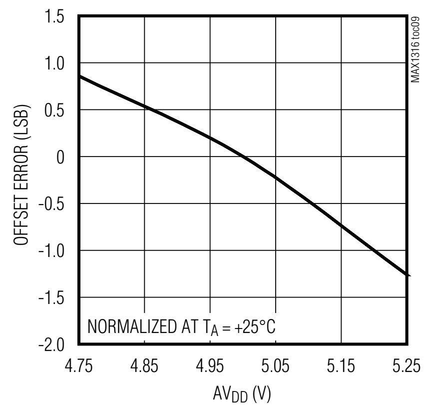
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



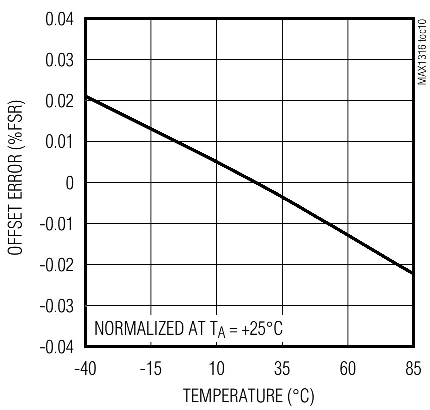
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



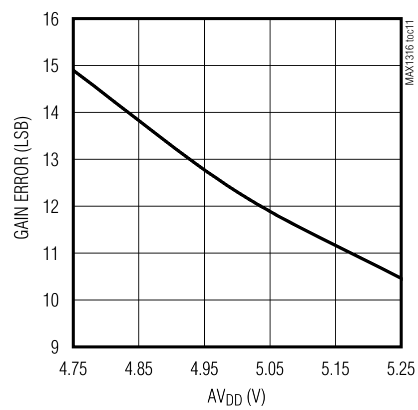
OFFSET ERROR vs. SUPPLY VOLTAGE



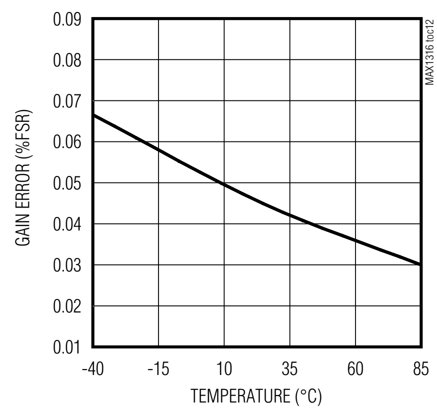
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE

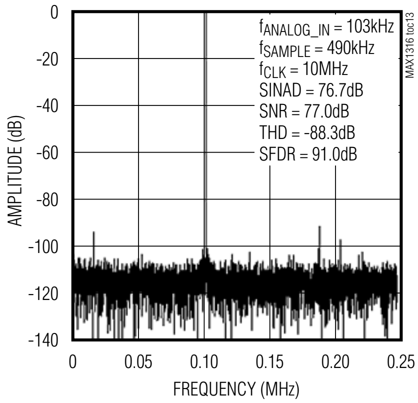


8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

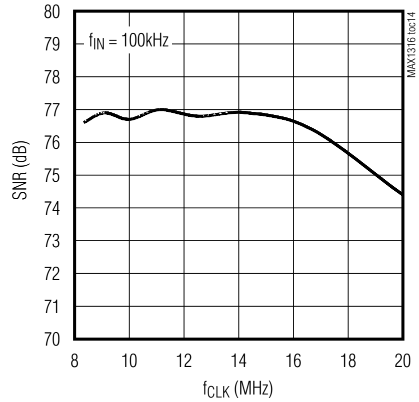
Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits* section, f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{\text{EXTCLK}}$ = AGND (external clock), SHDN = DGND, T_A = +25°C, unless otherwise noted.)

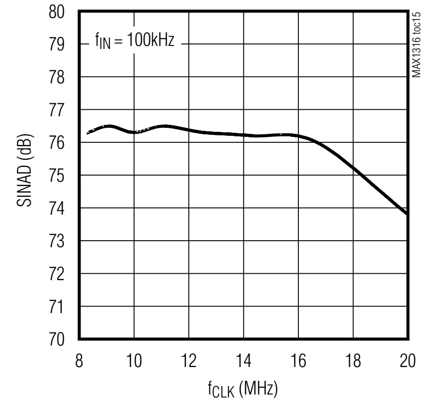
FFT



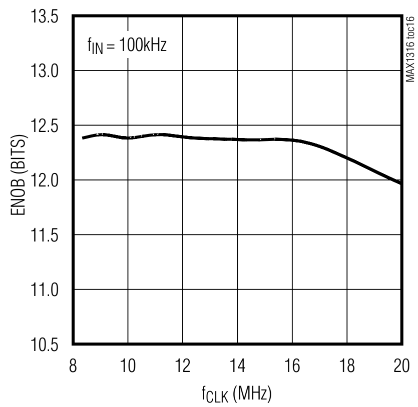
SIGNAL-TO-NOISE RATIO vs. CLOCK FREQUENCY



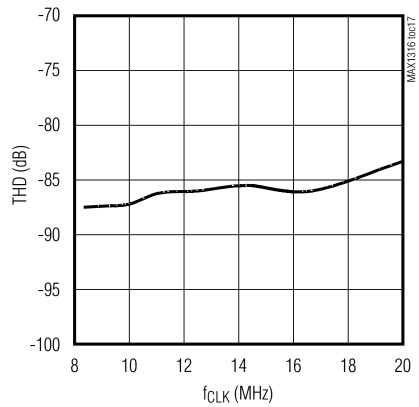
SIGNAL-TO-NOISE PLUS DISTORTION vs. CLOCK FREQUENCY



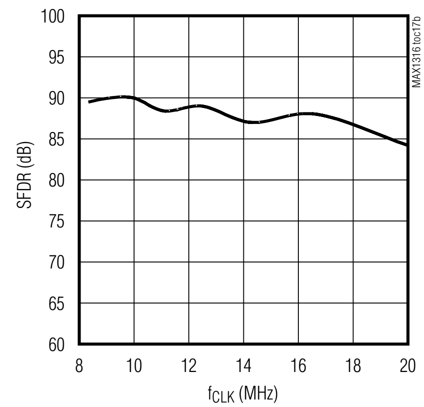
EFFECTIVE NUMBER OF BITS vs. CLOCK FREQUENCY



TOTAL HARMONIC DISTORTION vs. CLOCK FREQUENCY

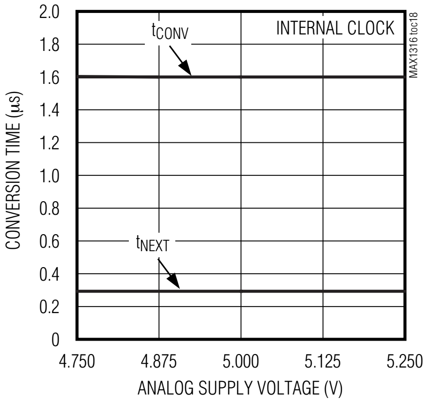


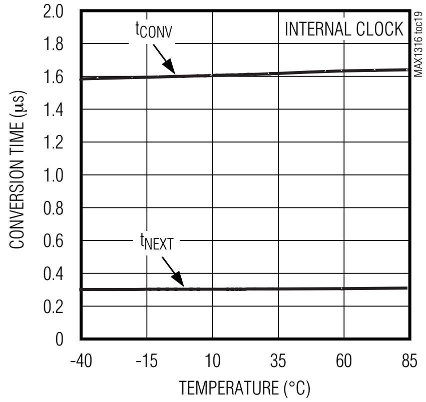
SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK FREQUENCY

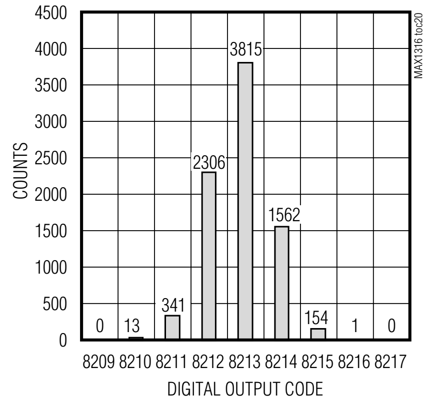


Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits* section, f_{CLK} = 10MHz, 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = +25°C, unless otherwise noted.)







Pin Description

PIN			NAME	FUNCTION
MAX1316 MAX1320 MAX1324	MAX1317 MAX1321 MAX1325	MAX1318 MAX1322 MAX1326		
1, 15, 17	1, 15, 17	1, 15, 17	AV_{DD}	Analog Supply Input. AV_{DD} is the power input for the analog section of the converter. Apply 4.75V to 5.25V to AV_{DD}. Bypass AV_{DD} to AGND (pin 14 to pin 15, pin 16 to pin 17, pin 1 to pin 2) with a 0.1µF capacitor at each AV_{DD} input.
2, 3, 14, 16, 23	2, 3, 14, 16, 23	2, 3, 14, 16, 23	AGND	Analog Ground. AGND is the power return for AV_{DD}. Connect all AGNDs together.
4	4	4	CH0	Channel 0 Analog Input
5	5	5	CH1	Channel 1 Analog Input
6	6	6	MSV	Midscale Voltage Bypass. For the MAX1316/MAX1317/MAX1318, connect a 2.2µF and a 0.1µF capacitor from MSV to AGND. For the MAX1320/MAX1321/MAX1322/MAX1324/MAX1325/MAX1326, connect MSV directly to AGND.
7	7	—	CH2	Channel 2 Analog Input
8	8	—	CH3	Channel 3 Analog Input
9	—	—	CH4	Channel 4 Analog Input

8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1316 MAX1320 MAX1324	MAX1317 MAX1321 MAX1325	MAX1318 MAX1322 MAX1326		
10	—	—	CH5	Channel 5 Analog Input
11	—	—	CH6	Channel 6 Analog Input
12	—	—	CH7	Channel 7 Analog Input
13	13	13	INTCLK/$\overline{\text{EXTCLK}}$	Clock-Mode Select Input. Use INTCLK/$\overline{\text{EXTCLK}}$ to select the internal or external conversion clock. Connect INTCLK/$\overline{\text{EXTCLK}}$ to AV_{DD} to select the internal clock. Connect INTCLK/$\overline{\text{EXTCLK}}$ to AGND to use an external clock connected to CLK.
18	18	18	REF_{MS}	Midscale Reference Bypass or Input. REF_{MS} is the bypass point for an internally generated reference voltage. For the MAX1316/MAX1317/MAX1318, connect a 0.1µF capacitor from REF_{MS} to AGND. For the MAX1320/MAX1321/MAX1322/MAX1324/MAX1325/MAX1326, connect REF_{MS} directly to REF and bypass with a 0.1µF capacitor from REF_{MS} to AGND.
19	19	19	REF	ADC Reference Bypass or Input. REF is the bypass point for an internally generated reference voltage. Bypass REF with a 0.01µF capacitor to AGND. REF can be driven externally by a precision external voltage reference.
20	20	20	REF+	Positive Reference Bypass. REF+ is the bypass point for an internally generated reference voltage. Bypass REF+ with a 0.1µF capacitor to AGND. Also bypass REF+ to REF- with a 2.2µF and a 0.1µF capacitor.
21	21	21	COM	Reference Common Bypass. COM is the bypass point for an internally generated reference voltage. Bypass COM to AGND with a 2.2µF and a 0.1µF capacitor.
22	22	22	REF-	Negative Reference Bypass. REF- is the bypass point for an internally generated reference voltage. Bypass REF- with a 0.1µF capacitor to AGND. Also bypass REF- to REF+ with a 2.2µF and a 0.1µF capacitor.
24	24	24	D0	Digital I/O Bit 0 of 14-Bit Parallel Data Bus. High impedance when $\overline{\text{RD}}$ = 1 or $\overline{\text{CS}}$ = 1.
25	25	25	D1	Digital I/O Bit 1 of 14-Bit Parallel Data Bus. High impedance when $\overline{\text{RD}}$ = 1 or $\overline{\text{CS}}$ = 1.
26	26	26	D2	Digital I/O Bit 2 of 14-Bit Parallel Data Bus. High impedance when $\overline{\text{RD}}$ = 1 or $\overline{\text{CS}}$ = 1.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1316 MAX1320 MAX1324	MAX1317 MAX1321 MAX1325	MAX1318 MAX1322 MAX1326		
27	27	27	D3	Digital I/O Bit 3 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
28	28	28	D4	Digital I/O Bit 4 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
29	29	29	D5	Digital I/O Bit 5 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
30	30	30	D6	Digital I/O Bit 6 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
31	31	31	D7	Digital I/O Bit 7 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
32	32	32	D8	Digital Out Bit 8 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
33	33	33	D9	Digital Out Bit 9 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
34	34	34	D10	Digital Out Bit 10 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
35	35	35	D11	Digital Out Bit 11 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
36	36	36	D12	Digital Out Bit 12 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
37	37	37	D13	Digital Out Bit 13 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
38	38	38	DV_{DD}	Digital-Supply Input. Apply +2.7V to +5.25V to DV_{DD}. Bypass DV_{DD} to DGND with a 0.1µF capacitor.
39	39	39	DGND	Digital-Supply GND. DGND is the power return for DV_{DD}. Connect DGND to AGND at only one point (see the *Layout, Grounding, and Bypassing* section).
40	40	40	$\overline{EOC}$	End-of-Conversion Output. $\overline{EOC}$ goes low to indicate the end of a conversion. $\overline{EOC}$ returns high after one clock period.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1316 MAX1320 MAX1324	**MAX1317 MAX1321 MAX1325**	**MAX1318 MAX1322 MAX1326**		
41	41	41	$\overline{\text{EOLC}}$	End-of-Last-Conversion Output. $\overline{\text{EOLC}}$ goes low to indicate the end of the last conversion. $\overline{\text{EOLC}}$ returns high when CONVST goes low for the next conversion sequence.
42	42	42	$\overline{\text{RD}}$	Read Input. When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ go low, the device initiates a read command of the parallel data buses, D0–D13. D0–D13 are high impedance while either $\overline{\text{RD}}$ or $\overline{\text{CS}}$ is high.
43	43	43	$\overline{\text{WR}}$	Write Input. The write command initiates when $\overline{\text{WR}}$ and $\overline{\text{CS}}$ go low. A write command loads the configuration byte on D0–D7.
44	44	44	$\overline{\text{CS}}$	Chip-Select Input. Pulling $\overline{\text{CS}}$ low activates the digital interface. D0–D13 are high impedance while either $\overline{\text{CS}}$ or $\overline{\text{RD}}$ is high.
45	45	45	CONVST	Convert-Start Input. Driving CONVST high places the device in hold mode and initiates the conversion process. The analog inputs are sampled on the rising edge of CONVST. When CONVST is low, the analog inputs are tracked.
46	46	46	CLK	External-Clock Input. CLK accepts an external-clock signal up to 15MHz. Connect CLK to DGND for internally clocked conversions. To select external-clock mode, set INTCLK/$\overline{\text{EXTCLK}}$ = 0.
47	47	47	SHDN	Shutdown Input. Set SHDN = 0 for normal operation. Set SHDN = 1 for shutdown mode.
48	48	48	ALLON	Enable-All-Channels Input. Drive ALLON high to enable all input channels. When ALLON is low, only input channels selected as active are powered. Select channels as active using the configuration register.
—	9–12	7–12	I.C.	Internally Connected. Connect I.C. to AGND. For factory use only.

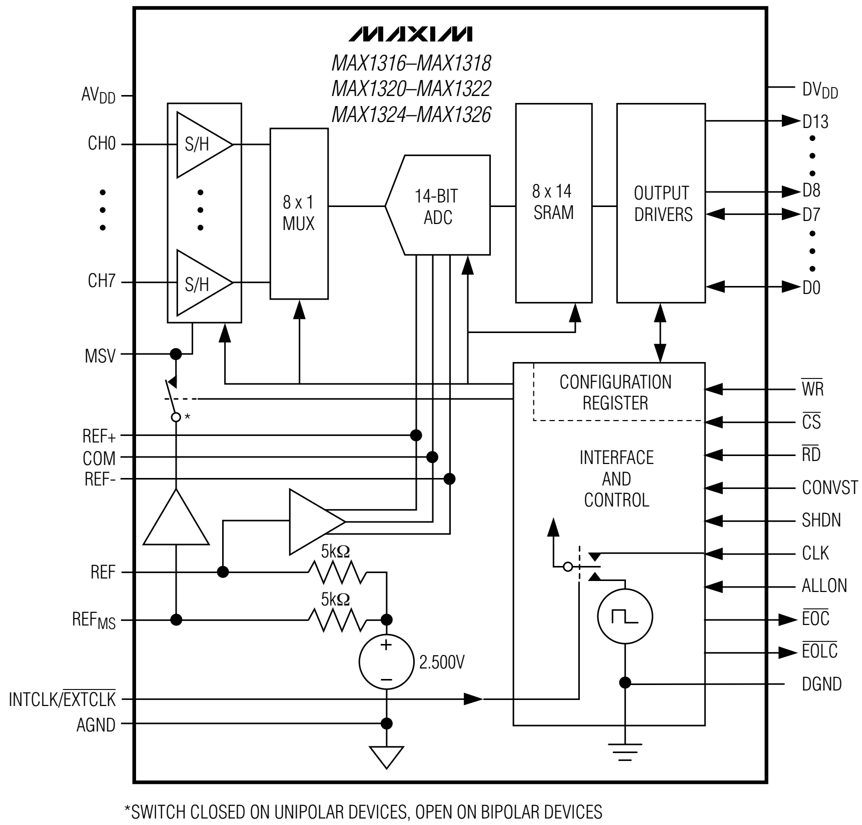


Figure 1. Functional Diagram

Detailed Description

The MAX1316–MAX1318/MAX1320–MAX1322/MAX1324-MAX1326 are 14-bit ADCs. They offer two, four, or eight (independently selectable) input channels, each with its own T/H circuitry. Simultaneous sampling of all active channels preserves relative phase information, making these devices ideal for motor control and power monitoring. These devices are available with 0 to +5V, ±5V, and ±10V input ranges. The 0 to +5V devices feature ±6V fault-tolerant inputs. The ±5V and ±10V devices feature ±16.5V fault-tolerant inputs. Two channels convert in 2µs; all eight channels convert in 3.8µs, with a maximum 8-channel throughput of 263ksps per channel. Internal or external reference and internal- or external-clock capability offer great flexibility and ease of use. A write-only configuration register can mask out unused channels, and a shutdown feature reduces power. A 16.6MHz, 14-bit, parallel data bus outputs the conversion result. Figure 1 shows the functional diagram of these devices.

Analog Inputs

T/H

To preserve phase information across these multichannel devices, each input channel has a dedicated T/H amplifier.

Use a low-input source impedance to minimize gain-error harmonic distortion. The time required for the T/H to acquire an input signal depends on the input source impedance. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_1) is the maximum time the device takes to acquire the signal. Use the following formula to calculate acquisition time:

$$t_1 = 10 (R_S + R_{IN}) \times 6pF$$

where R_{IN} = 2.2kΩ, R_S = the input signal's source impedance, and t_1 is never less than 180ns. A source impedance of less than 100Ω does not significantly affect the ADC's performance.

8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

To improve the input-signal bandwidth under AC conditions, drive the input with a wideband buffer (>50MHz) that can drive the ADC's input capacitance and settle quickly. For example, the MAX4265 can be used for +5V unipolar devices, or the MAX4350 can be used for ±5V bipolar inputs.

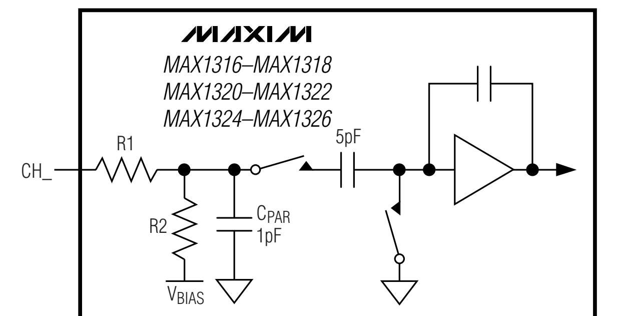
The T/H aperture delay is typically 13ns. The aperture-delay mismatch between T/Hs of 50ps allows the relative phase information of up to eight different inputs to be preserved. Figure 2 shows a simplified equivalent input circuit, illustrating the ADC's sampling architecture.

Input Bandwidth

The input tracking circuitry has a 12MHz small-signal bandwidth, making it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Input Range and Protection

These devices provide ±10V, ±5V, or 0 to +5V analog input voltage ranges. Figure 2 shows the equivalent input circuit. Overvoltage protection circuitry at the analog input provides ±16.5V fault protection for the bipolar input devices and ±6.0V fault protection for the unipolar input devices. This fault-protection circuit limits the current going into or out of the device to less than 50mA, providing an added layer of protection from momentary overvoltage or undervoltage conditions at the analog input.



INPUT RANGE (V)	R1 (kΩ)	R2 (kΩ)	V_{BIAS} (V)
0 TO +5	3.33	5.00	0.90
±5	6.67	2.86	2.50
±10	13.33	2.35	2.06

Figure 2. Typical Input Circuit

Power-Saving Modes

Shutdown Mode

During shutdown, the analog and digital circuits in the device power down and the device draws less than 100µA from AV_{DD}, and less than 100µA from DV_{DD}. Select shutdown mode using the SHDN input. Set SHDN high to enter shutdown mode. After coming out of shutdown, allow a 1ms wake-up time before making the first conversion. When using an external clock, apply at least 20 clock cycles with CONVST high before making the first conversion. When using internal-clock mode, wait at least 2µs before making the first conversion.

ALLON

ALLON is useful when some of the analog input channels are selected (see the *Configuration Register* section). Drive ALLON high to power up all input channel circuits, regardless of whether they are selected as active by the configuration register. Drive ALLON low or connect to ground to power only the input channels selected as active by the configuration register, saving 2mA per channel (typ). The wake-up time for any channel turned on with the configuration register is 2µs (typ) when ALLON is low. The wake-up time with ALLON high is only 0.01µs. New configuration-register information does not become active until the next CONVST falling edge. Therefore, when using software to control power states (ALLON = 0), pulse CONVST low once before applying the actual CONVST signal (Figure 3). With an external clock, apply at least 15 clock cycles before the second CONVST. If using internal-clock mode, wait at least 1.5µs or until the first $\overline{EOC}$ before generating the second CONVST.

Table 1. Conversion Times Using the Internal Clock

NUMBER OF CHANNELS	INTERNAL-CLOCK CONVERSION TIME
1	1.6
2	1.9
3	2.2
4	2.5
5	2.8
6	3.1
7	3.4
8	3.7

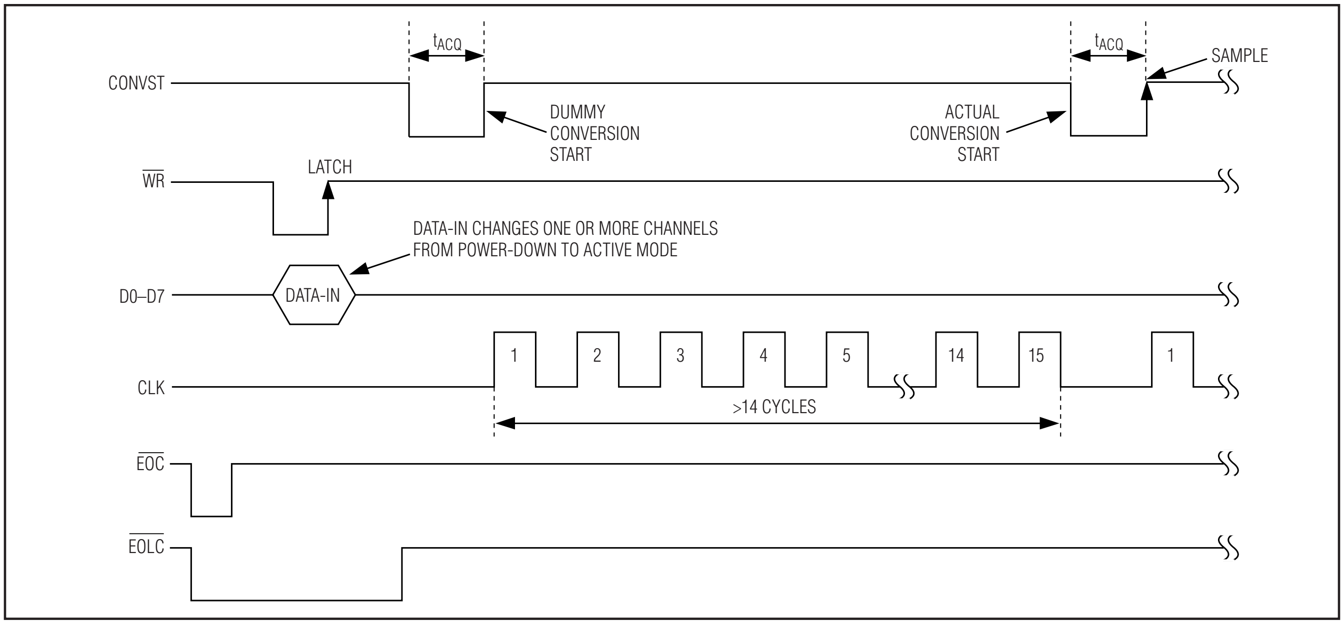


Figure 3. Software Channel Wake-Up Timing (ALLON = 0)

Clock Modes

These devices provide an internal clock of 10MHz (typ). Alternatively, an external clock can be used.

Internal Clock

Internal-clock mode frees the microprocessor from the burden of running the ADC conversion clock. For internal-clock operation, connect INTCLK/$\overline{\text{EXTCLK}}$ to AV_{DD} and connect CLK to DGND. Table 1 illustrates the total conversion time using internal-clock mode.

External Clock

For external-clock operation, connect INTCLK/$\overline{\text{EXTCLK}}$ to AGND and connect an external-clock source to CLK. Note that INTCLK/$\overline{\text{EXTCLK}}$ is referenced to the analog power supply, AV_{DD}. The external-clock frequency can be up to 15MHz, with a duty cycle between 30% and 70%. Clock frequencies of 100kHz and lower can be used, but the droop in the T/H circuits reduce linearity.

Selecting an Input Buffer

Most applications require an input buffer to achieve 14-bit accuracy. Although slew-rate and bandwidth are important, the most critical specification is settling time. The sampling requires a relatively brief sampling interval of 150ns. At the beginning of the acquisition, the internal sampling capacitor array connects to CH_ (the amplifier output), causing some output disturbance. Ensure the amplifier is capable of settling to at least 14-bit accuracy during this interval. Use a low-noise, low-distortion, wideband amplifier (such as the MAX4350 or MAX4265), which settles quickly and is stable with the ADC's capacitive load (in parallel with any bypass capacitors on the analog inputs).

Applications Section

Digital Interface

The bidirectional, parallel, digital interface sets the 8-bit configuration register (see the *Configuration Register* section) and outputs the 14-bit conversion result. The interface includes the following control signals: chip select ($\overline{\text{CS}}$), read ($\overline{\text{RD}}$), write ($\overline{\text{WR}}$), end of conversion ($\overline{\text{EOC}}$), end of last conversion ($\overline{\text{EOLC}}$), convert start (CONVST), shutdown ($\overline{\text{SHDN}}$), all on (ALLON), internal-clock select (INTCLK /$\overline{\text{EXTCLK}}$), and external-clock input (CLK). Figures 4, 5, 6, 7, Table 4, and the *Timing Characteristics* section show the operation of the interface. D0–D7 are bidirectional, and D8–D13 are output only. All bits are high impedance when $\overline{\text{RD}}$ = 1 or $\overline{\text{CS}}$ = 1.

Configuration Register

Enable channels as active by writing to the configuration register through I/O lines D0–D7 (Table 2). The bits in the configuration register map directly to the channels, with D0 controlling channel zero, and D7 controlling channel seven. Setting any bit high activates the corresponding input channel, while resetting any bit low deactivates the corresponding channel. Devices with fewer than eight channels contain some bits that have no function.

Table 2. Configuration Register

PART NO.	STATE	BIT/CHANNEL							
		D0/CH0	D1/CH1	D2/CH2	D3/CH3	D4/CH4	D5/CH5	D6/CH6	D7/CH7
MAX1316 MAX1320 MAX1324	ON	1	1	1	1	1	1	1	1
	OFF	0	0	0	0	0	0	0	0
MAX1317 MAX1321 MAX1325	ON	1	1	1	1	NA	NA	NA	NA
	OFF	0	0	0	0	NA	NA	NA	NA
MAX1318 MAX1322 MAX1326	ON	1	1	NA	NA	NA	NA	NA	NA
	OFF	0	0	NA	NA	NA	NA	NA	NA

NA = Not applicable.

To write to the configuration register, pull $\overline{CS}$ and $\overline{WR}$ low, load bits D0–D7 onto the parallel bus, and force $\overline{WR}$ high. The data are latched on the rising edge of $\overline{WR}$ (Figure 4). It is possible to write to the configuration register at any point during the conversion sequence; however, it is not active until the next convert-start signal. At power-up, write to the configuration register to select the active channels before beginning a conversion. Shutdown does not change the configuration register. See the *Shutdown Mode* and the *ALLON* sections for information about using the configuration register for power saving.

Starting a Conversion

To start a conversion using internal-clock mode, pull CONVST low for at least the acquisition time (t_1). The T/H acquires the signal while CONVST is low, and conversion begins on the rising edge of CONVST. An end-of-conversion signal ($\overline{EOC}$) pulses low when the first result becomes available, and for each subsequent result until the end of the conversion cycle. The end-of-last-conversion signal ($\overline{EOLC}$) goes low when the last conversion result is available (Figures 5, 6, and 7).

To start a conversion using external-clock mode, pull CONVST low for at least the acquisition time (t_1). The T/H acquires the signal while CONVST is low, and conversion begins on the rising edge of CONVST. Apply an external clock to CLK. To avoid T/H droop degrading the sampled analog input signals, the first clock pulse should occur within 10µs from the rising edge of CONVST, and have a minimum clock frequency of 100kHz. The first conversion result is available for read on the rising edge of the 17th clock cycle, and subsequent conversions after every third clock cycle thereafter (Figures 5, 6, and 7).

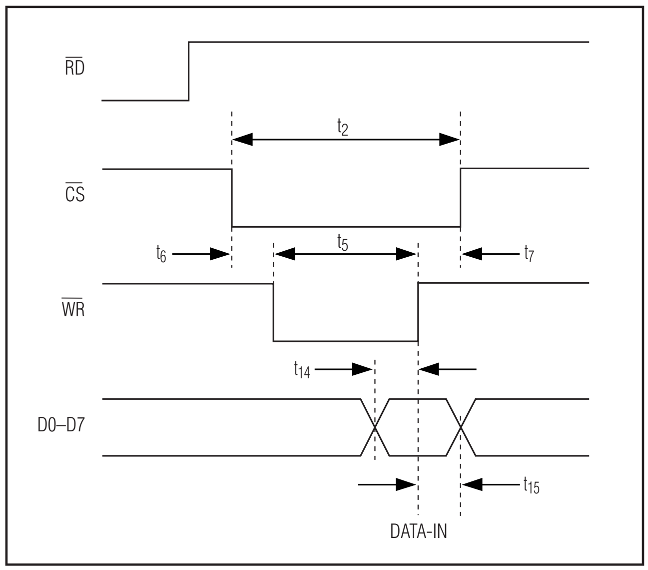


Figure 4. Write Timing

In both internal- and external-clock modes, CONVST must be held high until the last conversion result is read. For best operation, the rising edge of CONVST must be a clean, high-speed, low-jitter digital signal.

Table 3 shows the total throughput as a function of the clock frequency and the number of channels selected for conversion. The calculations use the nominal speed of the internal clock (10MHz) and a 200ns CONVST pulse width.

Data Throughput

The data throughput (f_{TH}) of the MAX1316–MAX1318/MAX1320–MAX1322/MAX1324–MAX1326 is a function of the clock speed (f_{CLK}). In internal-clock mode, f_{CLK} = 10MHz. In external-clock mode, 100kHz ≤ f_{CLK} ≤ 12.5MHz. When reading during conversion (Figures 5 and 6), calculate f_{TH} as follows:

$$f_{TH} = \frac{1}{t_{QUIET} + \frac{16 + 3 \times (N-1) + 1}{f_{CLK}}}$$

where N is the number of active channels and t_{QUIET} includes acquistion time t_{ACQ}. t_{QUIET} is the period of bus inactivity before the rising edge of CONVST. Typically use t_{QUIET} = t_{ACQ} + 50ns, and prevent disturbance on the output bus from corrupting signal acquistion. See the *Starting a Conversion* section for more information.

Reading a Conversion Result

Reading During a Conversion

Figures 5 and 6 show the interface signals for initiating a read operation during a conversion cycle. These figures show two channels selected for conversion. If more channels are selected, the results are available successively every third clock cycle. $\overline{CS}$ can be low at all times; it can be low during the $\overline{RD}$ cycles, or it can be the same as $\overline{RD}$.

After initiating a conversion by bringing CONVST high, wait for $\overline{EOC}$ to go low (about 1.6µs in internal-clock mode or 17 clock cycles in external-clock mode) before reading the first conversion result. Read the conversion result by bringing $\overline{RD}$ low, thus latching the data to the parallel digital-output bus. Bring $\overline{RD}$ high to release the digital bus. Wait for the next falling edge of $\overline{EOC}$ (about 300ns in internal-clock mode or three clock cycles in external-clock mode) before reading the next result. When the last result is available, $\overline{EOLC}$ goes low.

Table 3. Throughput vs. Channels Sampled (t_{QUIET} = t_{ACQ} = 200ns, f_{CLK} = 10MHz)

CHANNELS SAMPLED (N)	CLOCK CYCLES UNTIL LAST RESULT	CLOCK CYCLE FOR READING LAST CONVERSION	TOTAL CONVERSION TIME (ns)	SAMPLES PER SECOND (ksps)	THROUGHPUT PER CHANNEL (ksps)
1	16	1	1900	526	526
2	19	1	2200	909	455
3	22	1	2500	1200	400
4	25	1	2800	1429	357
5	28	1	3100	1613	323
6	31	1	3400	1765	294
7	34	1	3700	1892	270
8	37	1	4000	2000	250

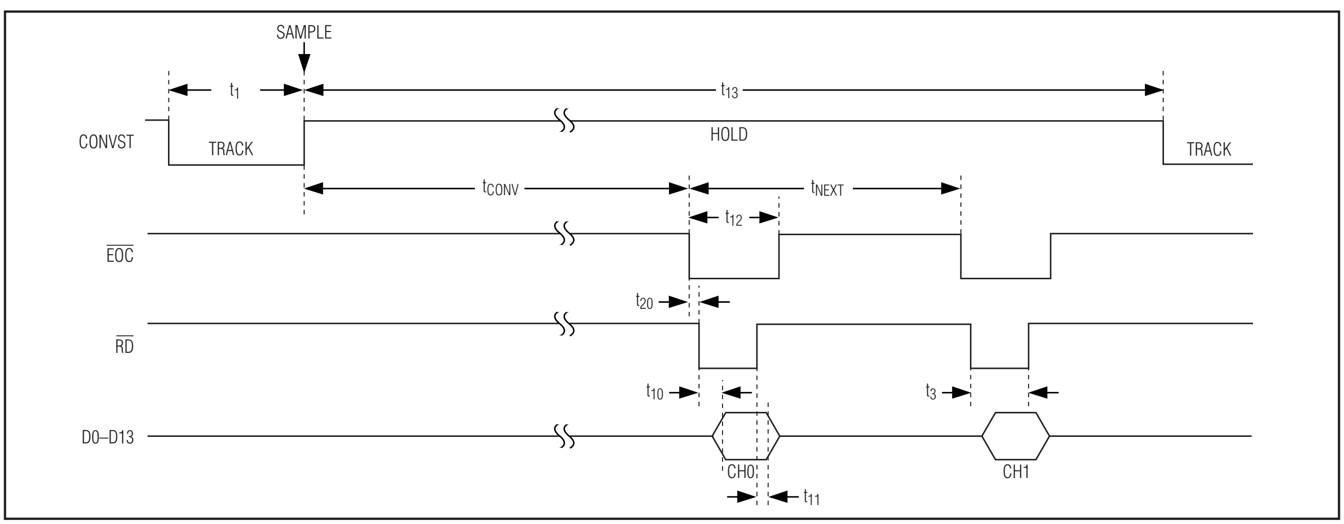


Figure 5. Read During Conversion—Two Channels Selected, Internal Clock

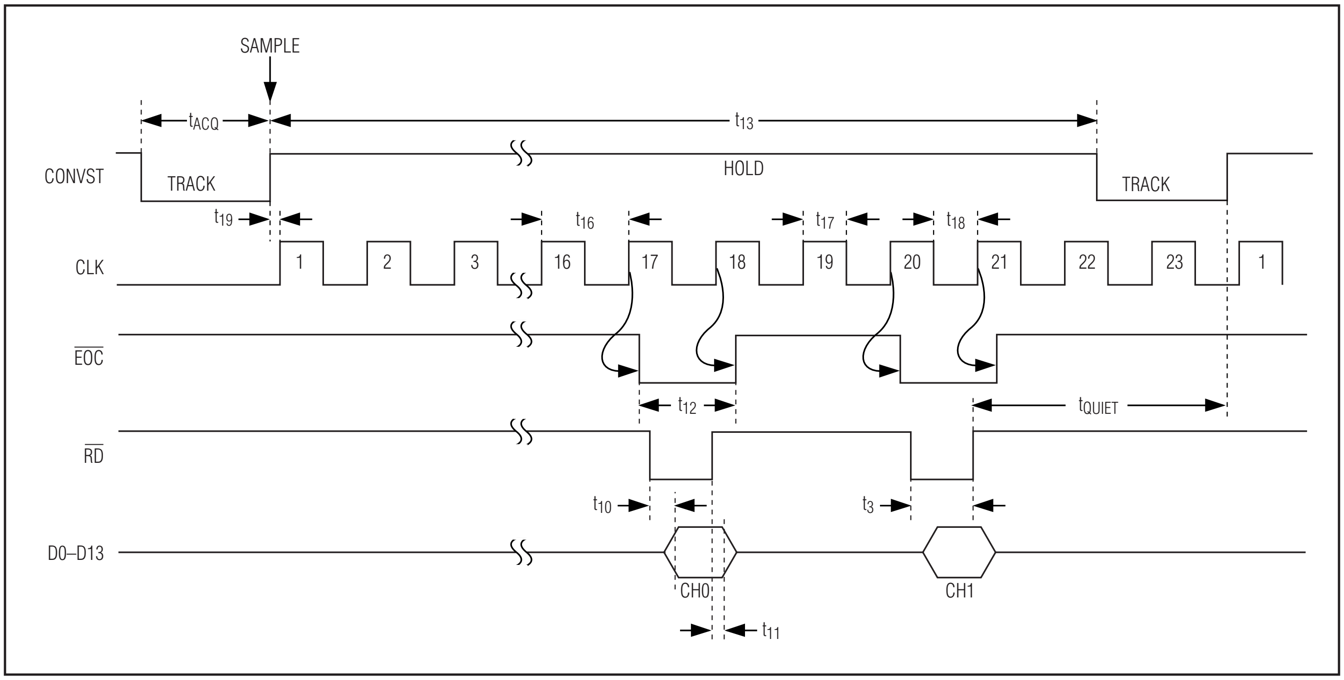


Figure 6. Read During Conversion—Two Channels Selected, External Clock

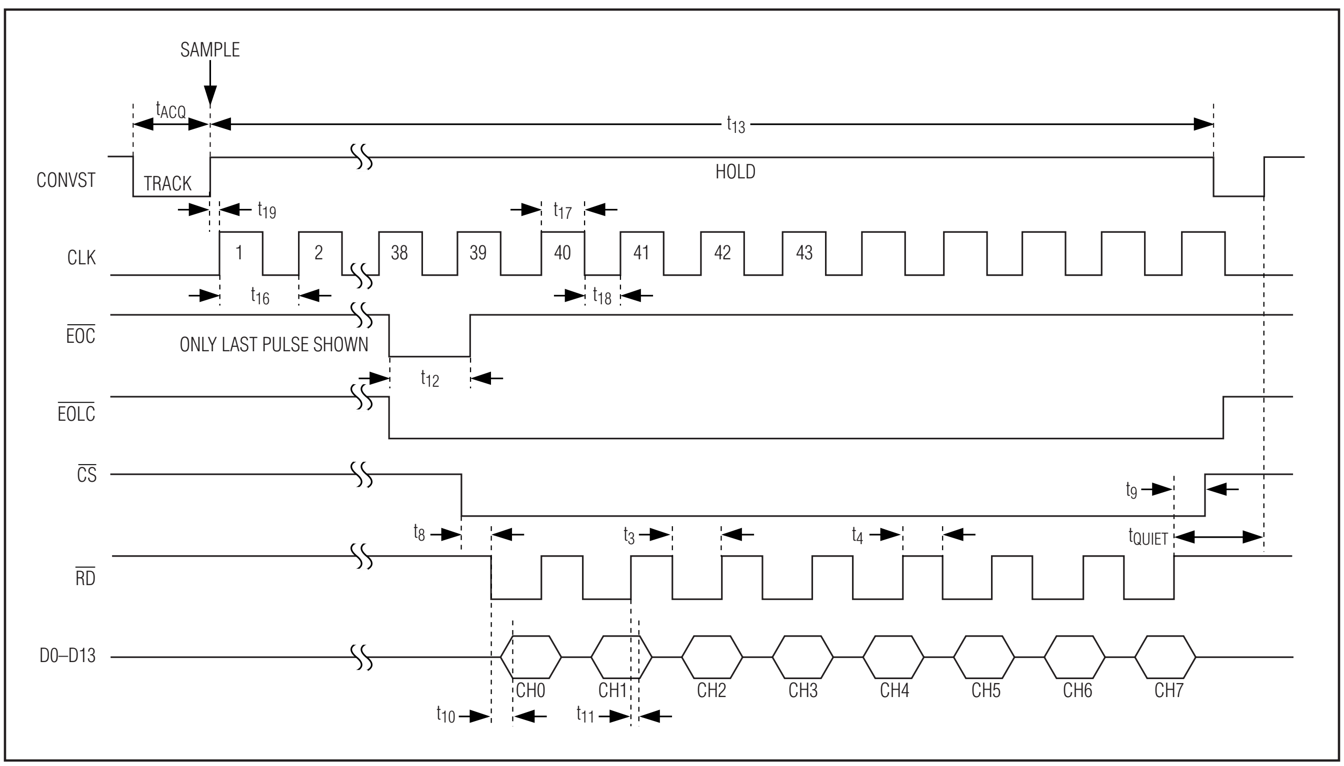


Figure 7. Reading After Conversion—Eight Channels Selected, External Clock

Reading After Conversion

Figure 7 shows the interface signals for a read operation after a conversion with all eight channels enabled. At the falling edge of $\overline{EOLC}$, on the 38th clock pulse after the initiation of a conversion, driving $\overline{CS}$ and $\overline{RD}$ low places the first conversion result onto the parallel bus, which can be latched on the rising edge of $\overline{RD}$. Successive low pulses of $\overline{RD}$ place the successive conversion results onto the bus. Pulse CONVST low to initiate a new conversion.

Power-Up Reset

At power-up, all channels are selected for conversion (see the *Configuration Register* section). After applying power, allow a 1.0ms wake-up time to elapse before initiating the first conversion. Then, hold CONVST high for at least 2.0μs after the wake-up time is complete. If using an external clock, apply 20 clock pulses to CLK with CONVST high before initiating the first conversion.

Reference

Internal Reference

The internal-reference circuits provide for analog input voltages of 0 to +5V unipolar (MAX1316/MAX1317/MAX1318), ±5V bipolar (MAX1320/MAX1321/MAX1322), or ±10V bipolar (MAX1324/MAX1325/MAX1326). Install external capacitors for reference stability, as indicated in Table 4, and as shown in the *Typical Operating Circuits*.

External Reference

Connect a +2.0V to +3.0V external reference at REF_{MS} and/or REF. When connecting an external reference, the input impedance is typically 5kΩ. The external reference must be able to drive 200μA of current and have a low output impedance. For more information about using external references see the *Transfer Functions* section.

Layout, Grounding, and Bypassing

For best performance use PC boards with ground planes. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), or do not run digital lines underneath the ADC package. Figure 8 shows the recommended system ground connections when not using a ground plane. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this ground.

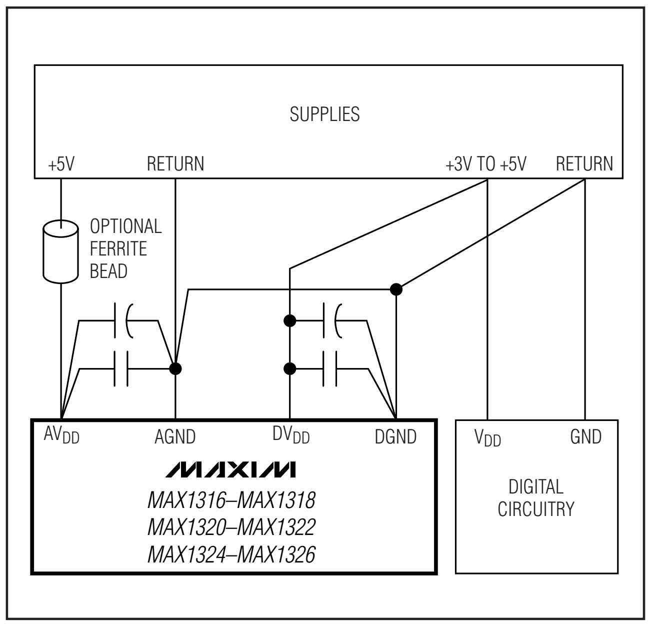


Figure 8. Power-Supply Grounding and Bypassing

Table 4. Reference Bypass Capacitors

LOCATION	INPUT VOLTAGE RANGE	
	UNIPOLAR (μF)	BIPOLAR (μF)
MSV bypass capacitor to AGND	2.2 II 0.1	NA
REF_{MS} bypass capacitor to AGND	0.01	0.01 (connect REF_{MS} to REF)
REF bypass capacitor to AGND	0.01	0.01 (connect REF_{MS} to REF)
REF+ bypass capacitor to AGND	0.1	0.1
REF+ to REF- capacitor	2.2 II 0.1	2.2 II 0.1
REF- bypass capacitor to AGND	0.1	0.1
COM bypass capacitor to AGND	2.2 II 0.1	2.2 II 0.1

NA = Not applicable (connect MSV directly to AGND).

No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation. High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 2.2µF bypass capacitors close to the device. If the +5V power supply is very noisy, a ferrite bead can be connected as a lowpass filter, as shown in Figure 8.

Transfer Functions

Bipolar ±10V Devices

Table 5 and Figure 9 show the two's complement transfer function for the MAX1324/MAX1325/MAX1326 with a ±10V input range. The full-scale input range (FSR) is eight times the voltage at REF. The internal +2.500V reference gives a +20V FSR, while an external +2V to +3V reference allows an FSR of +16V to +24V, respectively. Calculate the LSB size using the following equation:

$$LSB = \frac{8 \times V_{REF}}{2^{14}}$$

This equals 1.2207mV with a +2.5V internal reference.

The input range is centered about V_{MSV}. Normally, MSV = AGND, and the input is symmetrical about zero. For a custom midscale voltage, drive MSV with an external voltage source. Noise present on MSV directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum FSR, be careful not to violate the absolute maximum voltage ratings of the analog inputs when choosing V_{MSV}.

Determine the input voltage as a function of V_{REF}, V_{MSV}, and the output code in decimal using the following equation:

$$V_{CH\_} = LSB \times CODE_{10} + V_{MSV}$$

Bipolar ±5V Devices

Table 6 and Figure 10 show the two's complement transfer function for the MAX1320/MAX1321/MAX1322 with a ±5V input range. The FSR is four times the voltage at REF. The internal +2.500V reference gives a +10V FSR, while an external +2V to +3V reference allows an FSR of +8V to +12V, respectively. Calculate the LSB size using the following equation:

$$LSB = \frac{4 \times V_{REF}}{2^{14}}$$

This equals 0.6104mV when using the internal reference.

Table 5. ±10V Bipolar Code Table

TWO'S COMPLEMENT BINARY OUTPUT CODE	DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	INPUT VOLTAGE (V) (V_{REF} = 2.5V, V_{MSV} = 0V)
01 1111 1111 1111 0x1FFF	8191	9.9994 ±0.5 LSB
01 1111 1111 1110 0x1FFE	8190	9.9982 ±0.5 LSB
00 0000 0000 0001 0x0001	1	0.0018 ±0.5 LSB
00 0000 0000 0000 0x0000	0	0.0006 ±0.5 LSB
11 1111 1111 1111 0x3FFF	-1	-0.0006 ±0.5 LSB
10 0000 0000 0001 0x2001	-8191	-9.9982 ±0.5 LSB
10 0000 0000 0000 0x2000	-8192	-9.9994 ±0.5 LSB

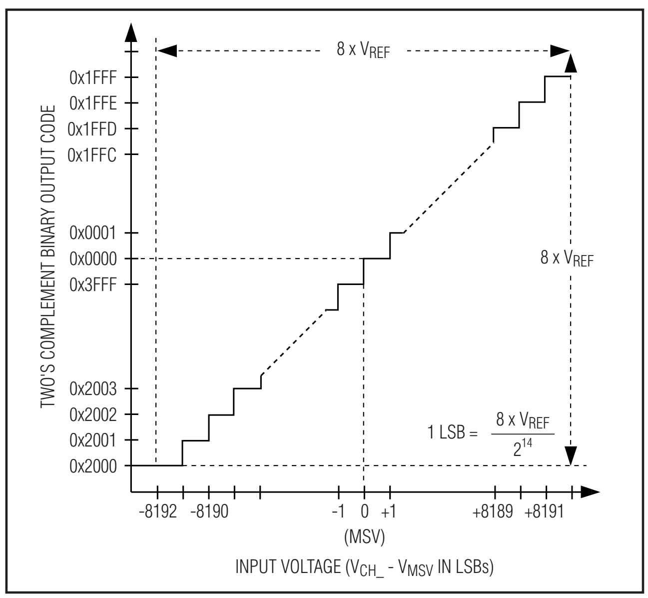


Figure 9. ±10V Bipolar Transfer Function

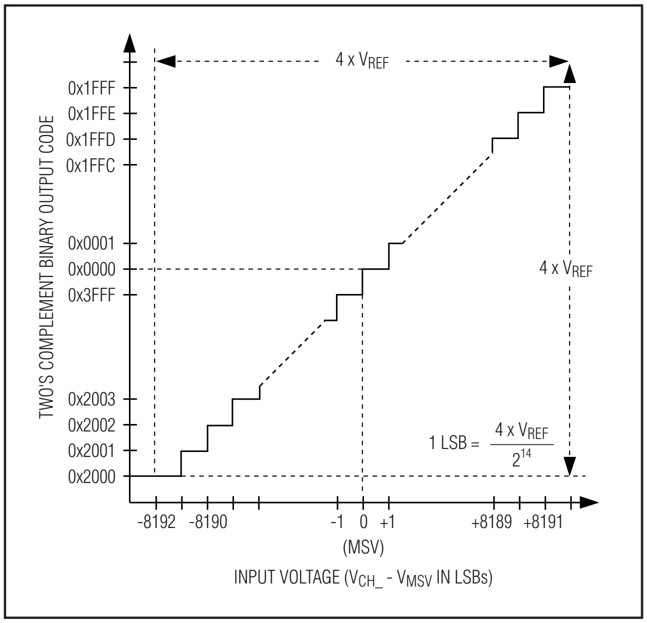


Figure 10. ±5V Bipolar Transfer Function

The input range is centered about V_{MSV}. Normally, MSV = AGND, and the input is symmetrical about zero. For a custom midscale voltage, drive MSV with an external voltage source. Noise present on MSV directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum FSR, be careful not to violate the absolute maximum voltage ratings of the analog inputs when choosing V_{MSV}. Determine the input voltage as a function of V_{REF}, V_{MSV}, and the output code in decimal using the following equation:

$$V_{CH\_} = LSB \times CODE_{10} + V_{MSV}$$

Unipolar 0 to +5V Devices

Table 7 and Figure 11 show the offset binary transfer function for the MAX1316/MAX1317/MAX1318 with a 0 to +5V input range. The FSR is two times the voltage at REF. The internal +2.500V reference gives a +5V FSR, while an external +2V to +3V reference allows an FSR of +4V to +6V, respectively. Calculate the LSB size using the following equation:

$$LSB = \frac{2 \times V_{REF}}{2^{14}}$$

This equals 0.3052mV when using the internal reference.

Table 6. ±5V Bipolar Code Table

TWO'S COMPLEMENT BINARY OUTPUT CODE	DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	INPUT VOLTAGE (V) (V_{REF} = 2.5V, V_{MSV} = 0V)
01 1111 1111 1111 0x1FFF	8191	4.9997 ±0.5 LSB
01 1111 1111 1110 0x1FFE	8190	4.9991 ±0.5 LSB
00 0000 0000 0001 0x0001	1	0.0009 ±0.5 LSB
00 0000 0000 0000 0x0000	0	0.0003 ±0.5 LSB
11 1111 1111 1111 0x3FFF	-1	-0.0003 ±0.5 LSB
10 0000 0000 0001 0x2001	-8191	-4.9991 ±0.5 LSB
10 0000 0000 0000 0x2000	-8192	-4.9997 ±0.5 LSB

Table 7. 0 to +5V Unipolar Code Table

BINARY OUTPUT CODE	DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	INPUT VOLTAGE (V) (V_{REF} = V_{REFMS} = 2.5V)
11 1111 1111 1111 0x3FFF	16383	4.9998 ±0.5 LSB
11 1111 1111 1110 0x3FFE	16382	4.9995 ±0.5 LSB
10 0000 0000 0001 0x2001	8193	2.5005 ±0.5 LSB
10 0000 0000 0000 0x2000	8192	2.5002 ±0.5 LSB
01 1111 1111 1111 0x1FFF	8191	2.4998 ±0.5 LSB
00 0000 0000 0001 0x0001	1	0.0005 ±0.5 LSB
00 0000 0000 0000 0x0000	0	0.0002 ±0.5 LSB

8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

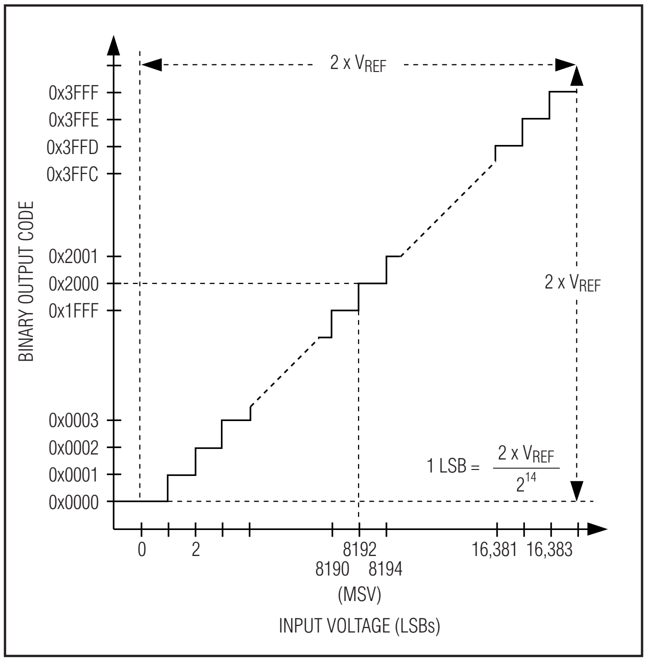


Figure 11. 0 to +5V Unipolar Transfer Function

The input range is centered about V_{MSV}, which is internally set to +2.500V. For a custom midscale voltage, drive REF_{MS} with an external voltage source and MSV will follow REF_{MS}. Noise present on MSV or REF_{MS} directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum FSR, be careful not to violate the absolute maximum voltage ratings of the analog inputs when choosing V_{MSV}. Determine the input voltage as a function of V_{REF}, V_{MSV}, and the output code in decimal using the following equation:

$$V_{CH\_} = LSB \times CODE_{10} + (V_{MSV} - 2.500V)$$

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Unipolar Offset Error

For the unipolar MAX1316/MAX1317/MAX1318, the ideal zero-scale transition from 0x0000 to 0x0001 occurs at 1 LSB (see Figure 11). The unipolar offset error is the amount of deviation between the measured zero-scale transition point and the ideal zero-scale transition point.

Bipolar Offset Error

For the bipolar MAX1320/MAX1321/MAX1322/MAX1324/MAX1325/MAX1326, the ideal zero-point transition from 0x3FFF to 0x0000 occurs at MSV, which is usually connected to ground (see Figures 9 and 10). The bipolar offset error is the amount of deviation between the measured zero-point transition and the ideal zero-point transition.

Gain Error

The ideal full-scale transition from 0x1FFE to 0x1FFF occurs at 1 LSB below full scale (see the *Transfer Functions* section). The gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point, once offset error has been nullified.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

where N = 14 bits.

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$SINAD(dB) = 20 \times \log \left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}} \right]$$

Effective Number of Bits

The effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture Jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the other channels. Channel-to-channel isolation is measured by applying DC to channels 1 to 7, while a -0.5dBFS sine wave is applied to channel 0. A 100kHz FFT is taken for channel 0 and channel 1. Channel-to-channel isolation is expressed in dB as the power ratio of the two 100kHz magnitudes.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

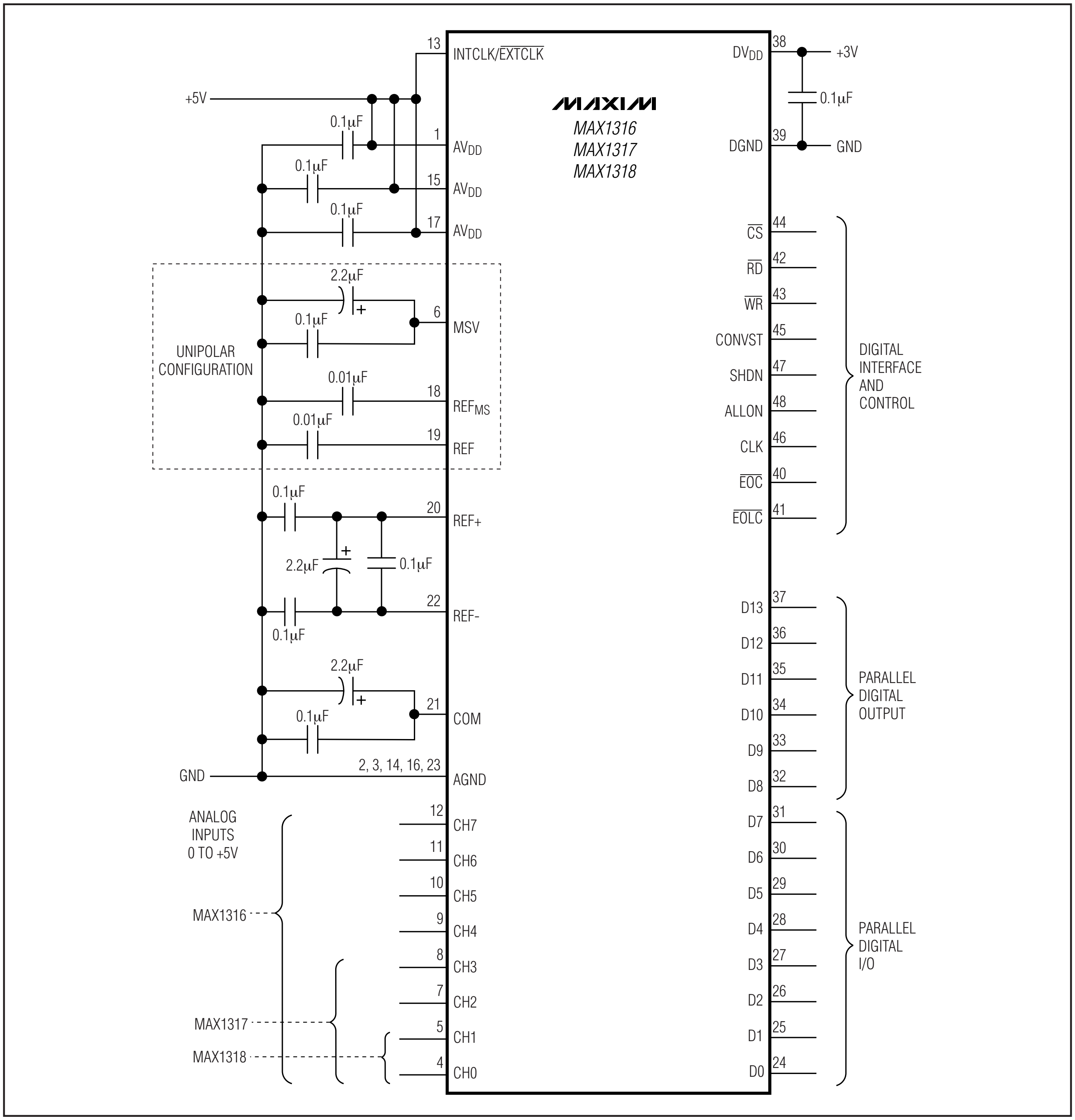
Chip Information

TRANSISTOR COUNT: 80,000

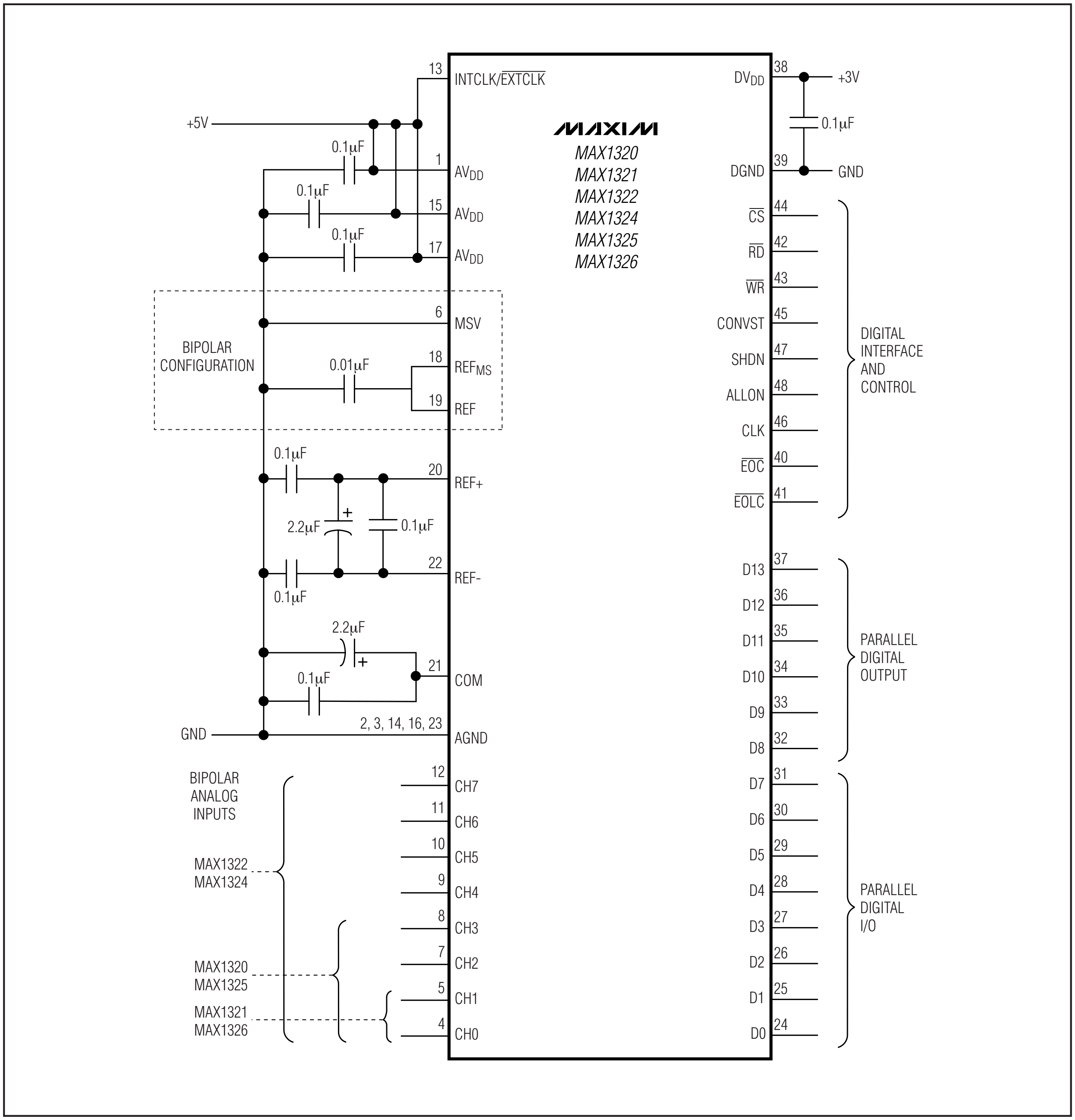
PROCESS: BiCMOS 0.6µm

8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Typical Operating Circuits

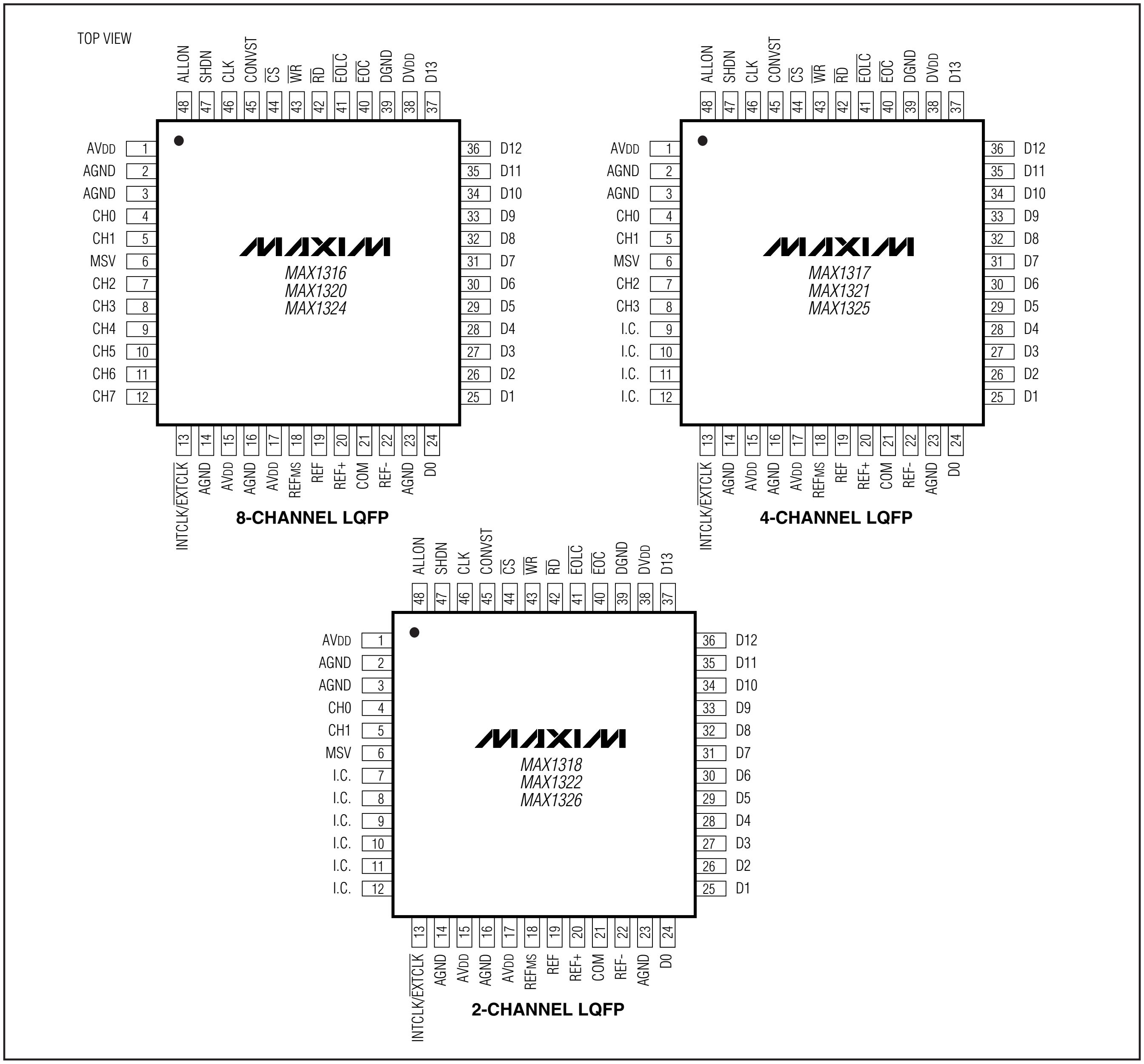


Typical Operating Circuits (continued)



8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Pin Configurations



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	C48-6	21-0054

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	2/07	Corrected units for input resistance in EC table	3
4	10/08	Changed specs for analog and digital supply current in EC table	4