Low-Cost, Multichemistry Battery-Charger Building Block

ABSOLUTE MAXIMUM RATINGS

DCIN, CSSP, CSSN to GND .....-0.3V to +30V
BST to GND .....-0.3V to +36V
BST to LX.....-0.3V to +6V
DHI to LX.....-0.3V to (V_{BST} + 0.3V)
LX to GND .....-6V to +30V
BATT, CSIP, CSIN to GND.....-0.3V to 20V
CSIP to CSIN or CSSP to CSSN or PGND to GND .....-0.3V to +0.3V
CCI, CCS, CCV, DLO, ICHG, IINP, ACIN, REF to GND .....-0.3V to (V_{LDO} + 0.3V)
DLOV, VCTL, ICTL, REFIN, CELLS, CLS, LDO, ACOK to GND .....-0.3V to +6V
DLOV to LDO.....-0.3V to +0.3V
DLO to PGND .....-0.3V to (V_{DLOV} + 0.3V)
LDO Short-Circuit Current 50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 12.6mW/°C above +70°C).....1008mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1) .....79.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1) .....27°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3.0V, V_{VCTL} = V_{ICTL} = 0.75 × V_{REFIN}, V_{CELLS} = 2.0V, V_{ACIN} = 0V, CLS = REF, V_{BST} - V_{LX} = 4.5V, V_{GND} = V_{PGND} = 0V, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; pins CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND LDO REGULATOR						
DCIN Input Voltage Range	V_{DCIN}		8		28	V
DCIN Undervoltage Lockout Trip Point		V_{DCIN} falling	7.0	7.4		V
		V_{DCIN} rising		7.5	7.85	
DCIN Quiescent Current	I_{DCIN}	8.0V < V_{DCIN} < 28V		2.7	6.0	mA
LDO Output Voltage		8.0V < V_{DCIN} < 28V, no load	5.25	5.40	5.55	V
LDO Load Regulation		0 < I_{LDO} < 10mA		34	100	mV
LDO Undervoltage Lockout Trip Point		V_{DCIN} = 8.0V	3.20	4.00	5.15	V
REF Output Voltage		0 < I_{REF} < 500µA	4.072	4.096	4.120	V
REF Undervoltage Lockout Trip Point		V_{REF} falling		3.1	3.9	V
TRIP POINTS						
BATT POWER_FAIL Threshold		V_{CSSP} falling	50	100	150	mV
BATT POWER_FAIL Threshold Hysteresis			100	200	300	mV
ACIN Threshold		V_{ACIN} rising	2.007	2.048	2.089	V
ACIN Threshold Hysteresis		0.5% of V_{REF}	10	20	30	mV
ACIN Input Bias Current		V_{ACIN} = 2.048V	-1		+1	µA
CLS Input Range			1.6		REF	V
CLS Input Bias Current		V_{CLS} = 2.0V	-1		+1	µA
SWITCHING REGULATOR						
Minimum Off-Time		V_{BATT} =16.8V	1.00	1.25	1.50	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3.0V, V_{VCTL} = V_{ICTL} = 0.75 × V_{REFIN}, V_{CELLS} = 2.0V, V_{ACIN} = 0V, CLS = REF, V_{BST} - V_{LX} = 4.5V, V_{GND} = V_{PGND} = 0V, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; pins CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum On-Time			5	10	15	ms
Oscillator Frequency	f_{OSC}	(Note 2)			400	kHz
DLOV Supply Current	I_{DLOV}	DLO low		5	10	µA
BST Supply Current	I_{BST}	DHI high		6	15	µA
LX Input Bias Current		V_{DCIN} = 28V, V_{BATT} = V_{LX} = 20V		150	500	µA
LX Input Quiescent Current		V_{DCIN} = 0V, V_{BATT} = V_{LX} = 20V		0.3	1.0	µA
DHI Maximum Duty Cycle			99.0	99.9		%
DHI On-Resistance High		V_{BST} - V_{LX} = 4.5V, I_{DHI} = +100mA		4	7	Ω
DHI On-Resistance Low		V_{BST} - V_{LX} = 4.5V, I_{DHI} = -100mA		1	2	Ω
DLO On-Resistance High		V_{DLOV} = 4.5V, I_{DLO} = +100mA		4	7	Ω
DLO On-Resistance Low		V_{DLOV} = 4.5V, I_{DLO} = -100mA		1	2	Ω
BATT Input Current	I_{BATT}	V_{BATT} = 19V, V_{DCIN} = 0V			5	µA
		V_{BATT} = 2V to 19V, V_{DCIN} > V_{BATT} + 0.3V		200	500	
CSIP/CSIN Input Current		V_{DCIN} = 0V		1	5	µA
		V_{CSIP} = V_{CSIN} = 12V			800	
CSSP/CSSN Input Current		V_{DCIN} = 0V		0.1	0.3	µA
		V_{CSSP} = V_{CSSN} = V_{DCIN} > 8.0V			800	
BATT/CSIP/CSIN Input Voltage Range			0		19	V
CSIP to CSIN Full-Scale Current-Sense Voltage		V_{BATT} = 12V	189	204	219	mV
CSSP to CSSN Full-Scale Current-Sense Voltage			189	204	219	mV
ERROR AMPLIFIERS						
GMV Amplifier Transconductance		VCTL = REFIN, V_{BATT} = 16.8V, CELLS = LDO	0.0625	0.1250	0.250	µS
GMI Amplifier Transconductance		ICTL = REFIN, V_{CSIP} - V_{CSIN} = 150.4mV	0.5	1	2	µS
GMS Amplifier Transconductance		V_{CLS} = 2.048V, V_{CSSP} - V_{CSSN} = 102.4mV	0.5	1	2	µS
CCI/CCS/CCV Clamp Voltage		0.25V < V_{CCI}, V_{CCS}, V_{CCV} < 2.0V	150	300	600	mV
CURRENT AND VOLTAGE SETTING						
Charging-Current Accuracy		ICTL = REFIN (see Equation 2)	-8		+8	%
		ICTL = REFIN/32 (see Equation 2)	-55		+55	
ICTL, VCTL, REFIN Input Bias Current		V_{VCTL} = V_{ICTL} = V_{REFIN} = 3V	-1		+1	µA
		V_{DCIN} = 0, V_{VCTL} = V_{ICTL} = V_{REFIN} = 5V	-1		+1	
ICTL Power-Down Mode Threshold Voltage			REFIN /100	REFIN /55	REFIN /33	V

Low-Cost, Multichemistry Battery-Charger Building Block

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3.0V, V_{VCTL} = V_{ICTL} = 0.75 × V_{REFIN}, V_{CELLS} = 2.0V, V_{ACIN} = 0V, CLS = REF, V_{BST} - V_{LX} = 4.5V, V_{GND} = V_{PGND} = 0V, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; pins CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery-Regulation Voltage Accuracy		V_{VCTL} = V_{REFIN} (2, 3, or 4 cells) (see Equation 1)	-0.5		+0.5	%
		V_{VCTL} = V_{REFIN}/20 (2, 3, or 4 cells) (see Equation 1)	-0.5		+0.5	
REFIN Range			2.0		3.6	V
REFIN Undervoltage Lockout				1.20	1.92	V
ICHG Transconductance		V_{ICHG} to (V_{CSIP} - V_{CSIN}); V_{CSIP} - V_{CSIN} = 0.185V; V_{ICHG} = 0V, 3.0V	0.95	1.00	1.05	µS
ICHG Accuracy		V_{CSIP} - V_{CSIN} = 0.185V	-5		+5	%
		V_{CSIP} - V_{CSIN} = 0.05V	-10		+10	
IINP Transconductance		V_{IINP} to (V_{CSSP} - V_{CSSN}); V_{CSSP} - V_{CSSN} = 0.185V; V_{IINP} = 0V, 3.0V (Note 3)	0.85	1.00	1.15	µS
IINP Current Accuracy		V_{CSSP} - V_{CSSN} = 0.185V (Note 3)	-15		+15	%
		V_{CSSP} - V_{CSSN} = 0.05V (Note 3)	-20		+20	
CSSP - CSSN Accuracy		V_{CSSP} - V_{CSSN} = 0.08V, V_{CLS} = 1.6V	-10		+10	%
		V_{CSSP} - V_{CSSN} = 0.2V, CLS = REF	-10		+10	
CSSP + CSSN Input Voltage Range			8.0		28	V
LOGIC LEVELS						
CELLS Input Low Voltage					0.2	V
CELLS Input Middle Voltage			0.4		V_{LDO} - 0.5	V
CELLS Input High Voltage			V_{LDO} - 0.25		V_{LDO}	V
CELLS Input Bias Current		V_{CELLS} = 0V or V_{LDO}	-10		+10	µA
ACOK Sink Current		V_{ACOK} = 0.4V	1			mA
ACOK Leakage Current		V_{ACOK} = 5.5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3.0V, V_{VCTL} = V_{ICTL} = 0.75 × V_{REFIN}, V_{CELLS} = 2.0V, V_{ACIN} = 0V, CLS = REF, V_{BST} - V_{LX} = 4.5V, V_{GND} = V_{PGND} = 0V, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; pins CCI, CCS, and CCV are compensated per Figure 1a; **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND LDO REGULATOR						
DCIN Input Voltage Range	V_{DCIN}		8.0		28.0	V
DCIN Undervoltage Lockout Trip Point		V_{DCIN} falling	7			V
		V_{DCIN} rising			7.85	
DCIN Quiescent Current	I_{DCIN}	8.0V < V_{DCIN} < 28V			6	mA
LDO Output Voltage		8.0V < V_{DCIN} < 28V, no load	5.25		5.65	V
TRIP POINTS						
BATT POWER_FAIL Threshold		V_{CSSP} falling	50		150	mV
BATT POWER_FAIL Threshold Hysteresis			100		300	mV
ACIN Threshold		V_{ACIN} rising	2.007		2.089	V
ACIN Threshold Hysteresis		0.5% of REF	10		30	mV
ACIN Input Bias Current		V_{ACIN} = 2.048V	-1		+1	µA
CLS Input Range			1.6		REF	V
CLS Input Bias Current		V_{CLS} = 2.0V	-1		+1	µA
SWITCHING REGULATOR						
Minimum Off-Time		V_{BATT} = 16.8V	1		1.5	µs
Maximum On-Time			5		15	ms
Oscillator Frequency	f_{OSC}	(Note 1)			400	kHz
DHI Maximum Duty Cycle			99			%
BATT Input Current	I_{BATT}	V_{BATT} = 19V, V_{DCIN} = 0V			5	µA
		V_{BATT} = 2V to 19V, V_{DCIN} > V_{BATT} + 0.3V			500	
CSIP/CSIN Input Current		V_{DCIN} = 0V			5	µA
		V_{CSIP} = V_{CSIN} = 12V			800	
CSSP/CSSN Input Current		V_{DCIN} = 0V			0.3	µA
		V_{CSSP} = V_{CSSN} = V_{DCIN} > 8.0V			800	
BATT/CSIP/CSIN Input Voltage Range			0		19	V
CSIP to CSIN Full-Scale Current-Sense Voltage		V_{BATT} = 12V	189		219	mV
CSSP to CSSN Full-Scale Current-Sense Voltage			189		219	mV
CURRENT AND VOLTAGE SETTING						
Charging Current Accuracy		ICTL = REFIN (see Equation 2)	-8		+8	%
		ICTL = REFIN/32 (see Equation 2)	-55		+55	
ICTL, VCTL, REFIN Input Bias Current		V_{VCTL} = V_{ICTL} = V_{REFIN} = 3V	-1		+1	µA
		V_{DCIN} = 0V, V_{VCTL} = V_{ICTL} = V_{REFIN} = 5V	-1		+1	

Low-Cost, Multichemistry Battery-Charger Building Block

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3.0V, V_{VCTL} = V_{ICTL} = 0.75 × V_{REFIN}, V_{CELLS} = 2.0V, V_{ACIN} = 0V, CLS = REF, V_{BST} - V_{LX} = 4.5V, V_{GND} = V_{PGND} = 0V, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; pins CCI, CCS, and CCV are compensated per Figure 1a; **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 1)

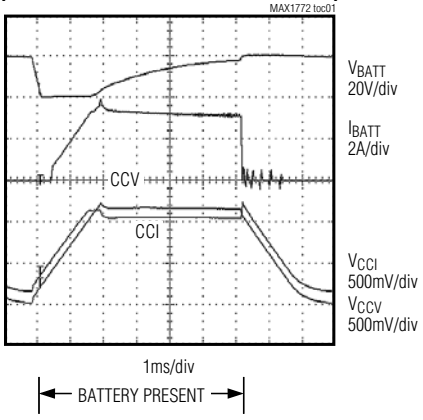
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ICTL Power-Down Mode Threshold Voltage			REFIN /100		REFIN /33	V
Battery Regulation Voltage Accuracy		V_{VCTL} = V_{REFIN} (2, 3, or 4 cells) (see Equation 1)	-1		+1	%
		V_{VCTL} = V_{REFIN}/20 (2, 3, or 4 cells) (see Equation 1)	-1		+1	
REFIN Range			2.0		3.6	V
REFIN Undervoltage Lockout					1.92	V
ICHG Accuracy		V_{CSIP} - V_{CSIN} = 0.185V	-5		+5	%
		V_{CSIP} - V_{CSIN} = 0.05V	-10		+10	
IINP Current Accuracy		V_{CSSP} - V_{CSSN} = 0.185V (Note 3)	-15		+15	%
		V_{CSSP} - V_{CSSN} = 0.05V (Note 3)	-20		+20	
CSSP - CSSN Accuracy		V_{CSSP} - V_{CSSN} = 0.08V, V_{CLS} = 1.6V	-10		+10	%
		V_{CSSP} - V_{CSSN} = 0.2V, CLS = REF	-10		+10	
CSSP + CSSN Input Voltage Range			8		28	V
LOGIC LEVELS						
CELLS Input Low Voltage					0.2	V
CELLS Input Middle Voltage			0.4		V_{LDO} - 0.5	V
CELLS Input High Voltage			V_{LDO} - 0.25		V_{LDO}	V
CELLS Input Bias Current		V_{CELLS} = 0V or V_{LDO}	-10		+10	µA
ACOK Sink Current		V_{ACOK} = 0.4V	1			mA
ACOK Leakage Current		V_{ACOK} = 5.5V	-1		+1	µA

Note 2: Guaranteed by design. Not production tested.
Note 3: Tested under DC conditions. See text for more detail.

Typical Operating Characteristics

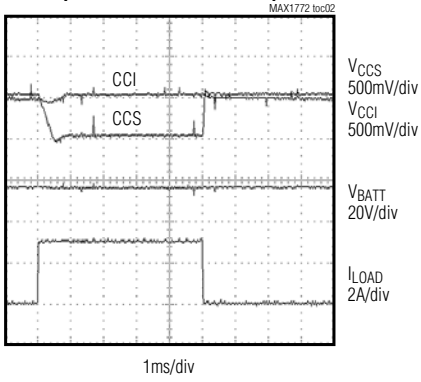
(Circuit of Figure 1a, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (BATTERY REMOVAL AND REINSERTION)



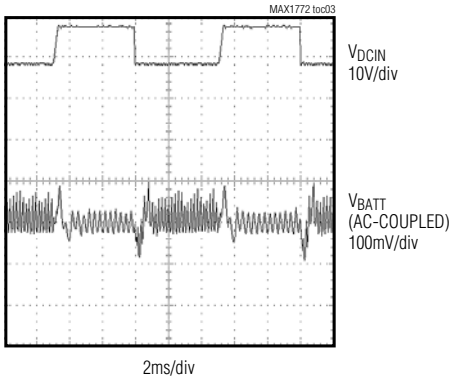
V_{ICTL} = 0.957V
V_{CTL} = 3.3V

LOAD-TRANSIENT RESPONSE (STEP-IN LOAD CURRENT)



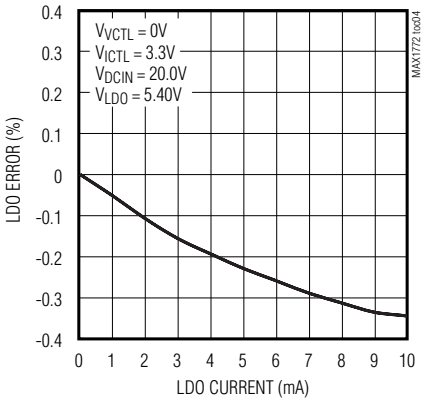
V_{ICTL} = 3.30V
CHARGING CURRENT = 2.0A
V_{BATT} = 16V
LOAD STEP = 0 TO 3A
I_{SOURCE} LIMIT = 5A

LINE-TRANSIENT RESPONSE



V_{BATT} = 16V
V_{DCIN} = 18.5V TO 27.5V
I_{LOAD} = 150mA

LDO LOAD REGULATION

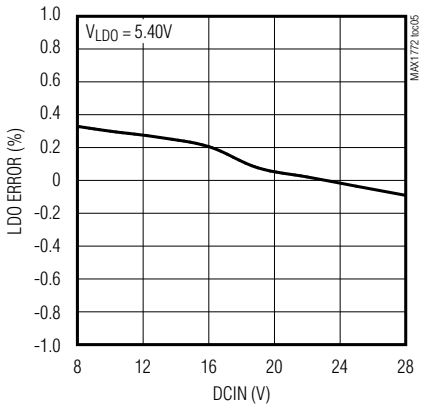


Low-Cost, Multichemistry Battery-Charger Building Block

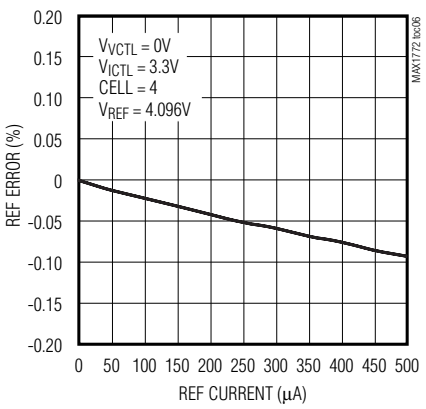
Typical Operating Characteristics (continued)

(Circuit of Figure 1a, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

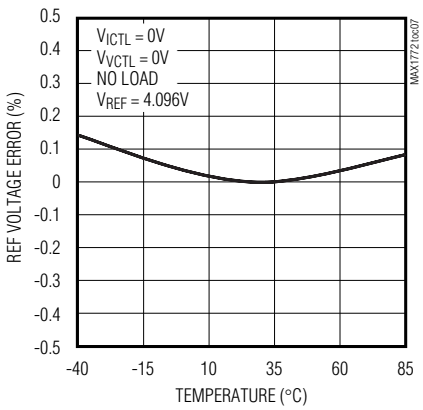
LDO LINE REGULATION



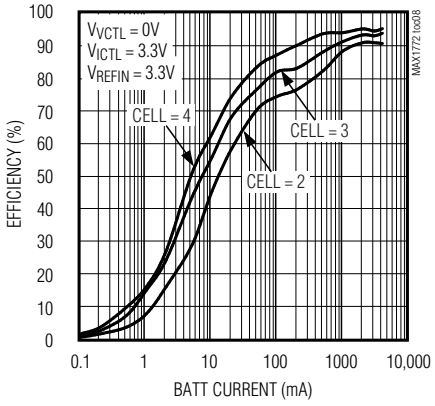
REF VOLTAGE LOAD REGULATION



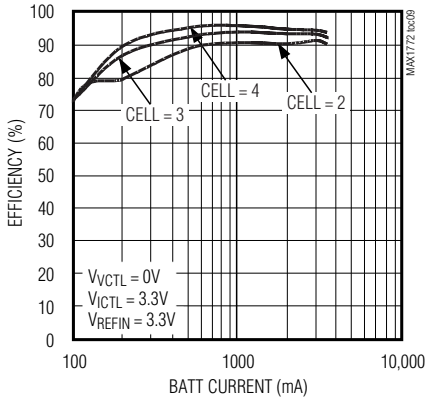
REF VOLTAGE ERROR vs. TEMPERATURE



EFFICIENCY vs. BATTERY CURRENT (VOLTAGE CONTROL LOOP)



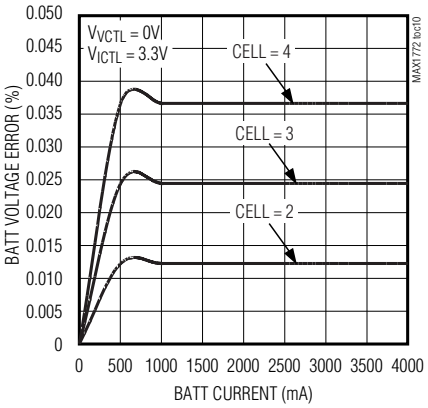
EFFICIENCY vs. BATTERY CURRENT (CURRENT CONTROL LOOP)



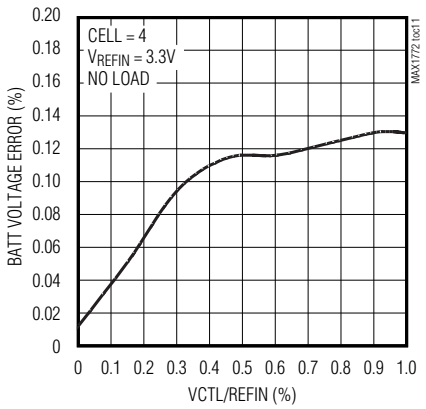
Typical Operating Characteristics (continued)

(Circuit of Figure 1a, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

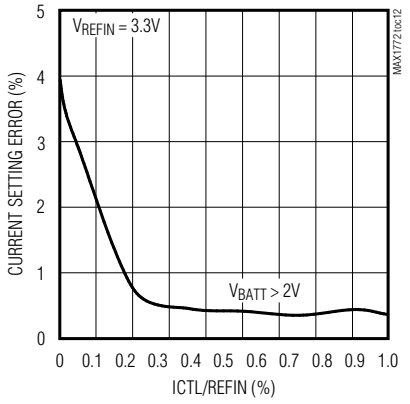
OUTPUT V/I CHARACTERISTICS



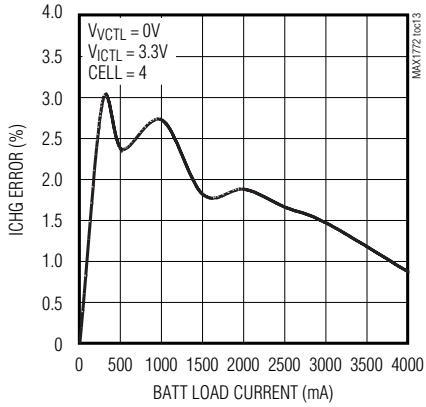
BATT VOLTAGE ERROR vs. VCTL



CURRENT SETTING ERROR vs. ICTL



ICHG ERROR vs. BATT LOAD CURRENT



Low-Cost, Multichemistry Battery-Charger Building Block

Pin Description

PIN	NAME	FUNCTION
1	DCIN	Charging Voltage Input
2	LDO	Device Power Supply. Output of the 5.4V linear regulator supplied from DCIN. Bypass LDO with a 1µF capacitor to GND.
3	CLS	Source Current-Limit Input. Voltage input for setting the current limit of the input source.
4	REF	4.096V Voltage Reference. Bypass REF with a 1µF capacitor to GND.
5	CCS	Input Current Regulation Loop Compensation Point. Connect a 0.01µF capacitor from CCS to GND.
6	CCI	Output Current Regulation Loop Compensation Point. Connect a 0.01µF capacitor from CCI to GND.
7	CCV	Voltage Regulation Loop Compensation Point. Connect 1kΩ resistor in series with a 0.1µF capacitor to GND.
8, 9	GND	Analog Ground
10	ICHG	ICHG is a scaled-down replica of the battery output current being sensed. It is used to monitor the charging current and indicates when the chip changes from voltage mode to current mode. The transconductance of (CSIP - CSIN) to ICHG is 1µS. Connect ICHG pin to GND if it is unused.
11	ACIN	AC Detect Input. Detects when the AC adapter voltage is available for charging.
12	ACOK	AC Detect Output. Open-drain output is high when ACIN is less than REF/2.
13	REFIN	Reference Input. Allows the ICTL and VCTL pins to have ratiometric ranges for increased DAC accuracy.
14	ICTL	Input for Setting Maximum Output Current. Range is REFIN/32 to REFIN. The device shuts down if this pin is forced below REFIN/55 (typ).
15	VCTL	Input for Setting Maximum Output Voltage. Range is 0 to REFIN.
16	CELLS	Trilevel Input for Setting Number of Cells. GND = 2 cells, LDO/2 = 3 cells, LDO = 4 cells.
17	BATT	Battery Voltage Input
18	CSIN	Output Current-Sense Negative Input
19	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
20	PGND	Power Ground
21	DLO	Low-Side Power MOSFET Driver Output. Connect DLO to a low-side nMOS gate.
22	DLOV	Low-Side Driver Supply
23	LX	Power Connection for the High-Side Power MOSFET Driver. Connect LX to a source of high-side nMOS.
24	DHI	High-Side Power MOSFET Driver Output. Connect DHI to a high-side nMOS gate.
25	BST	Power Connection for the High-Side Power MOSFET Driver. Connect a 0.1µF capacitor from LX to BST.
26	CSSN	Input Current-Sense for Charger (negative input)
27	CSSP	Input Current-Sense for Charger (positive input). Connect a current-sense resistor from CSSP to CSSN.
28	IINP	IINP is a scaled-down replica of the input current being sensed. It is used to monitor the total system current. The transconductance of (CSSP - CSSN) to IINP is 1mS. Connect IINP pin to GND if it is unused.

Detailed Description

The MAX1772 includes all of the functions necessary to charge Li+, NiMH, and NiCd batteries. A high-efficiency synchronous-rectified step-down DC-DC converter controls charging voltage and current. It also includes input source-current limiting and analog inputs for setting the charge current and charge voltage. The DC-DC converter uses external N-channel MOSFETs as the buck switch and synchronous rectifier to convert the input voltage to the required charging current and voltage. The typical application circuit shown in Figure 1a uses a microcontroller (µC) to allow control of charging current or voltage, while Figure 1b shows a typical application with charging voltage and current fixed to specific values for the application. The voltage at ICTL and the value of RS2 set the charging current. The DC-DC converter generates the control signals for the external MOSFETs to regulate the voltage and the current set by the VCTL, ICTL, and CELLS inputs.

The MAX1772 features a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by VCTL. The CCI battery current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by ICTL. A third loop (CCS) takes control and reduces the battery-charging current when the sum of the system load and the battery-charging current exceeds the charging source current limit set by CLS.

Setting the Battery Regulation Voltage

The MAX1772 uses a high-accuracy voltage regulator for charging voltage. The VCTL input adjusts the battery output voltage. VCTL is allowed to vary from 0 to REFIN (≈3.3V). The per-cell battery termination voltage is a function of the battery chemistry and construction; thus, consult the battery manufacturer to determine this voltage. The battery voltage is calculated by the equation:

$$V_{BATT} = CELLS \times \left(V_{REF} + \left(\frac{V_{REF}}{10} \times \frac{V_{VCTL}}{V_{REFIN}} \right) \right) \quad (1)$$

CELLS is the programming input for selecting cell count. Table 1 shows how CELLS is connected to charge 2, 3, or 4 cells. Use a voltage-divider from LDO to set the desired voltage at CELLS.

The internal error amplifier (GMV) maintains voltage regulation (Figure 2). The voltage error amplifier is compensated at CCV. The component values shown in Figure 1 provide suitable performance for most applications. Individual compensation of the voltage regulation and current-regulation loops allow for optimal compensation.

Setting the Charging-Current Limit

The ICTL input sets the maximum charging current. The current is set by current-sense resistor RS2, connected between CSIP and CSIN. The nominal differential voltage between CSIP and CSIN is 204mV; thus, for a 0.05Ω sense resistor, the maximum charging current is 4A. Battery-charging current is programmed with ICTL using the equation:

$$I_{CHG} = \frac{V_{REF}}{RS2} \times \frac{V_{ICTL}}{V_{REFIN}} \times \frac{1}{20} \quad (2)$$

The input range for ICTL is REFIN/32 to REFIN (≈3.3V). The device shuts down if ICTL is forced below REFIN/55 (typical). The current at ICHG is a scaled-down replica of the battery output current being sensed across CSIP and CSIN.

When choosing the current-sense resistor, note that the voltage drop across this resistor causes further power loss, reducing efficiency. However, adjusting ICTL to reduce the voltage across the current-sense resistor may degrade accuracy due to the input offset of the current-sense amplifier. The charging current-error amplifier (GMI) is compensated at CCI. A 0.01µF capacitor at CCI provides suitable performance for most applications.

Setting the Input Current Limit

The total input current (from a wall cube or other DC source) is a function of the system supply current and the battery-charging current. The input current regulator limits the source current by reducing the charging current when the input current exceeds the set input current limit. System current will normally fluctuate as portions of the system are powered up or put to sleep. Without input current regulation, the input source must be able to supply the maximum system current and the maximum charger input current. By using the input current limiter, the current capability of the AC wall adapter may be lowered, reducing system cost.

The MAX1772 limits the current drawn by the charger when the load current becomes high. The device limits the charging current, so the AC adapter voltage is not loaded down. An internal amplifier compares the voltage between CSSP and CSSN to the voltage at CLS. V_{CLS} can be set by a resistor-divider between REF and GND. Connect CLS to REF for maximum input current limiting.

Low-Cost, Multichemistry Battery-Charger Building Block

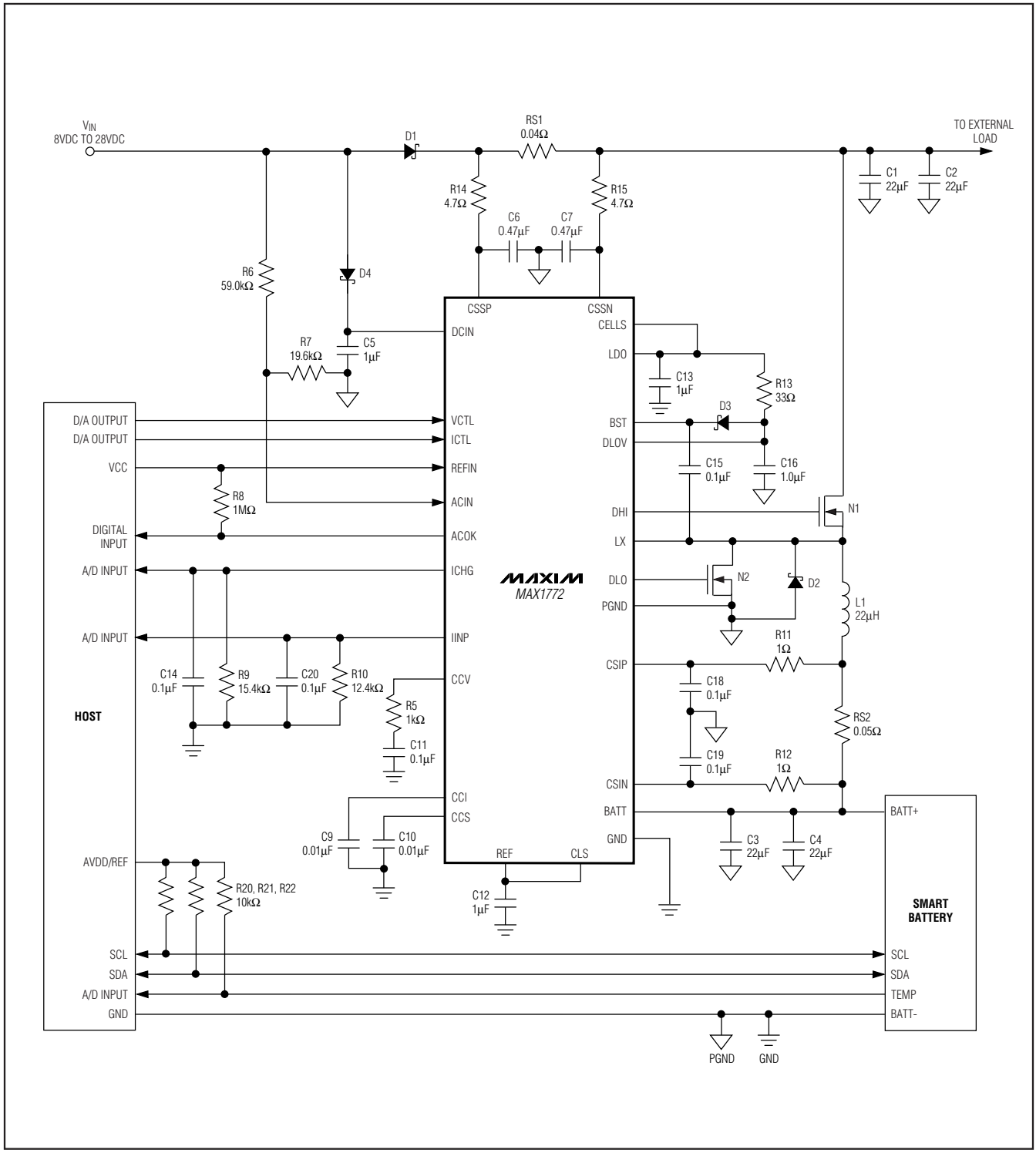


Figure 1a. µC-Controlled Typical Application Circuit

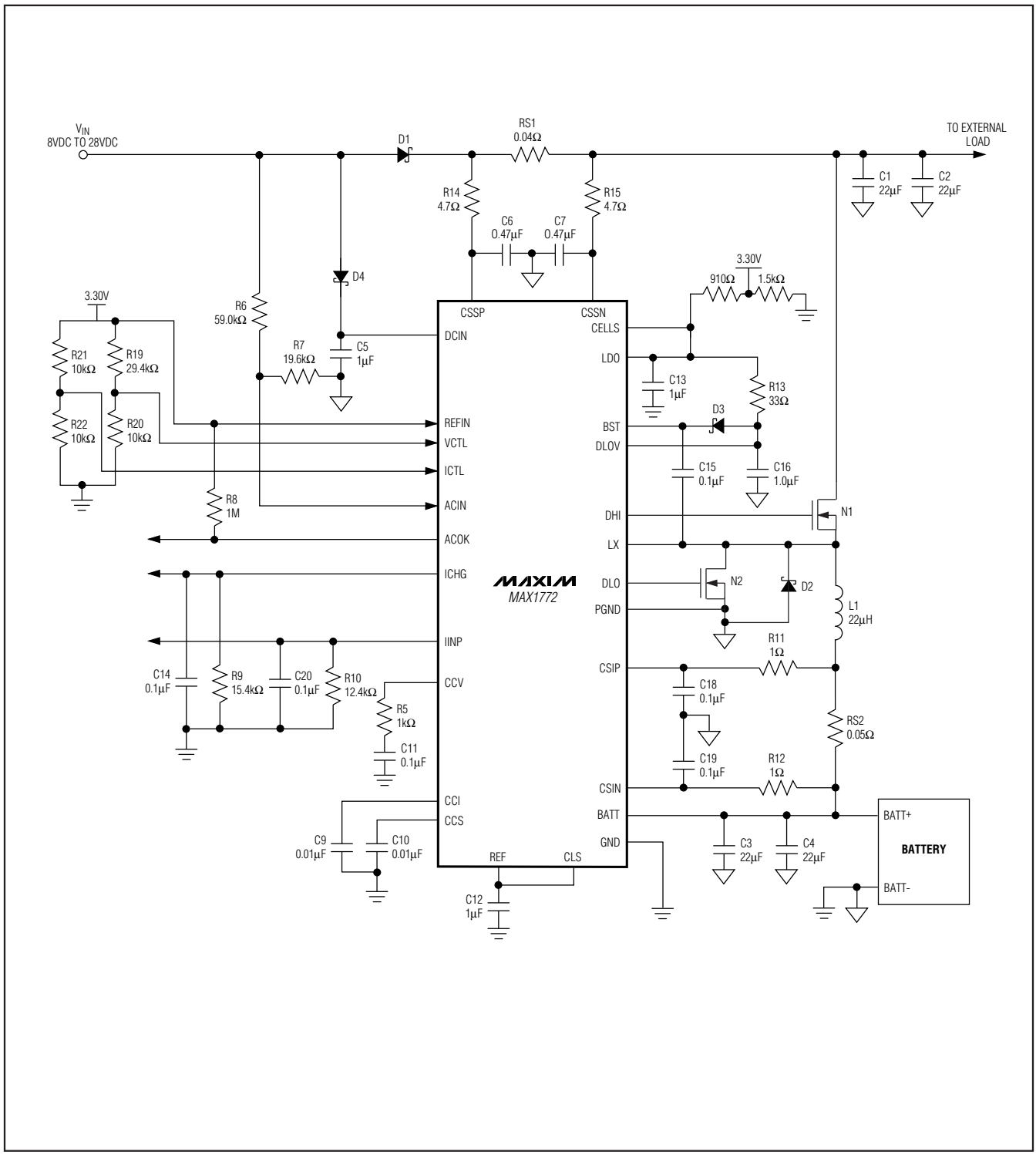


Figure 1b. Stand-Alone Typical Application Circuit

Low-Cost, Multichemistry Battery-Charger Building Block

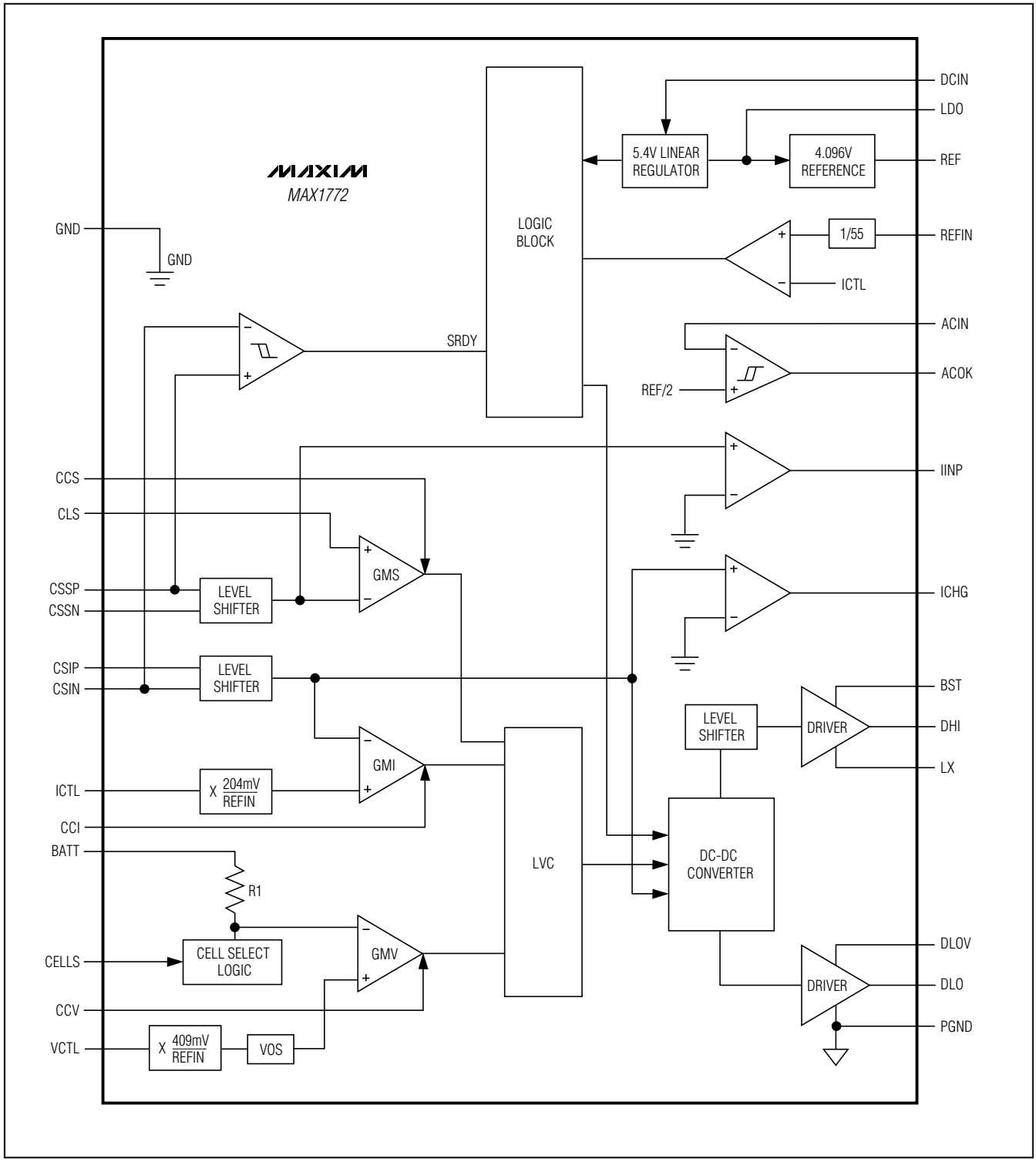


Figure 2. Functional Diagram

Table 1. Cell-Count Programming Table

CELL	CELL COUNT
V_{CELLS} < 0.20V	2
0.40V < V_{CELLS} < V_{LDO}-0.5V	3
V_{LDO} - 0.25V < V_{CELLS} < V_{LDO}	4

The input source current is the sum of the device current, the charger input current, and the load current. The device current is minimal (6mA) in comparison to the charge and load currents. The actual source current required is determined as follows:

$$I_{SOURCE} = I_{LOAD} + \left[\left(I_{CHARGE} \times V_{BATT}\right) / \left(V_{IN} \times \eta\right)\right] \quad (3)$$

where η is the efficiency of the DC-DC converter (85% to 95% typ).

V_{CLS} determines the reference voltage of the GMS error amplifier. Sense resistor RS1 sets the maximum allowable source current. Calculate the maximum current as follows:

$$I_{SOURCE\_MAX} = V_{CLS} / \left(20 \times RS1\right) \quad (4)$$

Once the input current limit is reached, the charging current is tapered back until the input current is below the desired threshold.

When choosing the current-sense resistor, note that the voltage drop across this resistor causes further power loss, reducing efficiency.

AC Adapter Detection

Connect the AC adapter voltage through a resistive divider to ACIN to detect when AC power is available, as shown in Figure 1. ACOK is an open-drain output and is high when ACIN is less than REF/2.

Current Measurement

Use ICHG to monitor the battery-charging current being sensed across CSIP and CSIN. The output voltage range is 0 to 3V. The voltage of ICHG is proportional to the output current by the equation:

$$V_{ICHG} = I_{ICHG} \times RS2 \times G_{ICHG} \times R9 \quad (5)$$

where I_{ICHG} is the battery-charging current, G_{ICHG} is the transconductance of ICHG (1mS typ), and R9 is the resistor connected between ICHG and ground.

Connect ICHG pin to ground if it is not used.

Use IINP to monitor the system input current being sensed across CSSP and CSSN. The output voltage range is 0 to 3V. The voltage of IINP is proportional to the output current by the equation:

$$V_{IINP} = I_{SOURCE} \times RS1 \times G_{IINP} \times R10 \quad (6)$$

where I_{SOURCE} is the DC current being supplied by the AC adapter power, G_{IINP} is the transconductance of IINP (1µS typ), and R10 is the resistor connected between IINP and ground.

In the typical application circuit, duty cycle affects the accuracy of V_{IINP} (Figure 3). AC load current also affects accuracy (Figure 4).

Connect IINP pin to ground if it is not used.

LDO Regulator

LDO provides a 5.4V supply derived from DCIN and can deliver up to 15mA of current. The MOSFET drivers are powered by DLOV and BST, which must be connected to LDO as shown in Figure 1. LDO also supplies the 4.096V reference (REF) and most of the control circuitry. Bypass LDO with a 1µF capacitor.

DC-to-DC Converter

The MAX1772 employs a buck regulator with a bootstrapped NMOS high-side switch and a low-side NMOS synchronous rectifier.

DC-DC Controller

The control scheme is a constant off-time variable frequency, cycle-by-cycle current mode. The off-time is constant for a given BATT voltage. It varies with V_{BATT} operation; a maximum on-time of 10ms allows the controller to achieve >99% duty cycle with continuous conduction. Figure 5 shows the controller functional diagram.

MOSFET Drivers

The low-side driver output DLO swings from 0 to DLOV. DLOV is usually connected through a filter to LDO. The high-side driver output DHI is bootstrapped off LX and swings from V_{LX} to V_{BST}. When the low-side driver turns on, BST rises to one diode voltage below DLOV.

Filter DLOV with a resistor-capacitor (RC) circuit whose cutoff frequency is about 50kHz. The configuration in Figure 1 introduces a cutoff frequency of around 48kHz:

$$f = 1/2\pi RC = 1 / (2\pi \times 33\Omega \times 0.1\mu F) = 48kHz \quad (7)$$

Low-Cost, Multichemistry Battery-Charger Building Block

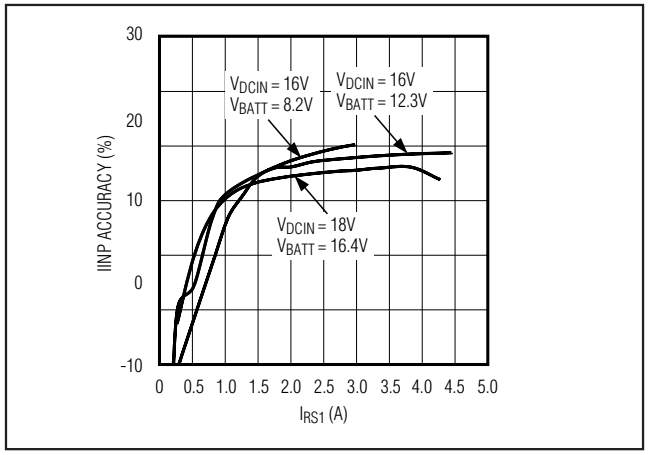


Figure 3. IINP Accuracy vs. V_{DCIN}/V_{BATT}

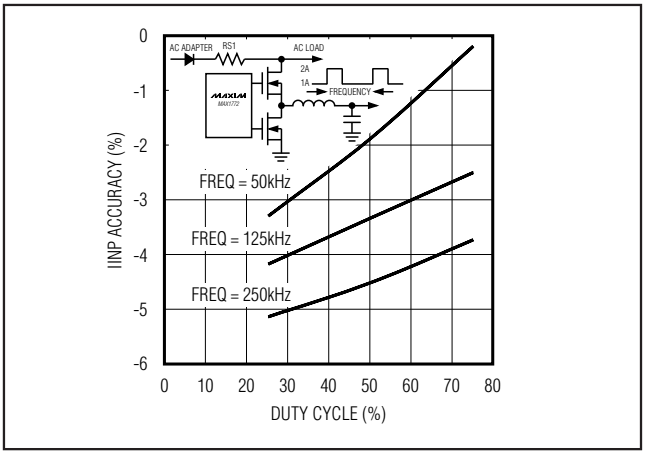


Figure 4. IINP Accuracy vs. AC Load Duty Cycle

Dropout Operation

The MAX1772 has 99.99% duty-cycle capability with a 10ms maximum on-time and 1µs off-time. This allows the charger to achieve dropout performance limited only by resistive losses in the DC-DC converter components (D1, N1, RS1, RS2) (Figure 1). The actual dropout voltage is limited to 100mV between CSSP and CSIN by the power-fail comparator.

Compensation

Each of the three regulation loops—the input current limit, the charging current limit, and charging voltage limit—can be compensated separately using the CCS, CCI, and CCV pins, respectively.

The charge-current-loop error-amp output is brought out at CCI. Likewise, the source current error-amp output is brought out at CCS; 0.01µF capacitors to ground at CCI and CCS compensate the current loops in most charger designs. Raising the value of these capacitors reduces the bandwidth of these loops.

The voltage-regulating-loop error-amp output is brought out at CCV. Compensate this loop by connecting a series RC network from CCV to GND. Recommended values are 1kΩ and 0.1µF. The zero set by the series RC increases midfrequency gain to provide phase compensation. The pole at CCV is set by the capacitor and the voltage error-amp output impedance at low frequencies to integrate the DC error.

Component Selection

Table 2 lists the recommended components and refers to the circuit of Figure 1. The following sections describe how to select these components.

MOSFETs and Schottky Diodes

Schottky diode D1 provides power to the load when the AC adapter is inserted. This diode must be able to deliver the maximum current as set by RS1.

The n-channel MOSFETs (N1, N2) are the switching devices for the buck controller. High-side switch N1 should have a current rating of at least 8A and have an on-resistance ($R_{DS(ON)}$) of 50mΩ or less. The driver for N1 is powered by BST; its current should be less than 10mA. Select a MOSFET with a low total gate charge (Q_{GATE}) and determine the required drive current by $I_{GATE} = Q_{GATE} \times f$ (where f is the DC-DC converter's 400kHz maximum switching frequency).

The low-side switch (N2) should also have a current rating of at least 8A, have an $R_{DS(ON)}$ of 100mΩ or less, and a total gate charge less than 10nC. N2 is used to provide the starting charge to the BST capacitor (C15). During normal operation, the current is carried by Schottky diode D2. Choose a Schottky diode capable of carrying the maximum charging current.

D3 is a signal-level diode, such as the 1N4148. This diode provides the supply current to the high-side MOSFET driver.

Inductor Selection

Inductor L1 provides power to the battery while it is being charged. It must have a saturation current of at least 4A plus 1/2 of the current ripple (ΔI_L):

$$I_{SAT} = 4A + (1/2)\,\Delta I_L \qquad (8)$$

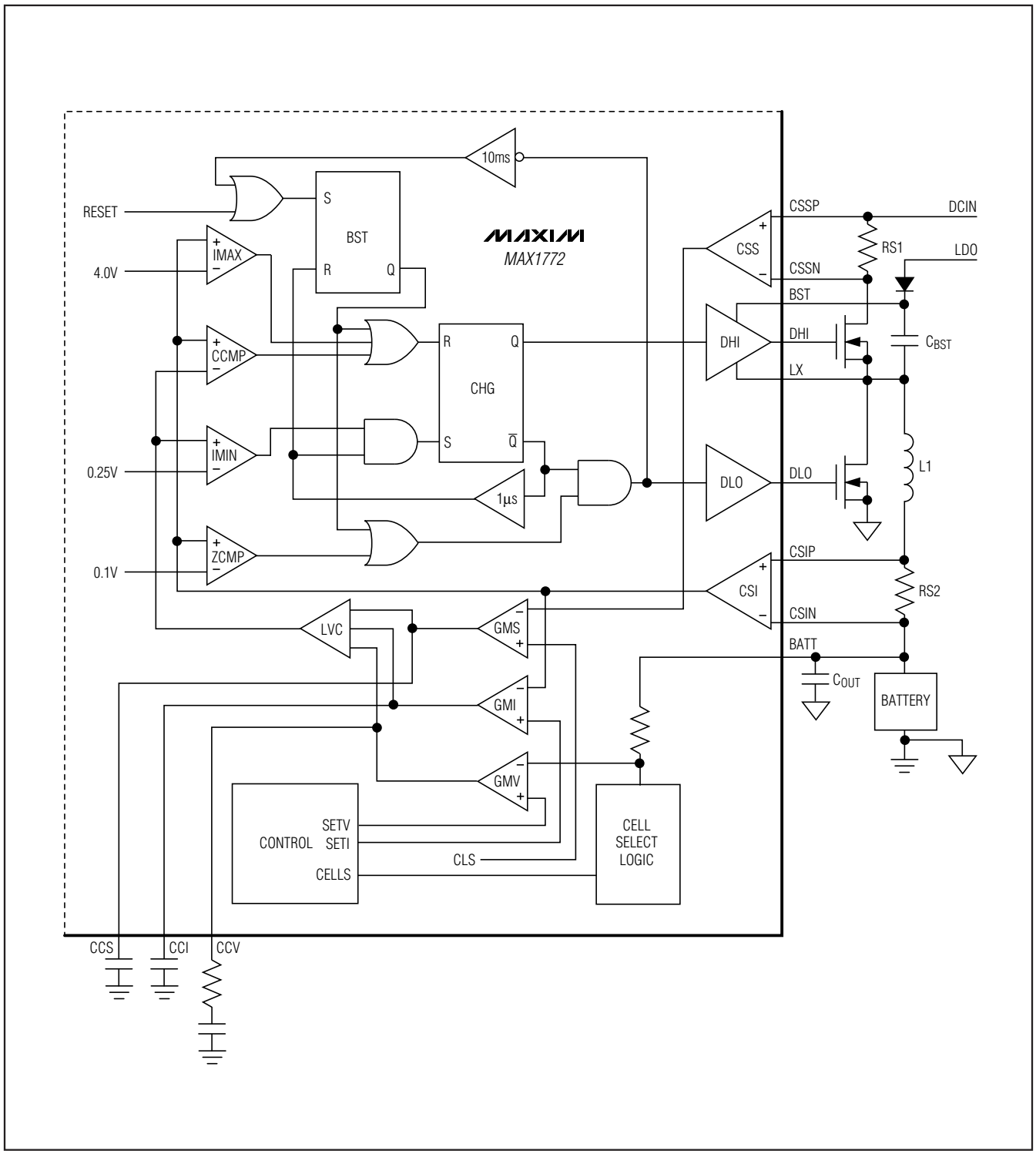


Figure 5. DC-to-DC Converter Functional Diagram

Low-Cost, Multichemistry Battery-Charger Building Block

The controller determines the constant off-time period, which is dependent on BATT voltage. This makes the ripple current independent of input and battery voltage, and it should be kept to less than 1A. Calculate ΔI_L with the following equation:

$$\Delta I_L = \frac{21V\mu s}{L(\mu H)} \quad (9)$$

Higher inductor values decrease the ripple current. Smaller inductor values require high saturation current capabilities and degrade efficiency. Typically, a 22µH inductor is ideal for all operating conditions.

Current-Sense Input Filtering

In normal circuit operation with typical components, the current-sense signals can have high-frequency transients that exceed 0.5V due to large current changes and parasitic component inductance. To achieve proper battery and input current compliance, the current-sense input signals should be filtered to remove large common-mode transients. The input current-limit sensing circuitry is the most sensitive case due to large current steps in the input filter capacitors (C6, C7) in Figure 1. Use 0.47µF ceramic capacitors from CSSP and CSSN to ground. Smaller 0.1µF ceramic capacitors (C18, C19) can be used on the CSIP and CSIN inputs to ground since the current into the battery is continuous. Place these capacitors next to the single-point ground directly under the MAX1772.

Layout and Bypassing

Bypass DCIN with a 1µF to ground (Figure 1). D4 protects the MAX1772 when the DC power source input is reversed. A signal diode for D4 is adequate because DCIN only powers the LDO and the internal reference. Bypass LDO, BST, DLOV, and other pins as shown in Figure 1.

Good PCB layout is required to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions—preferably, a pencil sketch showing the placement of the power switching components and high current routing. Refer to the PCB layout in the MAX1772 evaluation kit for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high current connections, the bottom layer for quiet connections (REF, CCV, CCI, CCS, DCIN, and GND), and the inner layers for an uninterrupted ground plane.

Use the following step-by-step guide:

1) Place the high power connections first, with their grounds adjacent:
   - Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
   - Minimize ground trace lengths in the high current paths.
   - Minimize other trace lengths in the high current paths.
   - Use >5mm wide traces.
   - Connect C1 and C2 to high-side MOSFET (10mm max length).
   - LX node (MOSFETs, rectifier cathode, inductor (15mm max length)).

   Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias.

   The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PCB layout problems.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF capacitor). **Important: the IC must be no further than 10mm from the current-sense resistors.**

   Keep the gate drive traces (DHI, DLO, and BST) shorter than 20mm, and route them away from the current-sense lines and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.

3) Use a single-point star ground placed directly below the part. Connect the input ground trace, power ground (subground plane), and normal ground to this node.

Table 2. Component List

DESIGNATION	DESCRIPTION
C1, C2, C3, C4	22µF, 35V low-ESR tantalum capacitors AVX TPSE226M035R0300 or Sprague 593D226X0035E2W
C5	1µF, 50V ceramic capacitor (1210) Murata GRM42-2X7R105K050
C6, C7	0.47µF, 25V ceramic capacitors (1210) Murata GRM42-2X7R474K050
C9, C10	0.01µF ceramic capacitors (0805)
C12, C13	1µF, 10V ceramic capacitors (0805) Taiyo Yuden LMK212BJ105MG
C11, C14, C15, C16, C18, C19, C20	0.1µF, 50V ceramic capacitors (0805) Taiyo Yuden UMK212BJ104MG or Murata GRM40-034X7R104M050
D1	Schottky diode (DPAK) STM-Microelectronics STPS8L30B or ON Semiconductor MBRD630CT or Toshiba U5FWK2C42
D2	30V, 3A Schottky diode Nihon EC31QS03L
D3, D4	100mA Schottky diodes (SOT23) Central Semiconductor CMPSH-3 or Hitachi HRB0103A
L1	22µH power inductor Sumida CDRH127-220
N1	n-channel MOSFET International Rectifier IRF7805 or Fairchild FDS6680
N2	n-channel MOSFET Fairchild FDS6612A
RS1	0.04Ω ±1%, 1W resistor Dale WSL-2512-R040-F or IRC LR2512-01-R040-F
RS2	0.05Ω ±1%, 1W resistor Dale WSL-2512-R050-F or IRC LR2512-01-R050-F
R5	1kΩ ±5% resistor (0805)
R6	59.0kΩ ±1% resistor (0805)
R7	19.6kΩ ±1% resistor (0805)
R8	1MΩ ±5% resistor (0805)
R9	15.4kΩ ±1% resistor (0805)
R10	12.4kΩ ±1% resistor (0805)
R11, R12	1Ω ±5% resistors (0805)
R13	33Ω ±5% resistor (1206)
R14, R15	4.7Ω ±5% resistors (1206)
R19	29.4kΩ ±1% resistor (0805)
R20, R21, R22	10kΩ ±1% resistors (0805)

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 QSOP	E28-1	21-0055

Low-Cost, Multichemistry Battery-Charger Building Block

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/07	Initial release	—
4	2/09	Minor edits.	14

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX1772EEI+ MAX1772EEI+T