# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +36V
PGND to GND.....±0.3V
$V_L$ to GND .....-0.3V to +6V
BST3, BST5 to GND .....-0.3V to +36V
CSH3, CSH5 to GND.....-0.3V to +6V
FB3 to GND .....-0.3V to (CSL3 + 0.3V)
FB5 to GND .....-0.3V to (CSL5 +0.3V)
LX3 to BST3.....-6V to +0.3V
LX5 to BST5.....-6V to +0.3V
REF, SYNC, SEQ, STEER, $\overline{SKIP}$,
TIME/ON5, SECFB, $\overline{RESET}$ to GND .....-0.3V to ($V_L$ + 0.3V)
$V_{DD}$ to GND.....-0.3V to +20V
RUN/ON3, $\overline{SHDN}$ to GND.....-0.3V to (V+ + 0.3V)
12OUT to GND .....-0.3V to ($V_{DD}$ + 0.3V)
DL3, DL5 to PGND.....-0.3V to ($V_L$ + 0.3V)
DH3 to LX3 .....-0.3V to (BST3 + 0.3V)
DH5 to LX5 .....-0.3V to (BST5 + 0.3V)
$V_L$, REF Short to GND .....Momentary
12OUT Short to GND.....Continuous
REF Current.....+5mA to -1mA
$V_L$ Current.....+50mA
12OUT Current .....+200mA
$V_{DD}$ Shunt Current.....+15mA
Continuous Power Dissipation ($T_A$ = +70°C)
28-Pin SSOP (derate 9.52mW/°C above +70°C) .....762mW
32-Pin Thin QFN (derate 21.3mW/°C above +70°C) ..1702mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(V+ = 15V, both PWMs on, SYNC = $V_L$, $V_L$ load = 0, REF load = 0, $\overline{SKIP}$ = 0, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **MAIN SMPS CONTROLLERS** | | | | | |
| Input Voltage Range | | 4.2 | | 30.0 | V |
| 3V Output Voltage in Adjustable Mode | V+ = 4.2V to 30V, CSH3 - CSL3 = 0, CSL3 tied to FB3 | 2.42 | 2.5 | 2.58 | V |
| 3V Output Voltage in Fixed Mode | V+ = 4.2V to 30V, 0 < CSH3 - CSL3 < 80mV, FB3 = 0 | 3.20 | 3.39 | 3.47 | V |
| 5V Output Voltage in Adjustable Mode | V+ = 4.2V to 30V, CSH5 - CSL5 = 0, CSL5 tied to FB5 | 2.42 | 2.5 | 2.58 | V |
| 5V Output Voltage in Fixed Mode | V+ = 5.3V to 30V, 0 < CSH5 - CSL5 < 80mV, FB5 = 0 | 4.85 | 5.13 | 5.25 | V |
| Output Voltage Adjust Range | Either SMPS | REF | | 5.5 | V |
| Adjustable-Mode Threshold Voltage | Dual-mode comparator | 0.5 | | 1.1 | V |
| Load Regulation | Either SMPS, 0 < CSH_ - CSL_ < 80mV | | -2 | | % |
| Line Regulation | Either SMPS, 5.2V < V+ < 30V | | 0.03 | | %/V |
| Current-Limit Threshold | CSH3 - CSL3 or CSH5 - CSL5 | 80 | 100 | 120 | mV |
| | $\overline{SKIP}$ = $V_L$ or $V_{DD}$ < 13V or SECFB < 2.44V | -50 | -100 | -150 | |
| Idle Mode Threshold | $\overline{SKIP}$ = 0, not tested | 10 | 25 | 40 | mV |
| Soft-Start Ramp Time | From enable to 95% full current limit with respect to $f_{OSC}$ (Note 1) | | 512 | | clks |
| Oscillator Frequency | SYNC = $V_L$ | 450 | 500 | 550 | kHz |
| | SYNC = 0 | 283 | 333 | 383 | |

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, both PWMs on, SYNC = $V_L$, $V_L$ load = 0, REF load = 0, $\overline{SKIP}$ = 0, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Maximum Duty Factor | SYNC = $V_L$ | | 95 | 97 | | % |
| | SYNC = 0 (Note 2) | | 96.5 | 98 | | |
| SYNC Input High-Pulse Width | Not tested | | 200 | | | ns |
| SYNC Input Low-Pulse Width | Not tested | | 200 | | | ns |
| SYNC Rise/Fall Time | Not tested | | | | 200 | ns |
| SYNC Input Frequency Range | | | 400 | | 583 | kHz |
| Current-Sense Input Leakage Current | V+ = $V_L$ = 0, CSL3 = CSH3 = CSL5 = CSH5 = 5.5V | | | 0.01 | 10 | µA |
| **FLYBACK CONTROLLER** | | | | | | |
| $V_{DD}$ Regulation Threshold | Falling edge (Note 3) | | 13 | | 14 | V |
| SECFB Regulation Threshold | Falling edge (MAX1901/MAX1904) | | 2.44 | | 2.60 | V |
| DL Pulse Width | $V_{DD}$ < 13V or SECFB < 2.44V | | | 0.75 | | µs |
| $V_{DD}$ Shunt Threshold | Rising edge, hysteresis = 1% (Note 3) | | 18 | | 20 | V |
| $V_{DD}$ Shunt Sink Current | $V_{DD}$ = 20V (Note 3) | | 10 | | | mA |
| $V_{DD}$ Leakage Current | $V_{DD}$ = 5V, off mode (Notes 3, 4) | | | | 30 | µA |
| **12V LINEAR REGULATOR** (Note 3) | | | | | | |
| 12OUT Output Voltage | 13V < $V_{DD}$ < 18V, 0 < $I_{LOAD}$ < 120mA | | 11.65 | 12.10 | 12.50 | V |
| 12OUT Current Limit | 12OUT forced to 11V, $V_{DD}$ = 13V | | | 150 | | mA |
| Quiescent $V_{DD}$ Current | $V_{DD}$ = 18V, run mode, no 12OUT load | | | 50 | 100 | µA |
| **INTERNAL REGULATOR AND REFERENCE** | | | | | | |
| $V_L$ Output Voltage | $\overline{SHDN}$ = V+, RUN/ON3 = TIME/ON5 = 0, 5.4V < V+ < 30V, 0mA < $I_{LOAD}$ < 50mA | | 4.7 | | 5.1 | V |
| $V_L$ Undervoltage Lockout-Fault Threshold | Falling edge, hysteresis = 1% | | 3.5 | 3.6 | 3.7 | V |
| $V_L$ Switchover Threshold | Rising edge of CSL5, hysteresis = 1% | | 4.2 | 4.5 | 4.7 | V |
| REF Output Voltage | No external load (Note 5) | | 2.45 | 2.5 | 2.55 | V |
| REF Load Regulation | 0 < $I_{LOAD}$ < 50µA | | | | 12.5 | mV |
| | 0 < $I_{LOAD}$ < 5mA | | | | 100.0 | |
| REF Sink Current | | | 10 | | | µA |
| REF Fault-Lockout Voltage | Falling edge | | 1.8 | | 2.4 | V |
| V+ Operating Supply Current | $V_L$ switched over to CSL5, 5V SMPS on | | | 5 | 50 | µA |
| V+ Standby Supply Current | V+ = 5.5V to 30V, both SMPSs off, includes current into $\overline{SHDN}$ | | | 30 | 60 | µA |
| V+ Standby Supply Current in Dropout | V+ = 4.2V to 5.5V, both SMPSs off, includes current into $\overline{SHDN}$ | | | 50 | 200 | µA |
| V+ Shutdown Supply Current | V+ = 4.0V to 30V, $\overline{SHDN}$ = 0 | | | 4 | 10 | µA |
| Quiescent Power Consumption | Both SMPSs enabled, FB3 = FB5 = 0, CSL3 = CSH3 = 3.5V, CSL5 = CSH5 = 5.3V | (Note 3) | | 2.5 | 4 | mW |
| | | MAX1901/MAX1904 | | 1.5 | 4 | |

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, both PWMs on, SYNC = $V_L$, $V_L$ load = 0, REF load = 0, $\overline{SKIP}$ = 0, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **FAULT DETECTION** (MAX1901/MAX1902) | | | | | | |
| Overvoltage Trip Threshold | With respect to unloaded output voltage | | 4 | 7 | 10 | % |
| Overvoltage Fault Propagation Delay | CSL_ driven 2% above overvoltage trip threshold | | | 1.5 | | µs |
| Output Undervoltage Threshold | With respect to unloaded output voltage | | 60 | 70 | 80 | % |
| Output Undervoltage Lockout Time | From each SMPS enabled, with respect to $f_{OSC}$ | | 5,000 | 6,144 | 7,000 | clks |
| Thermal-Shutdown Threshold | Typical hysteresis = 10°C | | | 150 | | °C |
| **$\overline{RESET}$** | | | | | | |
| $\overline{RESET}$ Trip Threshold | With respect to unloaded output voltage, falling edge; typical hysteresis = 1% | | -7 | -5.5 | -4 | % |
| $\overline{RESET}$ Propagation Delay | Falling edge, CSL_ driven 2% below $\overline{RESET}$ trip threshold | | | 1.5 | | µs |
| $\overline{RESET}$ Delay Time | With respect to $f_{OSC}$ | | 27,000 | 32,000 | 37,000 | clks |
| **INPUTS AND OUTPUTS** | | | | | | |
| Feedback-Input Leakage Current | FB3, FB5; SECFB = 2.6V | | | 1 | 50 | nA |
| Logic Input-Low Voltage | RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = REF), $\overline{SHDN}$, STEER, SYNC | | | | 0.6 | V |
| Logic Input-High Voltage | RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = REF), $\overline{SHDN}$, STEER, SYNC | | 2.4 | | | V |
| Input Leakage Current | RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = REF), $\overline{SHDN}$, STEER, SYNC, SEQ; $V_{PIN}$ = 0V or 3.3V | | | | ±1 | µA |
| Logic Output-Low Voltage | $\overline{RESET}$, $I_{SINK}$ = 4mA | | | | 0.4 | V |
| Logic Output-High Current | $\overline{RESET}$ = 3.5V | | 1 | | | mA |
| TIME/ON5 Input Trip Level | SEQ = 0 or $V_L$ | | 2.4 | | 2.6 | V |
| TIME/ON5 Source Current | TIME/ON5 = 0, SEQ = 0 or $V_L$ | | 2.5 | 3 | 3.5 | µA |
| TIME/ON5 On-Resistance | TIME/ON5; RUN/ON3 = 0, SEQ = 0 or $V_L$ | | | 15 | 80 | Ω |
| Gate-Driver Sink/Source Current | DL3, DH3, DL5, DH5; forced to 2V | | | 1 | | A |
| Gate-Driver On-Resistance | High or low (Note 6) | SSOP package | | 1.5 | 7 | Ω |
| | | QFN package | | 1.5 | 8 | |

## ELECTRICAL CHARACTERISTICS

(V+ = 15V, both PWMs on, SYNC = $V_L$, $V_L$ load = 0, REF load = 0, $\overline{SKIP}$ = 0, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 7)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **MAIN SMPS CONTROLLERS** | | | | | |
| Input Voltage Range | | 4.2 | | 30.0 | V |
| 3V Output Voltage in Adjustable Mode | V+ = 4.2V to 30V, CSH3 - CSL3 = 0, CSL3 tied to FB3 | 2.42 | | 2.58 | V |
| 3V Output Voltage in Fixed Mode | V+ = 4.2V to 30V, 0 < CSH3 - CSL3 < 80mV, FB3 = 0 | 3.20 | | 3.47 | V |
| 5V Output Voltage in Adjustable Mode | V+ = 4.2V to 30V, CSH5 - CSL5 = 0, CSL5 tied to FB5 | 2.42 | | 2.58 | V |
| 5V Output Voltage in Fixed Mode | V+ = 5.3V to 30V, 0 < CSH5 - CSL5 < 80mV, FB5 = 0 | 4.85 | | 5.25 | V |
| Output Voltage Adjust Range | Either SMPS | REF | | 5.5 | V |
| Adjustable-Mode Threshold Voltage | Dual-mode comparator | 0.5 | | 1.1 | V |
| Current-Limit Threshold | CSH3 - CSL3 or CSH5 - CSL5 | 80 | | 120 | mV |
| | $\overline{SKIP}$ = $V_L$ or $V_{DD}$ < 13V or SECFB < 2.44V | -50 | | -150 | |
| Oscillator Frequency | SYNC = $V_L$ | 450 | | 550 | kHz |
| | SYNC = 0 | 283 | | 383 | |
| Maximum Duty Factor | SYNC = $V_L$ | 95 | | | % |
| | SYNC = 0 (Note 2) | 97 | | | |
| SYNC Input Frequency Range | | 400 | | 583 | kHz |
| **FLYBACK CONTROLLER** | | | | | |
| $V_{DD}$ Regulation Threshold | Falling edge (Note 3) | 13 | | 14 | V |
| SECFB Regulation Threshold | Falling edge (MAX1901/MAX1904) | 2.44 | | 2.60 | V |
| $V_{DD}$ Shunt Threshold | Rising edge, hysteresis = 1% (Note 3) | 18 | | 20 | V |
| $V_{DD}$ Shunt Sink Current | $V_{DD}$ = 20V (Note 3) | 10 | | | mA |
| **12V LINEAR REGULATOR** (Note 3) | | | | | |
| 12OUT Output Voltage | 13V < $V_{DD}$ < 18V, 0mA < $I_{LOAD}$ < 100mA | 11.65 | | 12.50 | V |
| Quiescent $V_{DD}$ Current | $V_{DD}$ = 18V, run mode, no 12OUT load | | | 100 | µA |
| **INTERNAL REGULATOR AND REFERENCE** | | | | | |
| $V_L$ Output Voltage | $\overline{SHDN}$ = V+, RUN/ON3 = TIME/ON5 = 0, 5.4V < V+ < 30V, 0 < $I_{LOAD}$ < 50mA | 4.7 | | 5.1 | V |
| $V_L$ Undervoltage Lockout-Fault Threshold | Falling edge, hysteresis = 1% | 3.5 | | 3.7 | V |
| $V_L$ Switchover Threshold | Rising edge of CSL5, hysteresis = 1% | 4.2 | | 4.7 | V |
| REF Output Voltage | No external load (Note 5) | 2.45 | | 2.55 | V |
| REF Load Regulation | 0 < $I_{LOAD}$ < 50µA | | | 12.5 | mV |
| | 0 < $I_{LOAD}$ < 5mA | | | 100.0 | |
| REF Sink Current | | 10 | | | µA |
| REF Fault Lockout Voltage | Falling edge | 1.8 | | 2.4 | V |
| V+ Operating Supply Current | $V_L$ switched over to CSL5, 5V SMPS on | | | 50 | µA |

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, both PWMs on, SYNC = $V_L$, $V_L$ load = 0, REF load = 0, $\overline{SKIP}$ = 0, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 7)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| V+ Standby Supply Current | V+ = 5.5V to 30V, both SMPSs off, includes current into $\overline{SHDN}$ | | | | 60 | µA |
| V+ Standby Supply Current in Dropout | V+ = 4.2V to 5.5V, both SMPSs off, includes current into $\overline{SHDN}$ | | | | 200 | µA |
| V+ Shutdown Supply Current | V+ = 4.0V to 30V, $\overline{SHDN}$ = 0 | | | | 10 | µA |
| Quiescent Power Consumption | Both SMPSs enabled, FB3 = FB5 = 0, CSL3 = CSH3 = 3.5V, CSL5 = CSH5 = 5.3V | (Note 3) | | | 4 | mW |
| | | MAX1901/MAX1904 | | | 4 | |
| **FAULT DETECTION** (MAX1901/MAX1902) | | | | | | |
| Overvoltage Trip Threshold | With respect to unloaded output voltage | | 4 | | 10 | % |
| Output Undervoltage Threshold | With respect to unloaded output voltage | | 60 | | 80 | % |
| Output Undervoltage Lockout Time | From each SMPS enabled, with respect to $f_{OSC}$ | | 5,000 | | 7,000 | clks |
| **$\overline{RESET}$** | | | | | | |
| $\overline{RESET}$ Trip Threshold | With respect to unloaded output voltage, falling edge; typical hysteresis = 1% | | -7 | | -4 | % |
| $\overline{RESET}$ Delay Time | With respect to $f_{OSC}$ | | 27,000 | | 37,000 | clks |
| **INPUTS AND OUTPUTS** | | | | | | |
| Feedback-Input Leakage Current | FB3, FB5; SECFB = 2.6V | | | | 50 | nA |
| Logic Input-Low Voltage | RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = REF), $\overline{SHDN}$, STEER, SYNC | | | | 0.6 | V |
| Logic Input-High Voltage | RUN/ON3, $\overline{SKIP}$, TIME/ON5 (SEQ = REF), $\overline{SHDN}$, STEER, SYNC | | 2.4 | | | V |
| Logic Output-Low Voltage | $\overline{RESET}$, $I_{SINK}$ = 4mA | | | | 0.4 | V |
| Logic Output-High Current | $\overline{RESET}$ = 3.5V | | 1 | | | mA |
| TIME/ON5 Input Trip Level | SEQ = 0 or $V_L$ | | 2.4 | | 2.6 | V |
| TIME/ON5 Source Current | TIME/ON5 = 0, SEQ = 0 or $V_L$ | | 2.5 | | 3.5 | µA |
| TIME/ON5 On-Resistance | TIME/ON5; RUN/ON3 = 0, SEQ = 0 or $V_L$ | | | | 80 | Ω |
| Gate-Driver On-Resistance | High or low (Note 6) | SSOP package | | | 7 | Ω |
| | | QFN package | | | 8 | |

**Note 1:** Each of the four digital soft-start levels is tested for functionality; the steps are typically in 20mV increments.

**Note 2:** High duty-factor operation supports low input-to-output differential voltages, and is achieved at a lowered operating frequency (see the *Dropout Operation* section).

**Note 3:** MAX1902 only.

**Note 4:** Off mode for the 12V linear regulator occurs when the SMPS that has flyback feedback ($V_{DD}$) steered to it is disabled. In situations where the main outputs are being held up by external keep-alive supplies, turning off the 12OUT regulator prevents a leakage path from the output-referred flyback winding, through the rectifier, and into $V_{DD}$.

**Note 5:** Since the reference uses $V_L$ as its supply, the reference's V+ line-regulation error is insignificant.

**Note 6:** Production testing limitations due to package handing require relaxed maximum on-resistance specifications for the thin QFN package. The SSOP and thin QFN package contain the same die, and the thin QFN package imposes no additional resistance incircuit.

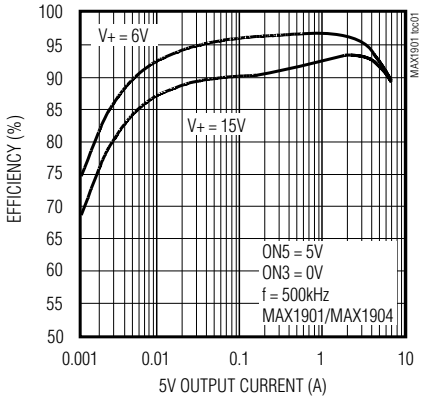
**Note 7:** Specifications from to 0°C to -40°C are guaranteed by design, not production tested.

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

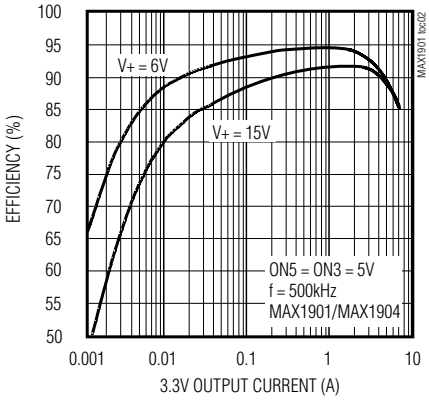
## Typical Operating Characteristics

(Circuit of Figure 1, Table 1, 6A/500kHz components, $T_A$ = +25°C, unless otherwise noted.)

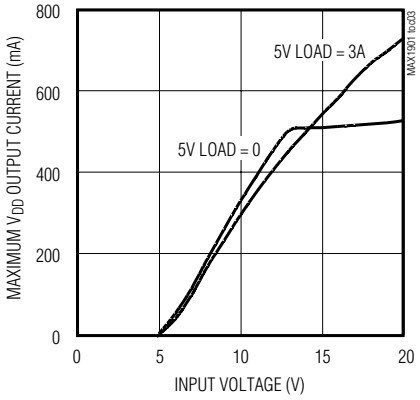
**EFFICIENCY vs. 5V OUTPUT CURRENT**



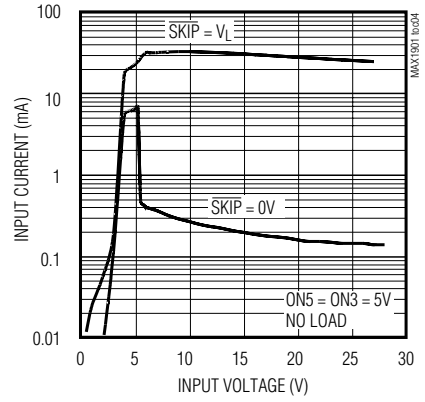

**EFFICIENCY vs. 3.3V OUTPUT CURRENT**



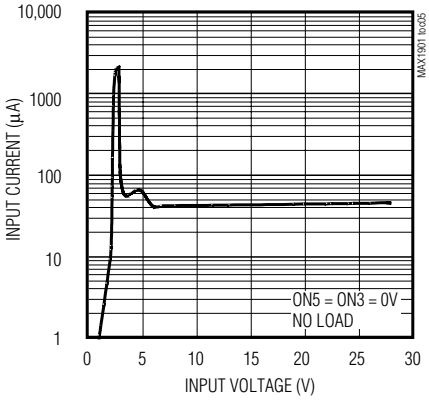

**MAXIMUM $V_{DD}$ OUTPUT CURRENT vs. INPUT VOLTAGE**



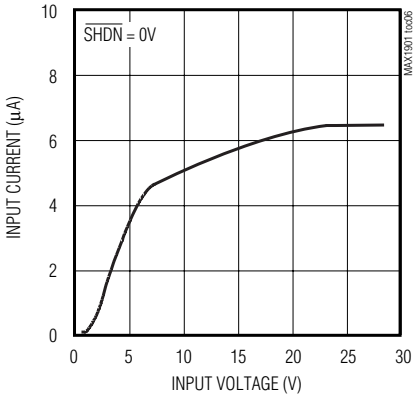

**NO LOAD INPUT CURRENT vs. INPUT VOLTAGE**



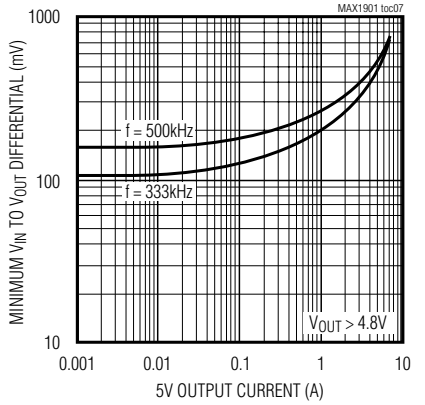

**V+ STANDBY INPUT CURRENT vs. INPUT VOLTAGE**



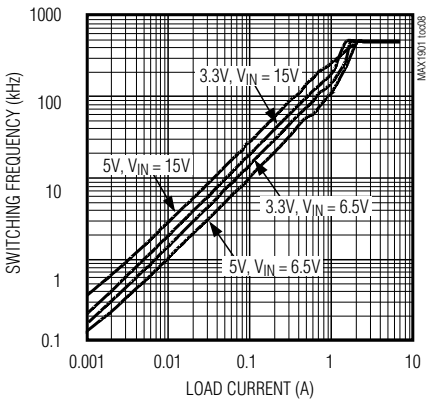

**SHUTDOWN INPUT CURRENT vs. INPUT VOLTAGE**



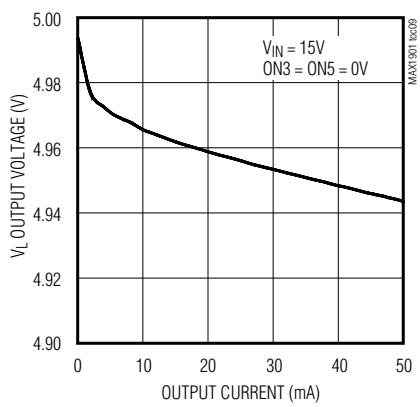

**MINIMUM $V_{IN}$ TO $V_{OUT}$ DIFFERENTIAL vs. 5V OUTPUT CURRENT**




**SWITCHING FREQUENCY vs. LOAD CURRENT**




**$V_L$ REGULATOR OUTPUT VOLTAGE vs. OUTPUT CURRENT**

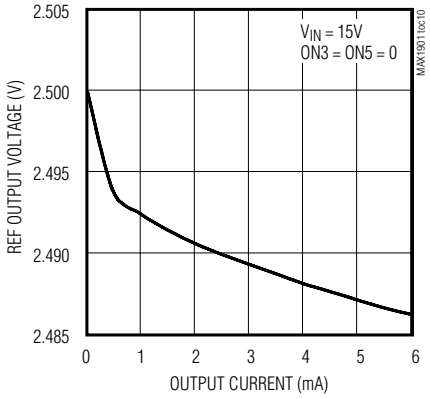


# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

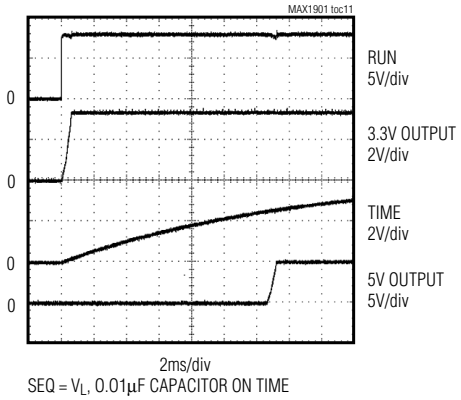
## Typical Operating Characteristics (continued)

(Circuit of Figure 1, Table 1, 6A/500kHz components, $T_A$ = +25°C, unless otherwise noted.)

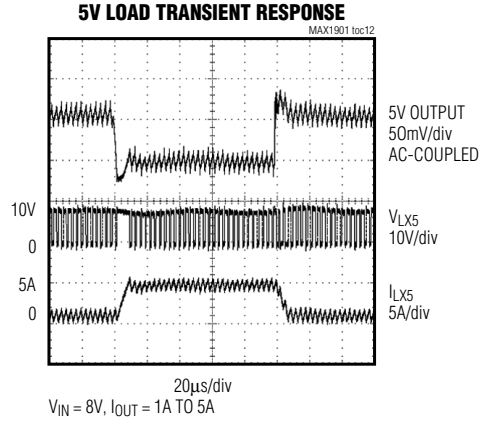
**REF OUTPUT VOLTAGE vs. OUTPUT CURRENT**



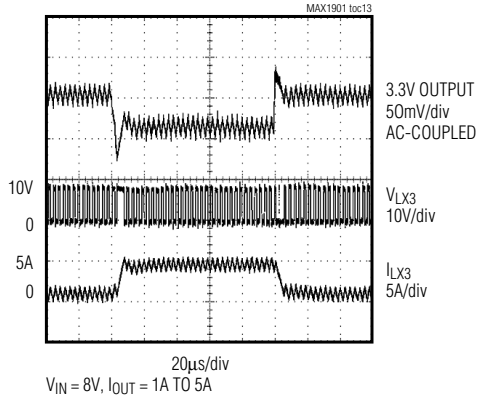

**STARTUP WAVEFORMS**




**5V LOAD TRANSIENT RESPONSE**




**3.3V LOAD TRANSIENT RESPONSE**



## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| SSOP | QFN | | |
| 1 | 29 | CSH3 | Current-Sense Input for the 3.3V SMPS. Current-limit level is 100mV referred to CSL3. |
| 2 | 30 | CSL3 | Current-Sense Input. Also serves as the feedback input in fixed-output mode. |
| 3 | 31 | FB3 | Feedback Input for the 3.3V SMPS. Regulates at FB3 = REF (approx. 2.5V) in adjustable mode. FB3 is a dual-mode input that also selects the 3.3V fixed output voltage setting when connected to GND. Connect FB3 to a resistor-divider for adjustable-output mode. |
| 4 | 1 | 12OUT (MAX1902) | 12V/120mA Linear-Regulator Output. Input supply comes from $V_{DD}$. Bypass 12OUT to GND with 1µF (min). |
| | | STEER (MAX1901/ MAX1904) | Logic-Control Input for Secondary Feedback. Selects the PWM that uses a transformer and secondary feedback signal (SECFB):<br>STEER = GND: 3.3V SMPS uses transformer<br>STEER = $V_L$: 5V SMPS uses transformer |
| 5 | 2 | $V_{DD}$ (MAX1902) | Supply Voltage Input for the 12OUT Linear Regulator. Also connects to an internal resistor-divider for secondary winding feedback and to an 18V overvoltage shunt regulator clamp. |
| | | SECFB (MAX1901/ MAX1904) | Secondary Winding Feedback Input. Normally connected to a resistor-divider from an auxiliary output. SECFB regulates at $V_{SECFB}$ = 2.5V (see the *Secondary Feedback Regulation Loop* section). Connect to $V_L$ if not used. |
| 6 | 3 | SYNC | Oscillator Synchronization and Frequency Select. Connect to $V_L$ for 500kHz operation; connect to GND for 333kHz operation. Can be driven at 400kHz to 583kHz for external synchronization. |
| 7 | 4 | TIME/ON5 | Dual-Purpose Timing Capacitor Pin and ON/$\overline{OFF}$ Control Input. See the *Power-Up Sequencing and ON/$\overline{OFF}$ Controls* section. |
| 8 | 5 | GND | Low-Noise Analog Ground and Feedback Reference Point |
| 9 | 7 | REF | 2.5V Reference Voltage Output. Bypass to GND with 1µF (min). |
| 10 | 8 | $\overline{SKIP}$ | Logic-control input that disables idle mode when high. Connect to GND for normal use. |
| 11 | 9 | $\overline{RESET}$ | Active-Low Timed Reset Output. $\overline{RESET}$ swings GND to $V_L$. Goes high after a fixed 32,000 clock-cycle delay following power-up. |
| 12 | 10 | FB5 | Feedback Input for the 5V SMPS. Regulates at FB5 = REF (approx. 2.5V) in adjustable mode. FB5 is a dual-mode input that also selects the 5V fixed output voltage setting when connected to GND. Connect FB5 to a resistor-divider for adjustable-output mode. |
| 13 | 11 | CSL5 | Current-Sense Input for the 5V SMPS. Also serves as the feedback input in fixed-output mode, and as the bootstrap supply input when the voltage on CSL5/$V_L$ is > 4.5V. |
| 14 | 12 | CSH5 | Current-Sense Input for the 5V SMPS. Current-limit level is 100mV referred to CSL5. |

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| QSOP | QFN | | |
| 15 | 13 | SEQ | Pin-strap input that selects the SMPS power-up sequence:<br>SEQ = GND: 5V before 3.3V, $\overline{RESET}$ output determined by both outputs<br>SEQ = REF: Separate ON3/ON5 controls, $\overline{RESET}$ output determined by 3.3V output<br>SEQ = $V_L$: 3.3V before 5V, $\overline{RESET}$ output determined by both outputs |
| 16 | 14 | DH5 | Gate-Drive Output for the 5V, High-Side N-Channel Switch. DH5 is a floating driver output that swings from LX5 to BST5, riding on the LX5 switching node voltage. |
| 17 | 15 | LX5 | Switching-Node (Inductor) Connection. Can swing 2V below ground without hazard. |
| 18 | 17 | BST5 | Boost Capacitor Connection for High-Side Gate Drive (0.1µF) |
| 19 | 18 | DL5 | Gate-Drive Output for the Low-Side Synchronous-Rectifier MOSFET. Swings 0 to $V_L$. |
| 20 | 19 | PGND | Power Ground |
| 21 | 20 | $V_L$ | 5V Internal Linear-Regulator Output. $V_L$ is also the supply-voltage rail for the chip. After the 5V SMPS output has reached 4.5V (typ), $V_L$ automatically switches to the output voltage through CSL5 for bootstrapping. Bypass to GND with 4.7µF. $V_L$ supplies up to 25mA for external loads. |
| 22 | 21 | V+ | Battery Voltage Input, 4.2V to 30V. Bypass V+ to PGND close to the IC with a 0.22µF capacitor. Connects to a linear regulator that powers $V_L$. |
| 23 | 22 | $\overline{SHDN}$ | Shutdown Control Input, Active Low. Logic threshold is set at approximately 1V. For automatic startup, connect $\overline{SHDN}$ to V+ through a 220kΩ resistor and bypass $\overline{SHDN}$ to GND with a 0.01µF capacitor. |
| 24 | 23 | DL3 | Gate-Drive Output for the Low-Side Synchronous-Rectifier MOSFET. Swings 0 to $V_L$. |
| 25 | 24 | BST3 | Boost Capacitor Connection for High-Side Gate Drive (0.1µF) |
| 26 | 26 | LX3 | Switching-Node (Inductor) Connection. Can swing 2V below ground without hazard. |
| 27 | 27 | DH3 | Gate-Drive Output for the 3.3V, High-Side N-Channel Switch. DH3 is a floating driver output that swings from LX3 to BST3, riding on the LX3 switching-node voltage. |
| 28 | 28 | RUN/ON3 | ON/$\overline{OFF}$ Control Input. See the *Power-Up Sequencing and ON/$\overline{OFF}$ Controls* section. |
| — | 6, 16, 25, 32 | N.C. | No Connection |

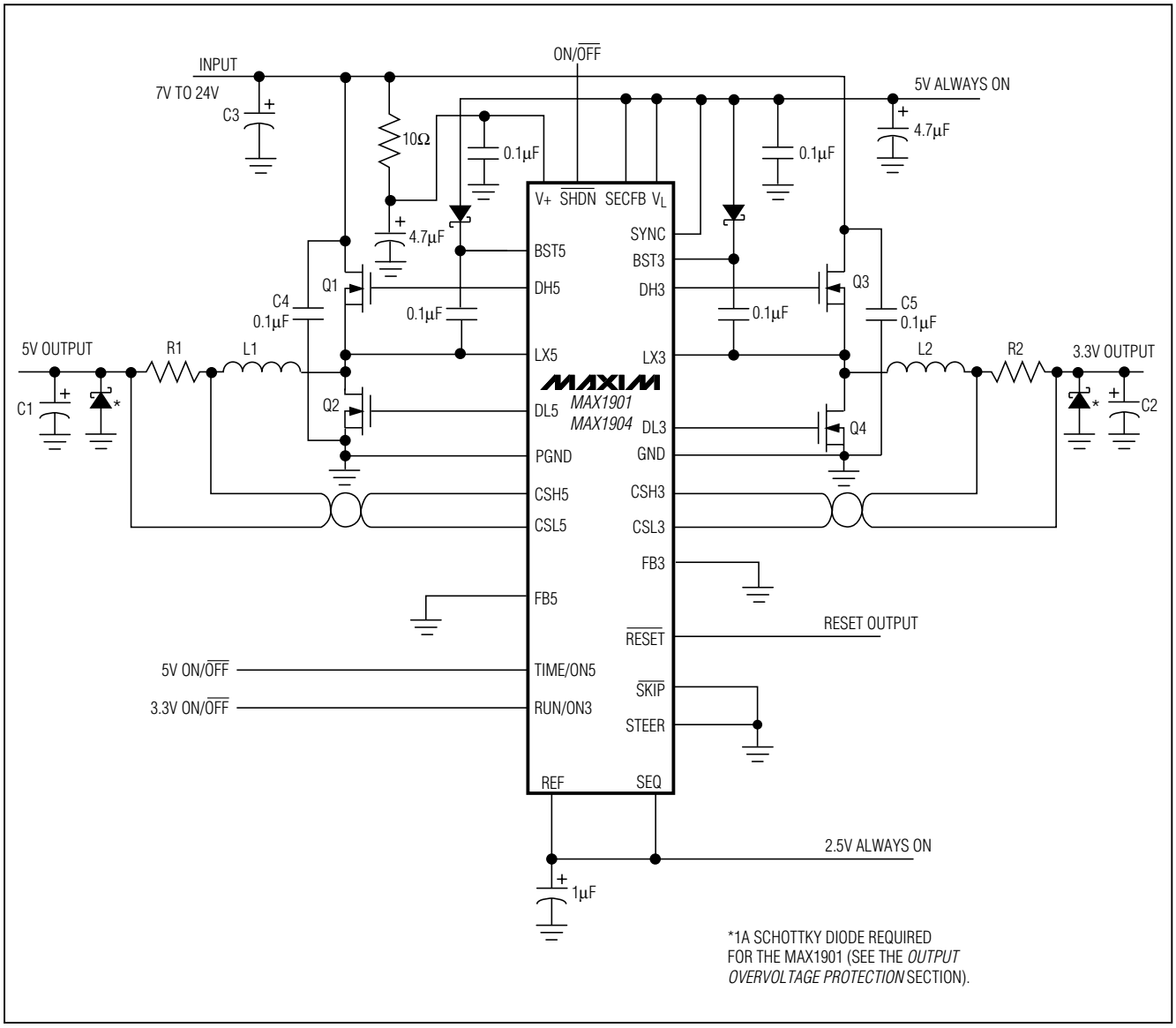



*Figure 1. Standard 3.3V/5V Application Circuit (MAX1901/MAX1904)*

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## Standard Application Circuit

The basic MAX1901/MAX1904 dual-output 3.3V/5V buck converter (Figure 1) is easily adapted to meet a wide range of applications with inputs up to 28V by substituting components from Table 1. These circuits represent a good set of tradeoffs between cost, size, and efficiency, while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current. Don't change the frequency of these circuits without first recalculating component values (particularly inductance value at maximum battery voltage). Adding a Schottky rectifier across each synchronous rectifier improves the efficiency of these circuits by approximately 1%, but this rectifier is otherwise not needed because the MOSFETs required for these circuits typically incorporate a high-speed silicon diode from drain to source. Use a Schottky rectifier rated at a DC current equal to at least one-third of the load current.

## Detailed Description

The MAX1901/MAX1902/MAX1904 are dual, BiCMOS, switch-mode power-supply controllers designed primarily for buck-topology regulators in battery-powered applications where high-efficiency and low-quiescent supply current are critical. Light-load efficiency is enhanced by automatic Idle-Mode operation, a variable-frequency pulse-skipping mode that reduces transition and gate-charge losses. Each step-down, power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET must exceed the battery voltage, and is provided by a flying-capacitor boost circuit that uses a 100nF capacitor connected to BST_.

**Table 1. Component Selection for Standard 3.3V/5V Application**

| COMPONENT | LOAD CURRENT | | |
|---|---|---|---|
| | 4A/333kHz | 4A/500kHz | 6A/500kHz |
| Input Range | 7V to 24V | 7V to 24V | 7V to 24V |
| Frequency | 333kHz | 500kHz | 500kHz |
| Q1, Q3 High-Side MOSFETs | 1/2 Fairchild FDS6982S or 1/2 International Rectifier IRF7901D1 | 1/2 Fairchild FDS6982S or 1/2 International Rectifier IRF7901D1 | Fairchild FDS6612A or International Rectifier IRF7807V |
| Q2, Q4 Low-Side MOSFETs with Integrated Schottky Diodes | 1/2 Fairchild FDS6982S or 1/2 International Rectifier IRF7901D1 | 1/2 Fairchild FDS6982S or 1/2 International Rectifier IRF7901D1 | Fairchild FDS6670S or International Rectifier IRF7807DV1 |
| C3 Input Capacitor | 3 × 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM | 3 × 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM | 4 × 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM |
| C1 Output Capacitor | 150µF, 6V POSCAP Sanyo 6TPC150M | 150µF, 6V POSCAP Sanyo 6TPC150M | 2 × 150µF, 6V POSCAP Sanyo 6TPC150M |
| C2 Output Capacitor | 2 × 150µF, 4V POSCAP Sanyo 4TPC150M | 2 × 150µF, 4V POSCAP Sanyo 4TPC150M | 2 × 220µF, 4V POSCAP Sanyo 4TPC220M |
| R1, R2 Resistors | 0.018Ω Dale WSL2512-R018-F | 0.018Ω Dale WSL2512-R018-F | 0.012Ω Dale WSL2512-R012-F |
| L1 Inductor | 10µH, 4.5A Ferrite Sumida CDRH124-100 | 7.0µH, 5.2A Ferrite Sumida CEI122-H-7R0 | 4.2µH, 6.9A Ferrite Sumida CEI122-H-4R2 |
| L2 Inductor | 7.0µH, 5.2A Ferrite Sumida CEI122-H-7R0 | 5.6µH, 5.2A Ferrite Sumida CEI122-H-5R6 | 4.2µH, 6.9A Ferrite Sumida CEI122-H-4R2 |

## Table 2. Component Suppliers

| MANUFACTURER | USA PHONE | FACTORY FAX |
|---|---|---|
| Dale-Vishay | 402-564-3131 | 402-563-6418 |
| Fairchild Semiconductor | 408-721-2181 | 408-721-1635 |
| International Rectifier | 310-322-3331 | 310-322-3332 |
| Sanyo | 619-661-6835 | 619-661-1055 |
| Sumida | 847-956-0666 | 847-956-0702 |
| Taiyo Yuden | 408-573-4150 | 408-573-4159 |

The MAX1901/MAX1902/MAX1904 contain ten major circuit blocks (Figure 2).

The two pulse-width-modulation (PWM) controllers each consist of a Dual Mode feedback network and multiplexer, a multi-input PWM comparator, high-side and low-side gate drivers, and logic. MAX1901/MAX1902 contain fault-protection circuits that monitor the main PWM outputs for undervoltage and overvoltage. A power-on sequence block controls the power-up timing of the main PWMs and determines whether one or both of the outputs are monitored for undervoltage faults. The MAX1902 includes a secondary feedback network and 12V linear regulator to generate a 12V output from a coupled-inductor flyback winding. The MAX1901/MAX1904 have a secondary feedback input (SECFB) instead, which allows a quasi-regulated, adjustable output, coupled-inductor flyback winding to be attached to either the 3.3V or the 5V main inductor. Bias generator blocks include the 5V IC internal rail ($V_L$) linear regulator, 2.5V precision reference, and automatic bootstrap switchover circuit. The PWMs share a common 333kHz/500kHz synchronizable oscillator.

These internal IC blocks aren't powered directly from the battery. Instead, the 5V $V_L$ linear regulator steps down the battery voltage to supply both $V_L$ and the gate drivers. The synchronous-switch gate drivers are directly powered from $V_L$, while the high-side switch gate drivers are indirectly powered from $V_L$ via an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the 5V linear regulator and powers the IC from the 5V PWM output voltage if the output is above 4.5V.

### PWM Controller Block

The two PWM controllers are nearly identical. The only differences are fixed output settings (3.3V vs. 5V), the VL/CSL5 bootstrap switch connected to the 5V PWM, and SECFB. The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums three signals: the output-voltage error signal with respect to the reference voltage, the current-sense signal, and the slope-compensation ramp (Figure 3). The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

When $\overline{SKIP}$ = low, Idle Mode circuitry automatically optimizes efficiency throughout the load current range. Idle Mode dramatically improves light-load efficiency by reducing the effective frequency, which reduces switching losses. It keeps the peak inductor current above 25% of the full current limit in an active cycle, allowing subsequent cycles to be skipped. Idle Mode transitions seamlessly to fixed-frequency PWM operation as load current increases.

With $\overline{SKIP}$ = high, the controller always operates in fixed-frequency PWM mode for lowest noise. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately $V_{OUT}$ / $V_{IN}$). As the high-side switch turns off, the synchronous rectifier latch sets; 60ns later, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

In PWM mode, the controller operates as a fixed-frequency current-mode controller where the duty ratio is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current value as a function of the output-voltage error signal. In continuous-conduction mode, the average inductor current is nearly the same as the peak current, so the circuit acts as a switch-mode transconductance amplifier. This pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing", a slope-compensation ramp is summed into the main PWM comparator to make the apparent duty factor less than 50%.

The MAX1901/MAX1902/MAX1904 use a relatively low loop gain, allowing the use of lower-cost output capacitors. The relative gains of the voltage-sense and current-sense inputs are weighted by the values of current sources that bias three differential input stages in the main PWM comparator (Figure 4). The relative gain of the voltage comparator to the current comparator is internally fixed at K = 2:1. The low loop gain results in the 2% typical load-regulation error. The low value of loop gain helps reduce output filter capacitor size and cost by shifting the unity-gain crossover frequency to a lower level.

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

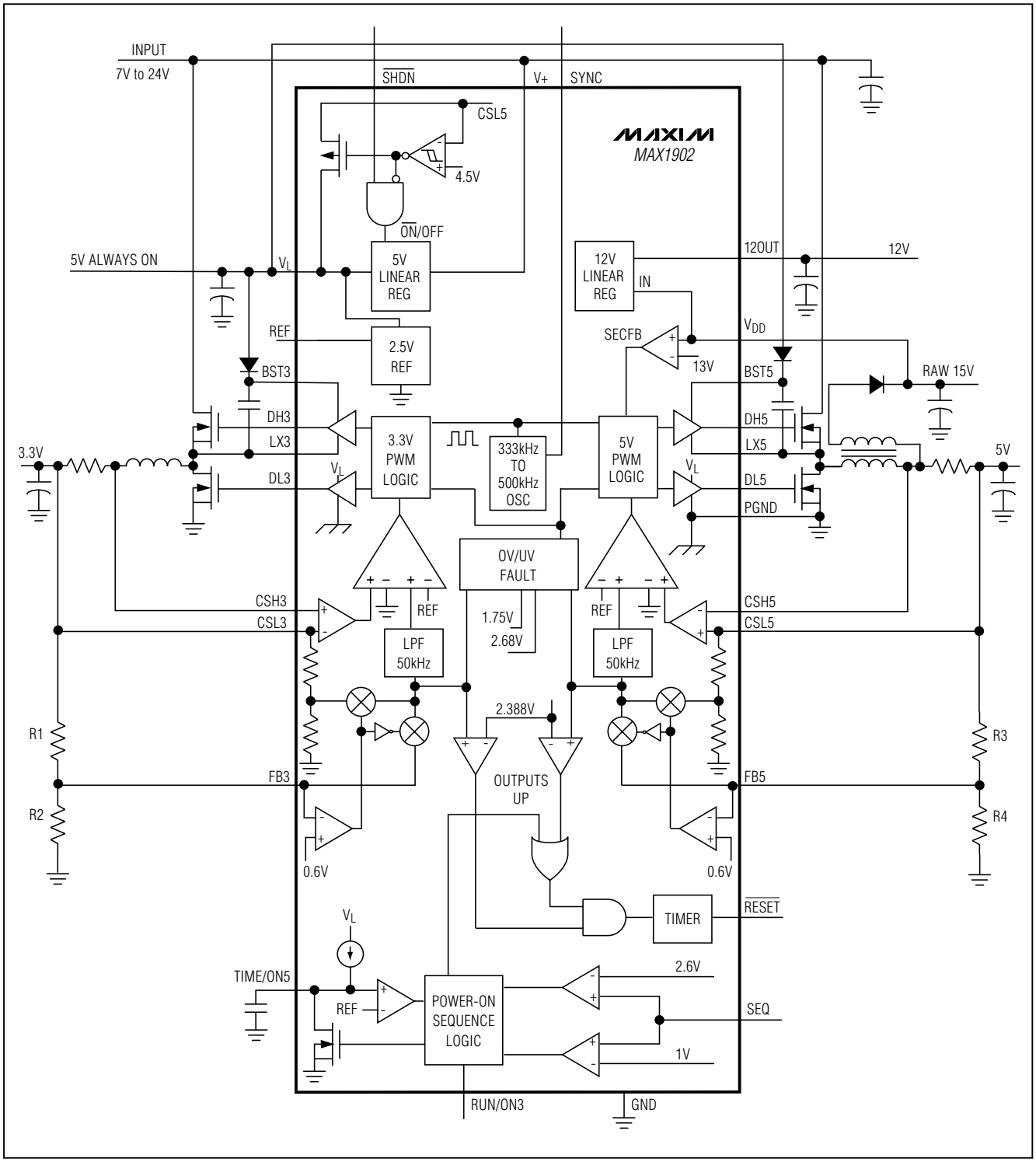



*Figure 2. MAX1902 Functional Diagram*

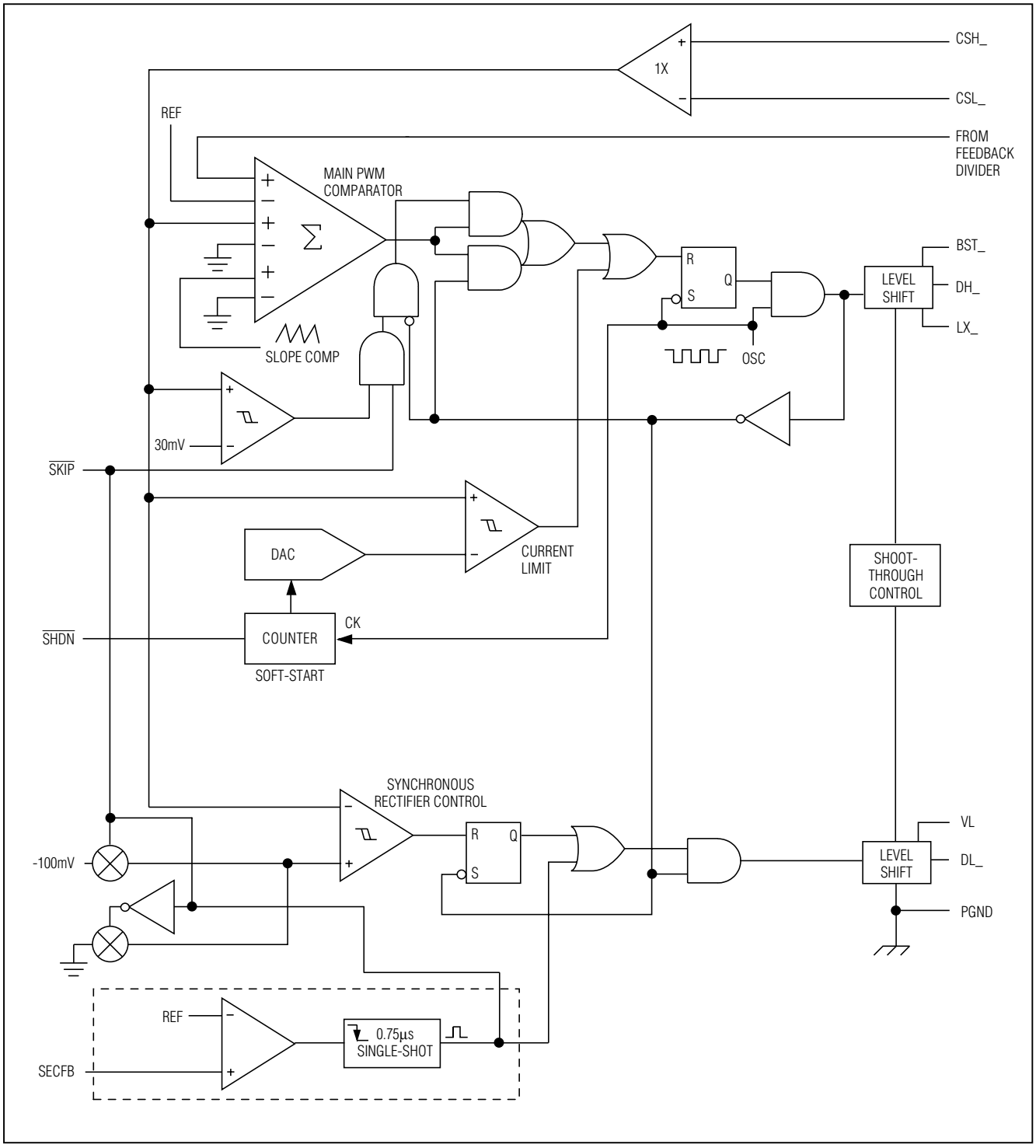



*Figure 3. PWM Controller Functional Block Diagram*

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## Table 3. SKIP PWM Table

| $\overline{SKIP}$ | LOAD CURRENT | MODE | DESCRIPTION |
|---|---|---|---|
| Low | Light | Idle | Pulse-skipping, supply current = 250µA at $V_{IN}$ =12V, discontinuous inductor |
| Low | Heavy | PWM | Constant-frequency PWM continuous-inductor current |
| High | Light | PWM | Constant-frequency PWM continuous-inductor current |
| High | Heavy | PWM | Constant-frequency PWM continuous-inductor current |

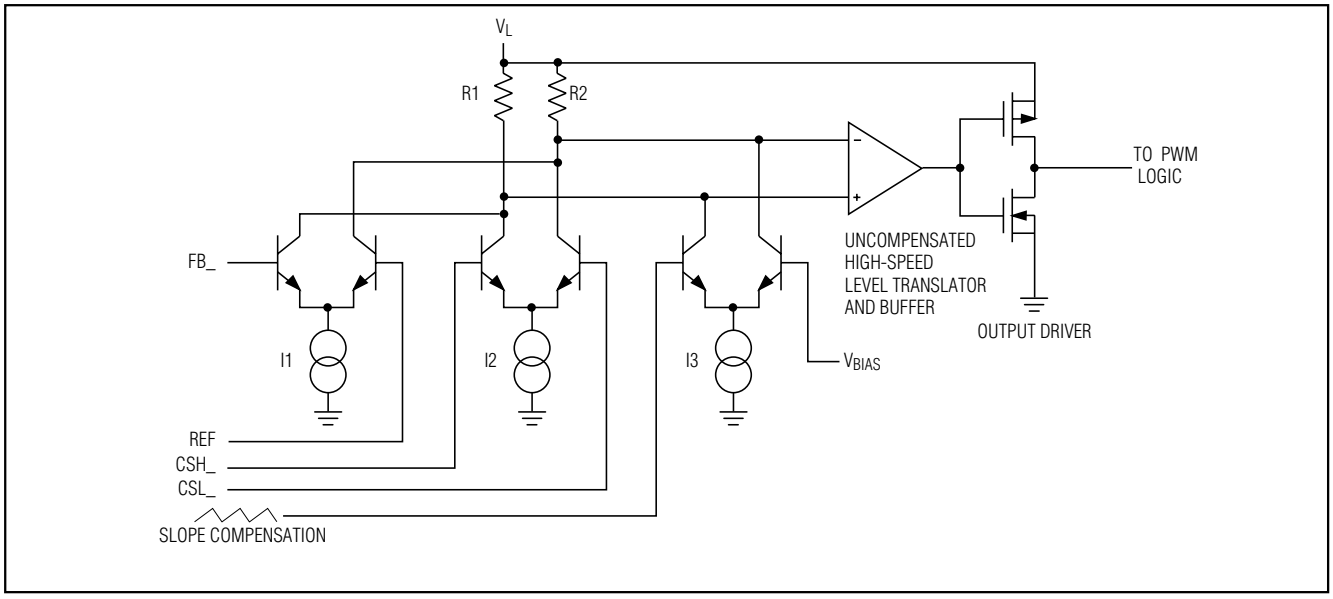



*Figure 4. Main PWM Comparator Block Diagram*

The output filter capacitors (Figure1, C1 and C2) set a dominant pole in the feedback loop that must roll off the loop gain to unity before encountering the zero introduced by the output capacitor's parasitic resistance (ESR) (see the *Design Procedure* section). A 50kHz pole-zero cancellation filter provides additional rolloff above the unity-gain crossover. This internal 50kHz low-pass compensation filter cancels the zero due to filter capacitor ESR. The 50kHz filter is included in the loop in both fixed-output and adjustable-output modes.

### Synchronous Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky catch diode with a low-resistance MOSFET switch. Also, the synchronous rectifier ensures proper startup of the boost gate-driver circuit.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot through"). In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero. The synchronous rectifier works under all operating conditions, including Idle Mode.

The SECFB signal further controls the synchronous switch timing in order to improve multiple-output cross-regulation (see the *Secondary Feedback Regulation Loop* section).

### Internal VL and REF Supplies

An internal regulator produces the 5V supply ($V_L$) that powers the PWM controller, logic, reference, and other blocks within the IC. This 5V low-dropout linear regulator supplies up to 25mA for external loads, with a reserve of 25mA for supplying gate-drive power. Bypass $V_L$ to GND with 4.7µF.

**Important:** Ensure that $V_L$ does not exceed 6V. Measure $V_L$ with the main output fully loaded. If it is pumped above 5.5V, either excessive boost-diode capacitance or excessive ripple at V+ is the probable cause. Use only small-signal diodes for the boost circuit (10mA to 100mA Schottky or 1N4148 are preferred), and bypass V+ to PGND with 4.7µF directly at the package pins.

The 2.5V reference (REF) is accurate to ±2% over temperature, making REF useful as a precision system reference. Bypass REF to GND with 1µF minimum. REF can supply up to 5mA for external loads. (Bypass REF with a minimum 1µF/mA reference load current.) However, if extremely accurate specifications for both the main output voltages and REF are essential, avoid loading REF more than 100µA. Loading REF reduces the main output voltage slightly, because of the reference load-regulation error.

When the 5V main output voltage is above 4.5V, an internal P-channel MOSFET switch connects CSL5 to VL, while simultaneously shutting down the VL linear regulator. This action bootstraps the IC, powering the internal circuitry from the output voltage, rather than through a linear regulator from the battery. Bootstrapping reduces power dissipation due to gate charge and quiescent losses by providing that power from a 90%-efficient switch-mode source, rather than from a much less efficient linear regulator.

### Boost High-Side Gate-Drive Supply (BST3 and BST5)

Gate-drive voltage for the high-side N-channel switches is generated by a flying-capacitor boost circuit (Figure 2). The capacitor between BST_ and LX_ is alternately charged from the VL supply and placed parallel to the high-side MOSFET's gate-source terminals. On startup, the synchronous rectifier (low-side MOSFET) forces LX_ to 0V and charges the boost capacitors to 5V. On the second half-cycle, the SMPS turns on the high-side MOSFET by closing an internal switch between BST_ and DH_. This provides the necessary enhancement voltage to turn on the high-side switch, an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing at the high-side MOSFET gate (DH3 and DH5) in discontinuous-conduction mode (light loads) is a natural operating condition. It is caused by residual energy in the tank circuit, formed by the inductor and stray capacitance at the switching node, LX. The gate-drive negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

### Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor (R1) must be sized for 80mV/ $I_{PEAK}$, where $I_{PEAK}$ is the required peak-inductor current to support the full load current, while components must be designed to withstand continuous-current stresses of 120mV/R1.

For breadboarding or for very-high-current applications, it may be useful to wire the current-sense inputs with a twisted pair, rather than PC traces. (This twisted pair need not be special; two pieces of wire-wrap wire twisted together is sufficient.) This reduces the possible noise picked up at CSH_ and CSL_, which can cause unstable switching and reduced output current. The CSL5 input also serves as the IC's bootstrap supply input. Whenever $V_{CSL5}$ > 4.5V, an internal switch connects CSL5 to $V_L$.

### Oscillator Frequency and Synchronization (SYNC)

The SYNC input controls the oscillator frequency. Low selects 333kHz; high selects 500kHz. SYNC can also be used to synchronize with an external 5V CMOS or TTL clock generator. SYNC has a guaranteed 400kHz to 583kHz capture range. A high-to-low transition on SYNC initiates a new cycle.

500kHz operation optimizes the application circuit for component size and cost. 333kHz operation provides increased efficiency, lower dropout, and improved load-transient response at low input-output voltage differences (see the *Low-Voltage Operation* section).

### Shutdown Mode

Holding $\overline{SHDN}$ low puts the IC into its 4µA shutdown mode. $\overline{SHDN}$ is logic input with a threshold of about 1V (the $V_{TH}$ of an internal N-channel MOSFET). For automatic startup, bypass $\overline{SHDN}$ to GND with a 0.01µF capacitor and connect it to V+ through a 220kΩ resistor.

### Power-Up Sequencing and $\overline{ON}/\overline{OFF}$ Controls

Startup is controlled by RUN/ON3 and TIME/ON5 in conjunction with SEQ. With SEQ tied to REF, the two control inputs act as separate $ON/\overline{OFF}$ controls for each supply. With SEQ tied to VL or GND, RUN/ON3 becomes the master $ON/\overline{OFF}$ control input and TIME/ON5 becomes a timing pin, with the delay between the two supplies determined by an external capacitor. The delay is approximately 800µs/nF. The 3.3V supply powers up first if SEQ is tied to VL, and the 5V supply is first if SEQ is tied to GND. When driving TIME/ON5 as a control input with external logic, always place a resistor (>1kΩ) in series with the input. This prevents possible crowbar current due to the internal discharge pulldown transistor, which turns on in standby mode and momentarily at the first power-up or in shutdown mode.

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

### RESET Power-Good Voltage Monitor

The power-good monitor generates a system RESET signal. At first power-up, RESET is held low until both the 3.3V and 5V SMPS outputs are in regulation. At this point, an internal timer begins counting oscillator pulses, and RESET continues to be held low until 32,000 cycles have elapsed. After this timeout period (64ms at 500kHz or 96ms at 333kHz), RESET is actively pulled up to $V_L$. If SEQ is tied to REF (for separate ON3/ON5 controls), only the 3.3V SMPS is monitored—the 5V SMPS is ignored.

### Output Undervoltage Shutdown Protection (MAX1901/MAX1902)

The output undervoltage lockout circuit is similar to foldback current limiting, but employs a timer rather than a variable current limit. Each SMPS has an undervoltage protection circuit that is activated 6144 clock cycles after the SMPS is enabled. If either SMPS output is under 70% of the nominal value, both SMPSs are latched off and their outputs are clamped to ground by the synchronous rectifier MOSFETs (see the *Output Overvoltage Protection* section). They won't restart until SHDN or RUN/ON3 is toggled, or until V+ power is cycled below 1V. Note that undervoltage protection can make prototype troubleshooting difficult, since you have only 12ms or 18ms to figure out what might be wrong with the circuit before both SMPSs are latched off. In extreme cases, it may be useful to substitute the MAX1904 into the prototype breadboard until the prototype is working properly.

### Output Overvoltage Protection (MAX1901/MAX1902)

Both SMPS outputs are monitored for overvoltage. If either output is more than 7% above the nominal regulation point, both low-side gate drivers (DL_) are latched high until SHDN or RUN/ON3 is toggled, or until V+ power is cycled below 1V. This action turns on the synchronous rectifiers with 100% duty, in turn rapidly discharging the output capacitors and forcing both SMPS outputs to ground. The DL outputs are also kept high whenever the corresponding SMPS is disabled, and in shutdown if $V_L$ is sustained.

Discharging the output capacitor through the main inductor causes the output to momentarily go below GND. Clamp this negative pulse with a back-biased 1A Schottky diode across the output capacitor (Figure 1).

To ensure overvoltage protection on initial power-up, connect signal diodes from both output voltages to $V_L$ (cathodes to $V_L$) to eliminate the $V_L$ power-up delay. This circuitry protects the load from accidental overvoltage caused by a short circuit across the high-side power MOSFETs. This scheme relies on the presence of a fuse, in series with the battery, which is blown by the resulting crowbar current. Note that the overvoltage circuitry will interfere with external keep-alive supplies that hold up the outputs (such as lithium backup or hot-swap power supplies); in such cases, the MAX1904 should be used.

### Low-Noise Operation (PWM Mode)

PWM mode (SKIP = high) minimizes RF and audio interference in noise-sensitive applications (such as hi-fi multimedia-equipped systems), cellular phones, RF communicating computers, and electromagnetic pen entry systems. See the summary of operating modes in Table 2. SKIP can be driven from an external logic signal.

## Table 4. Operating Modes

| SHDN | SEQ | RUN/ON3 | TIME/ON5 | MODE | DESCRIPTION |
|---|---|---|---|---|---|
| Low | X | X | X | Shutdown | All circuit blocks turned off. Supply current = 4µA. |
| High | REF | Low | Low | Standby | Both SMPSs off. Supply current = 30µA. |
| High | REF | High | Low | Run | 3.3V SMPS enabled/5V off. |
| High | REF | Low | High | Run | 5V SMPS enabled/3.3V off. |
| High | REF | High | High | Run | Both SMPSs enabled. |
| High | GND | Low | Timing Capacitor | Standby | Both SMPSs off. Supply current = 30µA. |
| High | GND | High | Timing Capacitor | Run | Both SMPSs enabled. 5V enabled before 3.3V. |
| High | VL | Low | Timing Capacitor | Standby | Both SMPSs off. Supply current = 30µA. |
| High | VL | High | Timing Capacitor | Run | Both SMPSs enabled. 3.3V enabled Before 5V. |

Interference due to switching noise is reduced in PWM mode by ensuring a constant switching frequency, thus concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator frequency for which switching frequency harmonics don't overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator. To extend the output-voltage regulation range, constant operating frequency is not maintained under overload or dropout conditions (see the *Dropout Operation* section).

PWM mode ($\overline{SKIP}$ = high) forces two changes upon the PWM controllers. First, it disables the minimum-current comparator, ensuring fixed-frequency operation. Second, it changes the detection threshold for reverse current limit from 0 to -100mV, allowing the inductor current to reverse at light loads. This results in fixed-frequency operation and continuous inductor-current flow. This eliminates discontinuous-mode inductor ringing and improves cross regulation of transformer-coupled multiple-output supplies, particularly in circuits that don't use additional secondary regulation via SECFB or $V_{DD}$.

In most applications, tie $\overline{SKIP}$ to GND to minimize quiescent supply current. VL supply current with $\overline{SKIP}$ high is typically 30mA, depending on external MOSFET gate capacitance and switching losses.

### Internal Digital Soft-Start Circuit

Soft-start allows a gradual increase of the internal current-limit level at startup to reduce input surge currents. Both SMPSs contain internal digital soft-start circuits, each controlled by a counter, a digital-to-analog converter (DAC), and a current-limit comparator. In shutdown or standby mode, the soft-start counter is reset to zero. When an SMPS is enabled, its counter starts counting oscillator pulses, and the DAC begins incrementing the comparison voltage applied to the current-limit comparator. The DAC output increases from 0 to 100mV in five equal steps as the count increases to 512 clocks. As a result, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on output capacitance and load current, and is typically 600µs with a 500kHz oscillator.

### Dropout Operation

Dropout (low input-output differential operation) is enhanced by stretching the clock pulse width to increase the maximum duty factor. The algorithm follows: If the output voltage ($V_{OUT}$) drops out of regulation without the current limit having been reached, the SMPS skips an off-time period (extending the on-time). At the end of the cycle, if the output is still out of regulation, the SMPS skips another off-time period. This action can continue until three off-time periods are skipped, effectively dividing the clock frequency by as much as four.

The typical PWM minimum off-time is 300ns, regardless of the operating frequency. Lowering the operating frequency raises the maximum duty factor above 97%.

### Adjustable-Output Feedback (Dual Mode FB)

Fixed, preset output voltages are selected when FB_ is connected to ground. Adjusting the main output voltage with external resistors is simple for any of the MAX1901/MAX1902/MAX1904, through resistor dividers connected to FB3 and FB5 (Figure 2). Calculate the output voltage with the following formula:

$$V_{OUT} = V_{REF} (1 + R1 / R2)$$

where $V_{REF}$ = 2.5V nominal.

The nominal output should be set approximately 1% or 2% high to make up for the MAX1901/MAX1902/MAX1904 -2% typical load-regulation error. For example, if designing for a 3.0V output, use a resistor ratio that results in a nominal output voltage of 3.05V. This slight offsetting gives the best possible accuracy. Recommended normal values for R2 range from 5kΩ to 100kΩ. To achieve a 2.5V nominal output, simply connect FB_ directly to CSL_.

Remote output-voltage sensing, while not possible in fixed-output mode due to the combined nature of the voltage-sense and current-sense inputs (CSL3 and CSL5), is easy to do in adjustable mode by using the top of the external resistor-divider as the remote sense point.

When using adjustable mode, it is a good idea to always set the "3.3V output" to a lower voltage than the "5V output." The 3.3V output must always be less than VL, so that the voltage on CSH3 and CSL3 is within the common-mode range of the current-sense inputs. While VL is nominally 5V, it can be as low as 4.7V when linearly regulating, and as low as 4.2V when automatically bootstrapped to CSH5.

### Secondary Feedback Regulation Loop (SECFB or $V_{DD}$)

A flyback-winding control loop regulates a secondary winding output, improving cross-regulation when the primary output is lightly loaded or when there is a low input-output differential voltage. If $V_{DD}$ or SECFB falls below its regulation threshold, the low-side switch is turned on for an extra 0.75µs. This reverses the induc-

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

tor (primary) current, pulling current from the output filter capacitor and causing the flyback transformer to operate in forward mode. The low impedance presented by the transformer secondary in forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing $V_{DD}$ or SECFB back into regulation. The secondary feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this condition, secondary output accuracy is determined by the secondary rectifier drop, transformer turns ratio, and accuracy of the main output voltage. A linear post-regulator may still be needed to meet strict output-accuracy specifications.

MAX1902 has a $V_{DD}$ pin that regulates at a fixed 13.5V, set by an internal resistor-divider. The MAX1901/MAX1904 have an adjustable secondary-output voltage set by an external resistor-divider on SECFB (Figure 5). Ordinarily, the secondary regulation point is set 5% to 10% below the voltage normally produced by the flyback effect. For example, if the output voltage as determined by turns ratio is 15V, set the feedback resistor ratio to produce 13.5V. Otherwise, the SECFB one-shot might be triggered unintentionally, unnecessarily increasing supply current and output noise.

### 12V Linear Regulator Output (MAX1902)

The MAX1902 includes a 12V linear regulator output capable of delivering 120mA of output current. Typically, greater current is available at the expense of output accuracy. If an accurate output of more than 120mA is needed, an external pass transistor can be added. The circuit in Figure 6 delivers more than 200mA. Total output current is constrained by the V+ input voltage and the transformer primary load (see Maximum $V_{DD}$ Output Current vs. Input Voltage graphs in the *Typical Operating Characteristics*).

## Design Procedure

The three predesigned 3V/5V standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common application needs. Also, one standard flyback transformer circuit supports the 12OUT linear regulator in the *Applications Information* section. Use the following design procedure to optimize these basic schematics for different voltage or current requirements. But before beginning a design, firmly establish the following:

**Maximum Input (Battery) Voltage, $V_{IN(MAX)}$**. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is

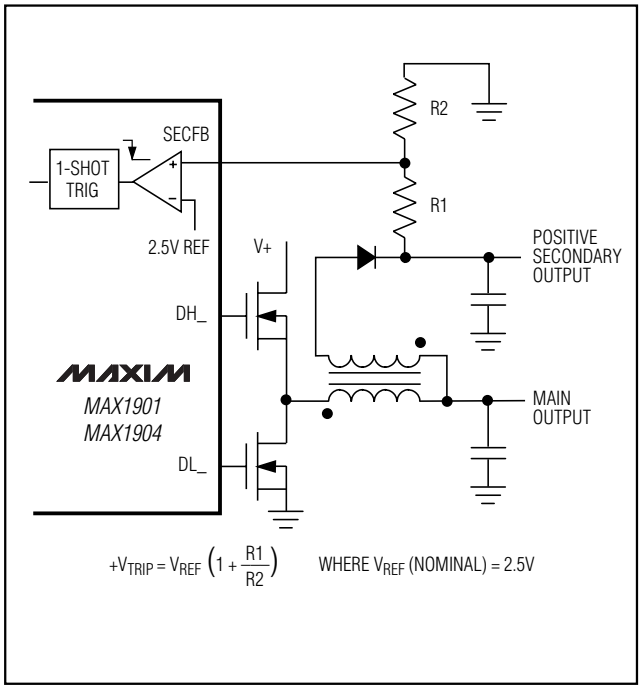



*Figure 5. Adjusting the Secondary Output Voltage with SECFB*

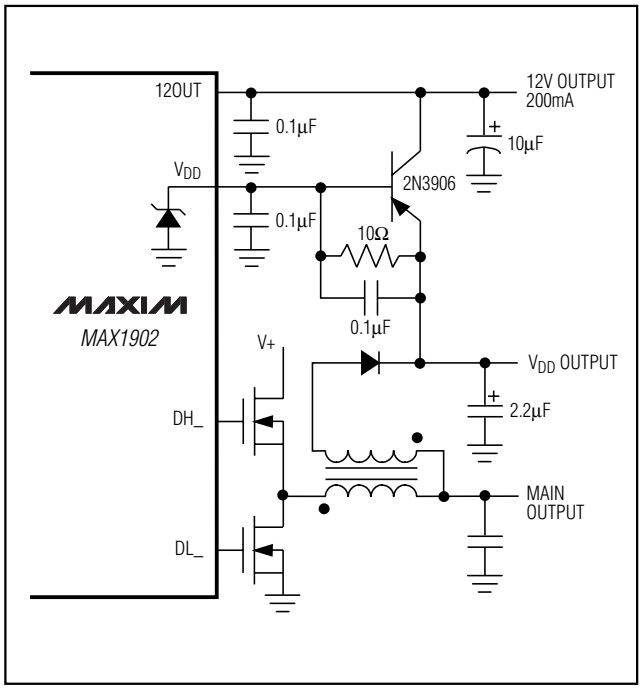



*Figure 6. Increased 12V Linear Regulator Output Current*

connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V.

**Minimum Input (Battery) Voltage, $V_{IN(MIN)}$.** This should be taken at full load under the lowest battery conditions. If $V_{IN(MIN)}$ is less than 4.2V, use an external circuit to externally hold $V_L$ above the $V_L$ undervoltage lockout threshold. If the minimum input-output difference is less than 1.5V, the filter capacitance required to maintain good AC load regulation increases (see the *Low-Voltage Operation* section).

### Inductor Value

The exact inductor value isn't critical and can be freely adjusted to make trade-offs between size, cost, and efficiency. Lower inductor values minimize size and cost, but reduce efficiency due to higher peak-current levels. The smallest inductor is achieved by lowering the inductance until the circuit operates at the border between continuous and discontinuous mode. Further reducing the inductor value below this crossover point results in discontinuous-conduction operation even at full load. This helps lower output-filter capacitance requirements, but efficiency suffers due to high $I^2R$ losses. On the other hand, higher inductor values mean greater efficiency, but resistive losses due to extra wire turns will eventually exceed the benefit gained from lower peak-current levels. Also, high inductor values can affect load-transient response (see the $V_{SAG}$ equation in the *Low-Voltage Operation* section). The equations that follow are for continuous-conduction operation, since the MAX1901/MAX1902/MAX1904 are intended mainly for high-efficiency, battery-powered applications. Discontinuous conduction doesn't affect normal idle-mode operation.

Three key inductor parameters must be specified: inductance value (L), peak current ($I_{PEAK}$), and DC resistance ($R_{DC}$). The following equation includes a constant (LIR) which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple. A good compromise between size and losses is found at a 30% ripple-current to load-current ratio (LIR = 0.3), which corresponds to a peak-inductor current 1.15 times higher than the DC load current.

$$L = \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times f \times I_{OUT} \times LIR}$$

where: f = switching frequency, normally 333kHz or 500kHz

$I_{OUT}$ = maximum DC load current

LIR = ratio of AC to DC inductor current, typically 0.3; should be >0.15

The nominal peak-inductor current at full load is 1.15 × $I_{OUT}$ if the above equation is used; otherwise, the peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + \frac{\left(V_{OUT}(V_{IN(MAX)} - V_{OUT}\right)}{2 \times f \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance should be low enough that $R_{DC} \times I_{PEAK} < 100mV$, as it is a key parameter for efficiency performance. If a standard off-the-shelf inductor is not available, choose a core with an $LI^2$ rating greater than $L \times I_{PEAK}^2$ and wind it with the largest-diameter wire that fits the winding area. Ferrite core material is strongly preferred. Shielded-core geometries help keep noise, EMI, and switching-waveform jitter low.

### Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case low current-limit threshold voltage (from the *Electrical Characteristics*) and the peak inductor current:

$$R_{SENSE} = \frac{80mV}{I_{PEAK}}$$

Use $I_{PEAK}$ from the second equation in the *Inductor Value* section.

Use the calculated value of $R_{SENSE}$ to size the MOSFET switches and specify inductor saturation-current ratings according to the worst-case high current-limit threshold voltage:

$$I_{PEAK(MAX)} = \frac{120mV}{R_{SENSE}}$$

Low-inductance resistors, such as surface-mount metal-film, are recommended.

### Input-Capacitor Value

The input filter capacitor is usually selected according to input ripple current requirements and voltage rating, rather than capacitor value. Ceramic capacitors or Sanyo OS-CON capacitors are typically used to handle the power-up surge-currents, especially when connecting to robust AC adapters or low-impedance batteries. RMS input ripple current ($I_{RMS}$) is determined by the input voltage and load current, with the worst case occurring at $V_{IN} = 2 \times V_{OUT}$:

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Therefore, when $V_{IN}$ is 2 x $V_{OUT}$:

$$I_{RMS} = \frac{I_{LOAD}}{2}$$

### Bypassing V+

Bypass the V+ input with a 4.7µF tantalum capacitor paralleled with a 0.1µF ceramic capacitor, close to the IC. A 10Ω series resistor to $V_{IN}$ is also recommended.

### Bypassing VL

Bypass the VL output with a 4.7µF tantalum capacitor paralleled with a 0.1µF ceramic capacitor, close to the device.

### Output-Filter Capacitor Value

The output-filter capacitor values are generally determined by the ESR and voltage-rating requirements, rather than actual capacitance requirements for loop stability. In other words, the low-ESR electrolytic capacitor that meets the ESR requirement usually has more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sanyo POSCAP, or Kemet T510. To ensure stability, the capacitor must meet both minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}(1 + V_{OUT} / V_{IN(MIN)})}{V_{OUT} \times R_{SENSE} \times f}$$

$$R_{ESR} < \frac{R_{SENSE} \times V_{OUT}}{V_{REF}}$$

These equations are worst case, with 45° of phase margin to ensure jitter-free, fixed-frequency operation and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules with less-expensive capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

No well-defined boundary exists between stable and unstable operation. As phase margin is reduced, the first symptom is a bit of timing jitter, which shows up as blurred edges in the switching waveforms where the scope won't quite sync up. Technically speaking, this jitter (usually harmless) is unstable operation, since the duty factor varies slightly. As capacitors with higher ESRs are used, the jitter becomes more pronounced, and the load-transient output-voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output-voltage tolerance. Note that even with zero phase margin and gross instability present, the output-voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads).

The output-voltage ripple is usually dominated by the filter capacitor's ESR, and can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in continuous-conduction mode is $V_{NOISE\ (p-p)} = I_{RIPPLE} \times [R_{ESR} + 1/(2 \times \pi \times f \times C_{OUT})]$. In idle mode, the inductor current becomes discontinuous, with high peaks and widely spaced pulses, so the noise can actually be higher at light load (compared to full load). In idle mode, calculate the output ripple as follows:

$$V_{NOISE(P-P)} = \frac{0.025 \times R_{ESR}}{R_{SENSE}} + \frac{0.0003 \times L \times [1/V_{OUT} + 1/(V_{IN} - V_{OUT})]}{R_{SENSE}^2 \times C_{OUT}}$$

### Transformer Design (for Auxiliary Outputs Only)

Buck-plus-flyback applications, sometimes called "coupled-inductor" topologies, need a transformer to generate multiple output voltages. Performing the basic electrical design is a simple task of calculating turns ratios and adding the power delivered to the secondary to calculate the current-sense resistor and primary inductance. However, extremes of low input-output differentials, widely different output loading levels, and high turns ratios can complicate the design due to parasitic transformer parameters such as interwinding capacitance, secondary resistance, and leakage inductance. For examples of what is possible with real world transformers, see the Maximum $V_{DD}$ Output Current vs. Input Voltage graph in the *Typical Operating Characteristics*.

Power from the main and secondary outputs is combined to get an equivalent current referred to the main output voltage (see the *Inductor Value* section for parameter definitions). Set the current-sense resistor value at 80mV / $I_{TOTAL}$.

$P_{TOTAL}$ = The sum of the output power from all outputs

$I_{TOTAL} = P_{TOTAL} / V_{OUT}$ = The equivalent output current referred to $V_{OUT}$

$$L_{PRIMARY} = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{TOTAL} \times LIR}$$

$$\text{Turns Ratio } N = \frac{V_{SEC} + V_{FWD}}{V_{OUT(MIN)} + V_{RECT} + V_{SENSE}}$$

where: $V_{SEC}$ = the minimum required rectified secondary output voltage

$V_{FWD}$ = the forward drop across the secondary rectifier

$V_{OUT(MIN)}$ = the minimum value of the main output voltage (from the *Electrical Characteristics* tables)

$V_{RECT}$ = the on-state voltage drop across the synchronous rectifier MOSFET

$V_{SENSE}$ = the voltage drop across the sense resistor

In positive-output applications, the transformer secondary return is often referred to the main output voltage, rather than to ground, to reduce the needed turns ratio. In this case, the main output voltage must first be subtracted from the secondary voltage to obtain $V_{SEC}$.

### Selecting Other Components

#### MOSFET Switches

The high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at $V_{GS}$ = 4.5V. Lower gate threshold specifications are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs will have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)} \times Q_G$ provides a good figure for comparing various MOSFETs. Newer MOSFET process technologies with dense cell structures generally perform best. The internal gate drivers tolerate >100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. $I^2R$ power losses are the greatest heat contributor for both high-side and low-side MOSFETs. $I^2R$ losses are distributed between Q1 and Q2 according to duty factor (see the following equations). Generally, switching losses affect only the upper MOSFET, since the Schottky rectifier clamps the switching node in most cases before the synchronous rectifier turns on. Gate charge losses are dissipated by the driver and don't heat the MOSFET. Calculate the temperature rise according to package thermal-resistance specifications to ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET occurs at maximum input voltage:

$$PD_{upperFET} = I_{LOAD}^2 \times R_{DS(ON)} \times DUTY + V_{IN} \times I_{LOAD} \times f \times \left( \frac{V_{IN} \times C_{RSS}}{I_{GATE}} + 20ns \right)$$

$$PD_{upperFET} = I_{LOAD}^2 \times R_{DS(ON)} \times (1\text{-}DUTY)$$

$$DUTY = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1})$$

where: On-state voltage drop $V_{Q\_} = I_{LOAD} \times R_{DS(ON)}$

$C_{RSS}$ = MOSFET reverse transfer capacitance

$I_{GATE}$ = DH driver peak output current capability (1A typ)

20ns = DH driver inherent rise/fall time

Under output short-circuit, the MAX1904 synchronous rectifier MOSFET suffers extra stress because its duty factor can increase to greater than 0.9. It may need to be oversized to tolerate a continuous DC short circuit. During short circuit, the MAX1901/MAX1902's output undervoltage shutdown protects the synchronous rectifier under output short-circuit conditions.

To reduce EMI, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source.

#### Rectifier Clamp Diode

The rectifier diode is a clamp across the low-side MOSFET that catches the negative inductor swing during the 60ns dead time between turning one MOSFET off and each low-side MOSFET on. The latest generations of MOSFETs incorporate a high-speed Schottky diode, which serves as an adequate clamp diode. For MOSFETs without integrated Schottky diodes, place a Schottky diode in parallel with the low-side MOSFET.

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

Use a Schottky diode with a DC current rating equal to one third of the load current. The Schottky diode's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

### Boost-Supply Diode

A signal diode such as a 1N4148 works well in most applications. If the input voltage can go below +6V, use a small (20mA) Schottky diode for slightly improved efficiency and dropout characteristics. Don't use large power diodes, such as 1N5817 or 1N4001, since high junction capacitance can pump up $V_L$ to excessive voltages.

### Rectifier Diode (Transformer Secondary Diode)

The secondary diode in coupled-inductor applications must withstand flyback voltages greater than 60V, which usually rules out most Schottky rectifiers. Common silicon rectifiers, such as the 1N4001, are also prohibited because they are too slow. This often makes fast silicon rectifiers such as the MURS120 the only choice. The flyback voltage across the rectifier is related to the $V_{IN}$ - $V_{OUT}$ difference, according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT}) \times N$$

where: N = the transformer turns ratio SEC/PRI

$V_{SEC}$ = the maximum secondary DC output voltage

$V_{OUT}$ = the primary (main) output voltage

Subtract the main output voltage ($V_{OUT}$) from $V_{FLYBACK}$ in this equation if the secondary winding is returned to $V_{OUT}$ and not to ground. The diode reverse-breakdown rating must also accommodate any ringing due to leakage inductance. The rectifier diode's current rating should be at least twice the DC load current on the secondary output.

### Low-Voltage Operation

Low input voltages and low input-output differential voltages each require extra care in their design. Low absolute input voltages can cause the $V_L$ linear regulator to enter dropout and eventually shut itself off. Low input voltages relative to the output (low $V_{IN}$ - $V_{OUT}$ differential) can cause bad load regulation in multi-output flyback applications (see the design equations in the *Transformer Design* section). Also, low $V_{IN}$ - $V_{OUT}$ differentials can also cause the output voltage to sag when the load current changes abruptly. The amplitude of the sag is a function of inductor value and maximum duty factor (an *Electrical Characteristics* parameter, 97% guaranteed over temperature at f = 333kHz), as follows:

$$V_{SAG} = \frac{I_{STEP}^2 \times L}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The cure for low-voltage sag is to increase the output capacitor's value. Take a 333kHz/6A application circuit as an example, at $V_{IN}$ = +5.5V, $V_{OUT}$ = +5V, L = 6.7µH, f = 333kHz, $I_{STEP}$ = 3A (half-load step), a total capacitance of 470µF keeps the sag less than 200mV. The capacitance is higher than that shown in the *Typical Application Circuit* because of the lower input voltage. Note that only the capacitance requirement increases, and the ESR requirements don't change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor.

## Applications Information

### Heavy-Load Efficiency Considerations

The major efficiency-loss mechanisms under loads are, in the usual order of importance:

- $P(I^2R) = I^2R$ losses
- P(tran) = transition losses
- P(gate) = gate-charge losses
- P(diode) = diode-conduction losses
- P(cap) = input capacitor ESR losses
- P(IC) = losses due to the IC's operating supply current

Inductor core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they aren't accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores, such as Kool-Mu, can work well:

$$\text{Efficiency} = P_{OUT}/P_{IN} \times 100\% = P_{OUT}/(P_{OUT} + P_{TOTAL}) \times 100\%$$

$$P_{TOTAL} = P(I^2R) + P(tran) + P(gate) + P(diode) + P(cap) + P(IC)$$

$$P(I^2R) = I_{LOAD}^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

where RDC is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and $R_{SENSE}$ is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high-side and low-side switches: because they time-share the inductor current. If the MOSFETs aren't identical, their losses can be estimated by averaging the losses according to duty factor.

**Table 5. Low-Voltage Troubleshooting Chart**

| SYMPTOM | CONDITION | ROOT CAUSE | SOLUTION |
|---|---|---|---|
| Sag or droop in $V_{OUT}$ under step-load change | Low $V_{IN}$ - $V_{OUT}$ differential, <1.5V | Limited inductor-current slew rate per cycle. | Increase bulk output capacitance per formula (see the *Low-Voltage Operation* section). Reduce inductor value. |
| Dropout voltage is too high ($V_{OUT}$ follows $V_{IN}$ as $V_{IN}$ decreases) | Low $V_{IN}$ - $V_{OUT}$ differential, <1V | Maximum duty-cycle limits exceeded. | Reduce operation to 333kHz. Reduce MOSFET on-resistance and coil DCR. |
| Unstable—jitters between different duty factors and frequencies | Low $V_{IN}$ - $V_{OUT}$ differential, <0.5V | Normal function of internal low-dropout circuitry. | Increase the minimum input voltage or ignore. |
| Secondary output won't support a load | Low $V_{IN}$ - $V_{OUT}$ differential, $V_{IN} < 1.3 \times V_{OUT(MAIN)}$ | Not enough duty cycle left to initiate forward-mode operation. Small AC current in primary can't store energy for flyback operation. | Reduce operation to 333kHz. Reduce secondary impedances; use a Schottky diode, if possible. Stack secondary winding on the main output. |
| Poor efficiency | Low input voltage, <5V | $V_L$ linear regulator is going into dropout and isn't providing good gate-drive levels. | Use a small 20mA Schottky diode for boost diode. Supply $V_L$ from an external source. |
| Won't start under load or quits before battery is completely dead | Low input voltage, <4.5V | $V_L$ output is so low that it hits the $V_L$ UVLO threshold. | Supply $V_L$ from an external source other than $V_{IN}$, such as the system 5V supply. |

$$P(tran) = V_{IN} \times I_{LOAD} \times f \times \frac{3}{2} \times \left[ \left( V_{IN} \times C_{RSS} / I_{GATE} \right) - 20ns \right]$$

where $C_{RSS}$ is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), $I_{GATE}$ is the DH gate-driver peak output current (1.5A typical), and 20ns is the rise/fall time of the DH driver (20ns typ).

$$P(gate) = Q_G \times f \times V_L$$

where $V_L$ is the internal-logic-supply voltage (5V), and $Q_G$ is the sum of the gate-charge values for low-side and high-side switches. For matched MOSFETs, $Q_G$ is twice the data sheet value of an individual MOSFET. If $V_{OUT}$ is set to less than 4.5V, replace $V_L$ in this equation with $V_{BATT}$. In this case, efficiency can be improved by connecting $V_L$ to an efficient 5V source, such as the system 5V supply:

$$P(diode) = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where $t_D$ is the diode-conduction time (120ns typ) and $V_{FWD}$ is the forward voltage of the diode.

This power is dissipated in the MOSFET body diode if no external Schottky diode is used:

$$P(cap) = (I_{RMS})^2 \times R_{ESR}$$

where $I_{RMS}$ is the input ripple current as calculated in the *Design Procedure* and *Input-Capacitor Value* sections.

### Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This makes the inductor current's AC component high compared to the load current, which increases core losses and $I^2R$ losses in the output filter capacitors. For best light-load efficiency, use MOSFETs with moderate gate-charge levels, and use ferrite, MPP, or other low-loss core material.

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

### Lossless-Inductor Current-Sensing

The DC resistance (DCR) of the inductor can be used to sense inductor current to improve the efficiency and to reduce the cost by eliminating the sense resistor. Figure 7 shows the sense circuit, where L is the inductance, $R_L$ is the inductor DCR, $R_S$, and $C_S$ form an RC low-pass sense network. If the time constant of the inductor is equal to that of the sense network, i.e.:

$$\frac{L}{R_L} = R_S C_S$$

then the voltage across $C_S$ becomes

$$V_S = R_L \times I_L$$

where $I_L$ is the inductor current.

Determine the required sense-resistor value using the equation given in the *Current-Sense Resistor Value* section. Choose an inductor with DCR equal or greater than the sense resistor value. If the DCR is greater than the sense-resistor value, use a divider to scale down the voltage. Use the maximum inductance and minimum DCR to get the maximum possible inductor time constant. Select $R_S$ and $C_S$ so that the maximum sense network time constant is equal or greater than the maximum inductor time constant.

### Reduced Output Capacitance Application

In applications where higher output ripple is acceptable, lower output capacitance or higher ESR output capacitors can be used. In such cases, cycle-by-cycle stability is maintained by adding feedforward compensation to offset for the increased output ESR. Figure 8 shows the addition of the feedforward compensation circuit. $C_{FB}$ provides noise filtering, $R_{FF}$ is the feedforward resistor and $C_{LX}$ provides DC blocking. Use 100pF for $C_{FB}$ and $C_{LX}$. Select $R_{FF}$ according to the equation below:

$$R_{FF} \le \frac{4 \times R3 \times L \times f}{ESR}$$

Set the value for $R_{FF}$ close to the calculation. Do not make $R_{FF}$ too small as that will introduce too much feedforward, possibly causing an overvoltage to be seen at the feedback pin, and changing the mode of operation to a voltage mode.

### PC Board Layout Considerations

Good PC board layout is required in order to achieve specified noise, efficiency, and stability performance. The PC board layout artist must be given explicit instructions, preferably a pencil sketch showing the placement of power-switching components and high-current routing. A ground plane is essential for optimum

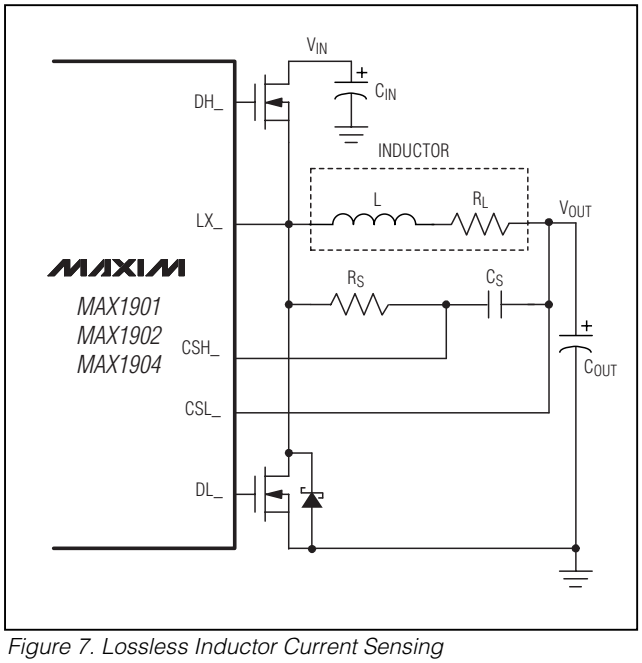



*Figure 7. Lossless Inductor Current Sensing*

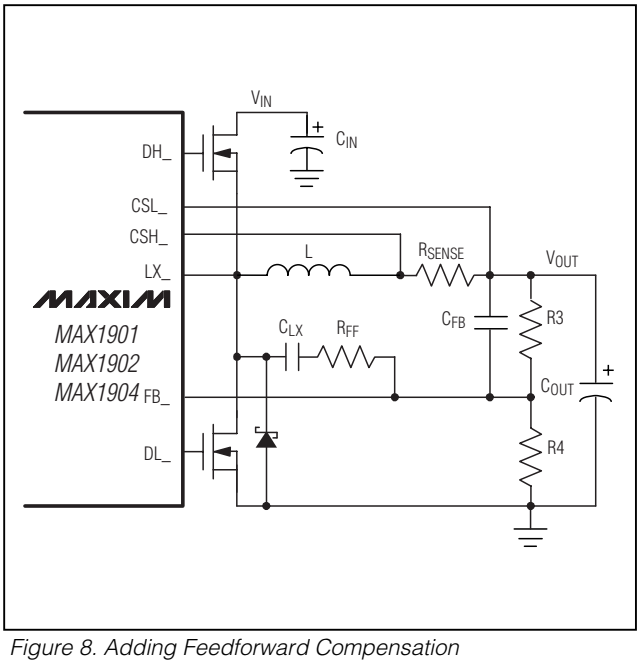



*Figure 8. Adding Feedforward Compensation*

performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, SS, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

1) Place the high-power components (Figure 1, C1, C3, C4, Q1, Q2, L1, and R1) first, with their grounds adjacent.
   - Priority 1: Minimize current-sense resistor trace lengths and ensure accurate current sensing with Kelvin connections (Figure 9).
   - Priority 2: Minimize ground trace lengths in the high-current paths (discussed below).
   - Priority 3: Minimize other trace lengths in the high current paths.

     Use >5mm-wide traces

     CIN to high-side MOSFET drain: 10mm max length

     Rectifier diode cathode to low-side MOSFET: 5mm max length

     LX node (MOSFETs, rectifier cathode, inductor): 15mm max length

Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide filled zone of top-layer copper so they don't go through vias. The resulting top layer "sub-ground-plane" is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems.

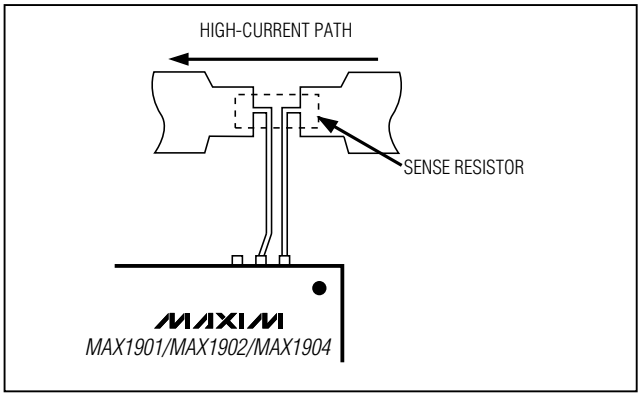
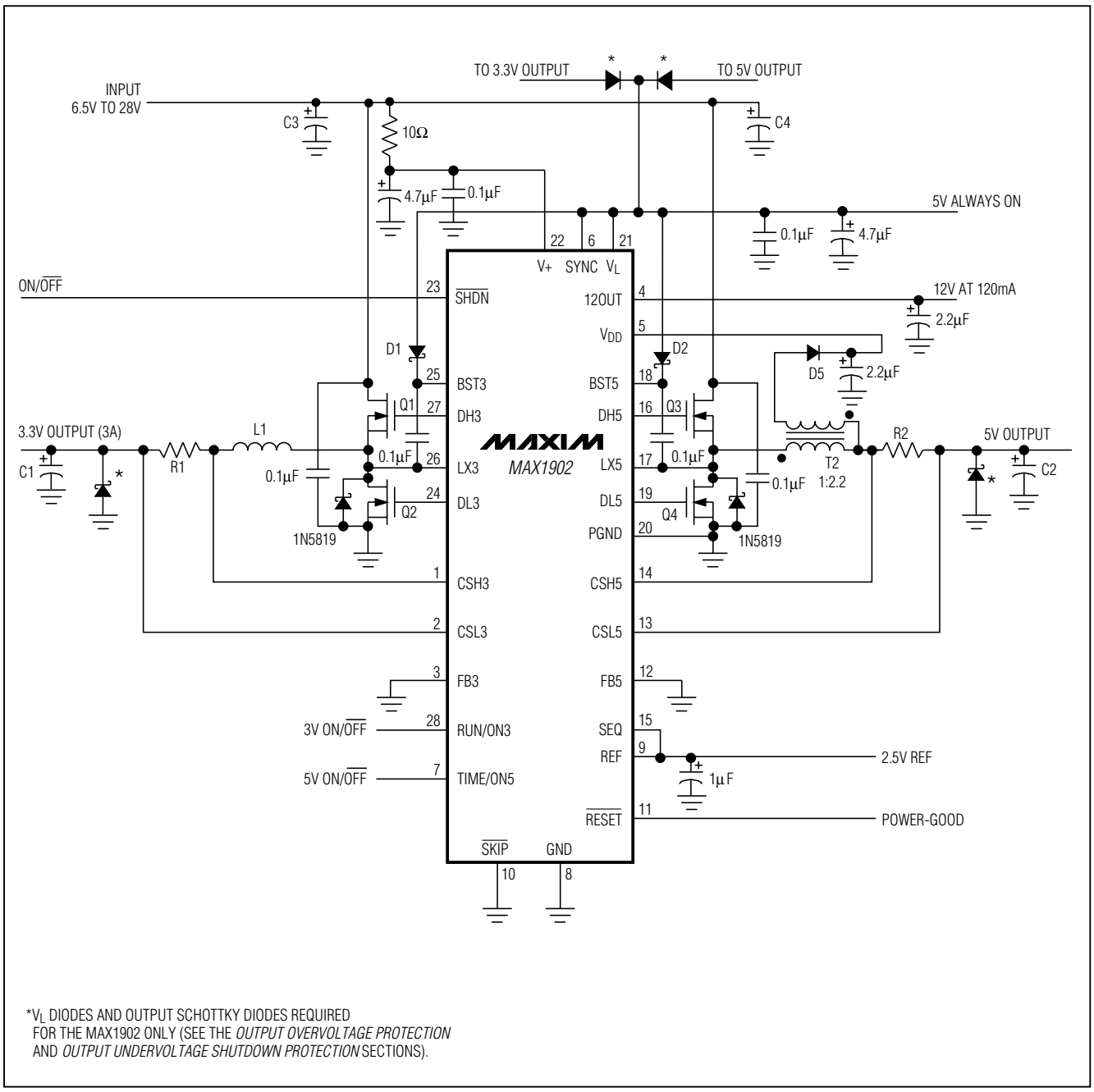



*Figure 9. Kelvin Connections for the Current-Sense Resistors*

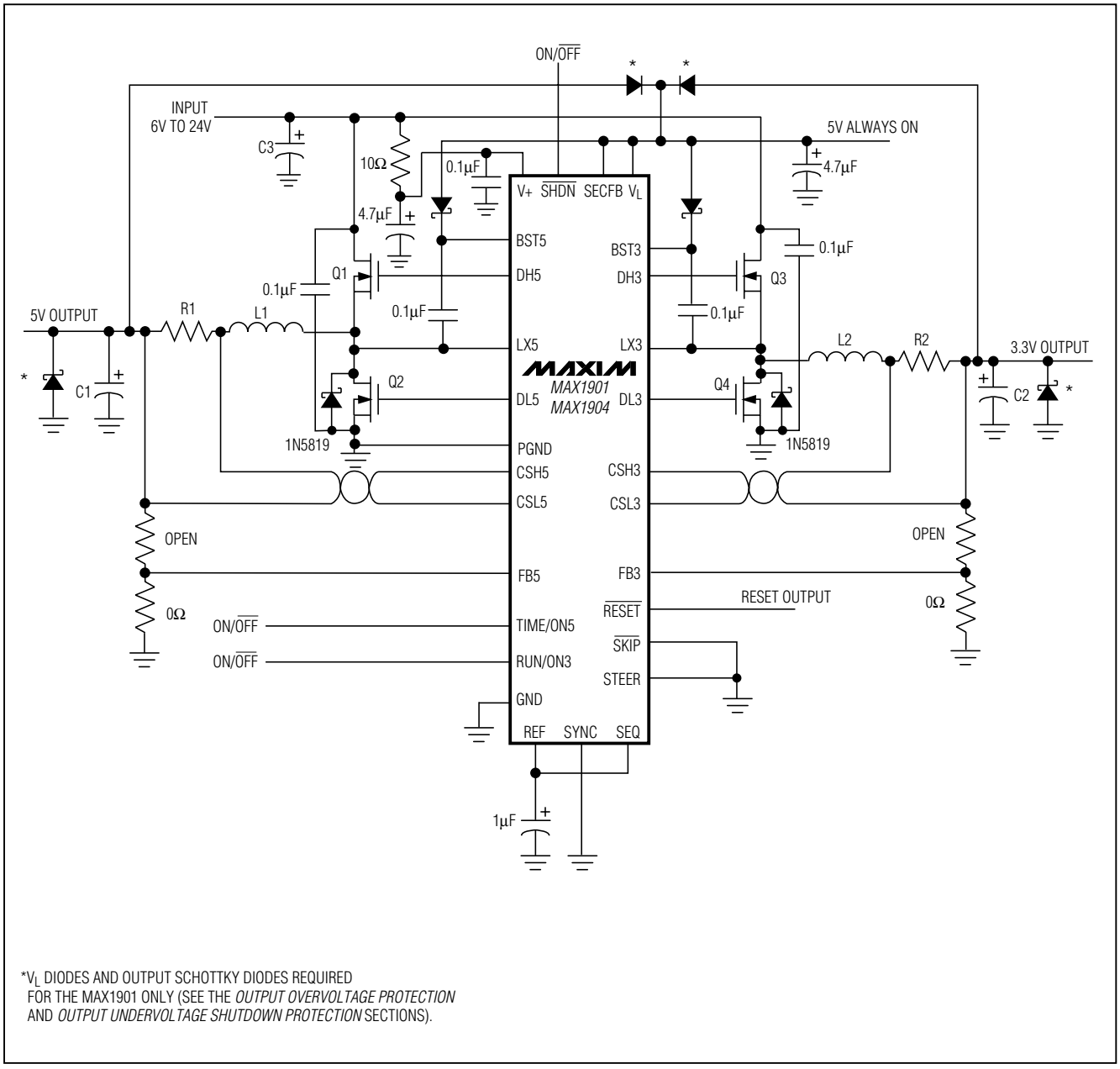
2) Place the IC and signal components. Keep the main switching nodes (LX nodes) away from sensitive analog components (current-sense traces and REF capacitor). Place the IC and analog components on the opposite side of the board from the power-switching node. **Important:** the IC must be no more than 10mm from the current-sense resistors. Keep the gate-drive traces (DH_, DL_, and BST_) shorter than 20mm and route them away from CSH_, CSL_, and REF.
3) Use a single-point star ground where the input ground trace, power ground (sub-ground-plane), and normal ground plane meet at the supply's output ground terminal. Connect both IC ground pins and all IC bypass capacitors to the normal ground plane.

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers




*$V_L$ DIODES AND OUTPUT SCHOTTKY DIODES REQUIRED FOR THE MAX1902 ONLY (SEE THE *OUTPUT OVERVOLTAGE PROTECTION* AND *OUTPUT UNDERVOLTAGE SHUTDOWN PROTECTION* SECTIONS).

*Figure 10. Triple Output Application for MAX1902*




*$V_L$ DIODES AND OUTPUT SCHOTTKY DIODES REQUIRED FOR THE MAX1901 ONLY (SEE THE *OUTPUT OVERVOLTAGE PROTECTION* AND *OUTPUT UNDERVOLTAGE SHUTDOWN PROTECTION* SECTIONS).

*Figure 11. Dual 6A Notebook Computer Power Supply*

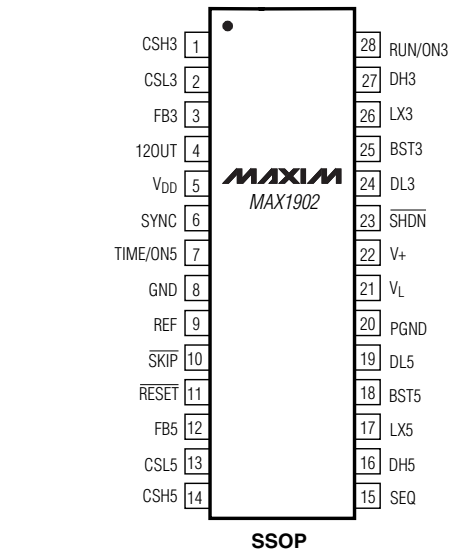
# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## Selector Guide

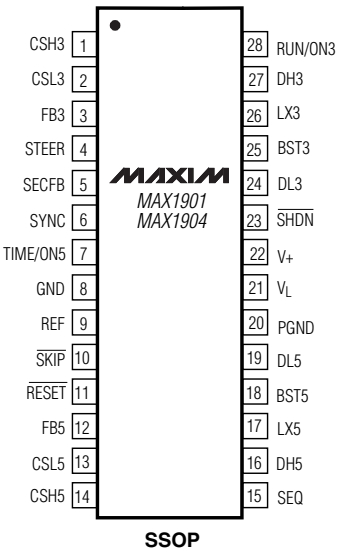
| DEVICE | AUXILLARY OUTPUT | SECONDARY FEEDBACK | OVER/UNDERVOLTAGE PROTECTION |
|---|---|---|---|
| MAX1901 | None (SECFB input) | Selectable (STEER pin) | Yes |
| MAX1902 | 12V Linear Regulator | Feeds into the 5V SMPS | Yes |
| MAX1904 | None (SECFB input) | Selectable (STEER pin) | No |

## Pin Configurations

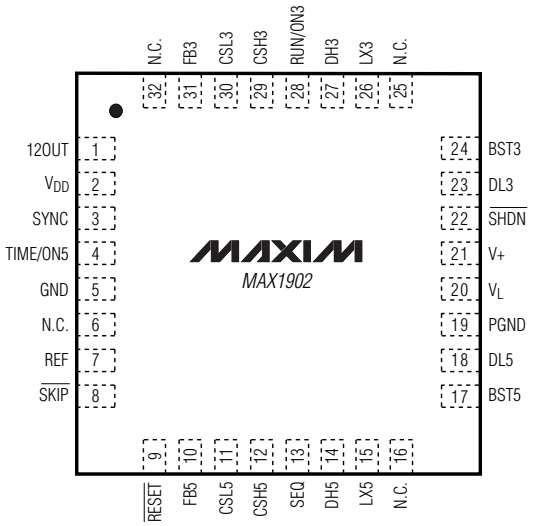
TOP VIEW



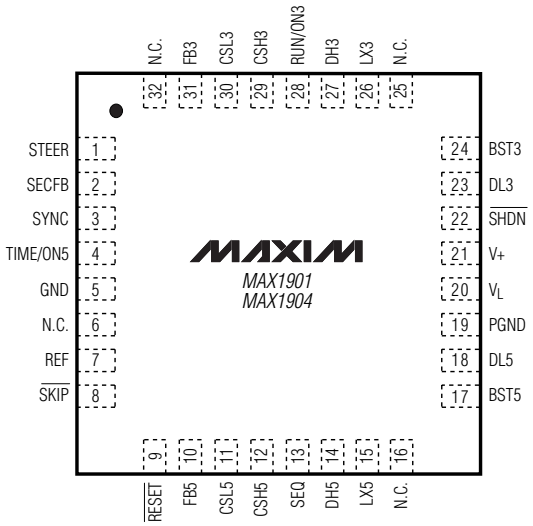

SSOP




SSOP




32 THIN QFN 5mm × 5mm

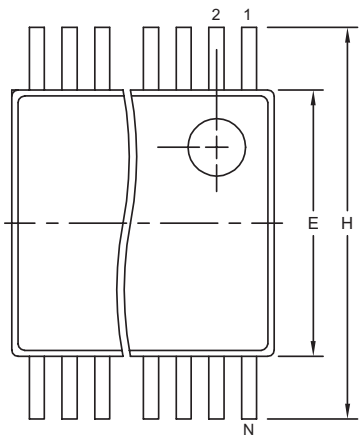



32 THIN QFN 5mm × 5mm

## Package Information

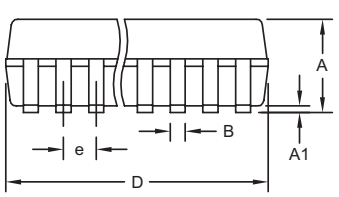
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

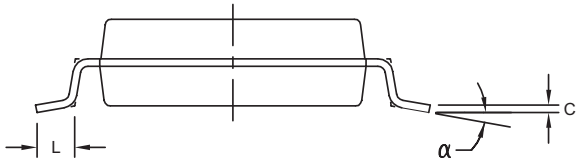
SSOP.EPS




| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.068 | 0.078 | 1.73 | 1.99 |
| A1 | 0.002 | 0.008 | 0.05 | 0.21 |
| B | 0.010 | 0.015 | 0.25 | 0.38 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | SEE VARIATIONS | | | |
| E | 0.205 | 0.212 | 5.20 | 5.38 |
| e | 0.0256 BSC | | 0.65 BSC | |
| H | 0.301 | 0.311 | 7.65 | 7.90 |
| L | 0.025 | 0.037 | 0.63 | 0.95 |
| α | 0∞ | 8∞ | 0∞ | 8∞ |

| | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | N |
|---|---|---|---|---|---|
| D | 0.239 | 0.249 | 6.07 | 6.33 | 14L |
| D | 0.239 | 0.249 | 6.07 | 6.33 | 16L |
| D | 0.278 | 0.289 | 7.07 | 7.33 | 20L |
| D | 0.317 | 0.328 | 8.07 | 8.33 | 24L |
| D | 0.397 | 0.407 | 10.07 | 10.33 | 28L |




NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

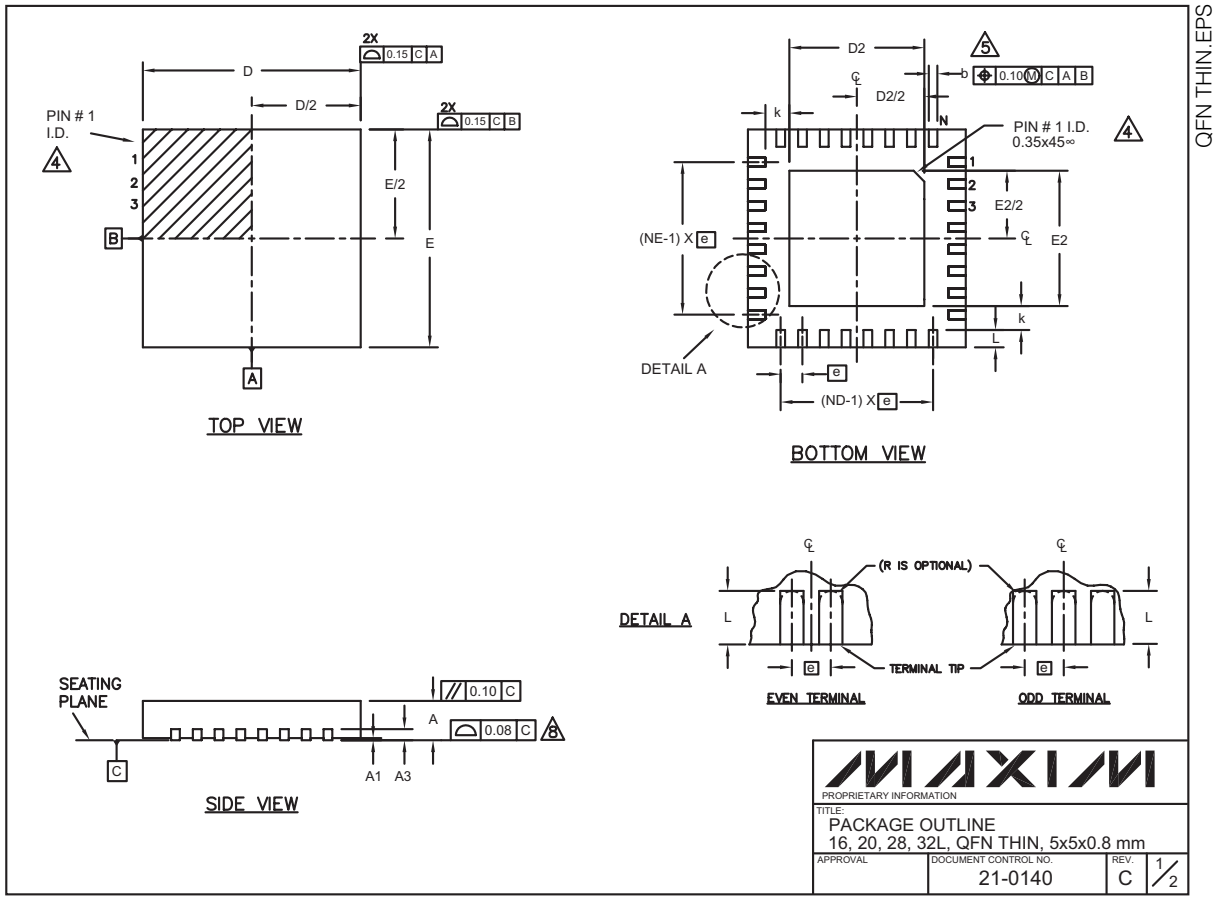
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0056 | C | 1/1 |

# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



# 500kHz Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A3 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 16 | | | 20 | | | 28 | | | 32 | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | |

EXPOSED PAD VARIATIONS

| PKG. CODES | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2855-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-2 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T3255-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | C | 2/2 |

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