ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +3.6V
RFL, RFH0, RFH1,
V_{CCIFCP}, V_{CCRFCP}, V_{CCDRV} to GND .....-0.3V to +5.5V
DI, CLK, $\overline{CS}$, GC, $\overline{SHDN}$, $\overline{TXGATE}$,
$\overline{IDLE}$, LOCK to GND .....-0.3V to (V_{CC} + 0.3V)
AC Input Pins (IFINL_, IFINH_, Q_, I_, TANKL_, TANKH_,
REF, RFPLL, LOL, LOH).....1.0V peak
Digital Input Current ($\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$,
CLK, DI, $\overline{CS}$) .....±10mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin QFN-EP (derate 27mW/°C above +70°C) 2.1W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(**MAX2361/MAX2363/MAX2365**, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.4V, R_{BIAS} = 10kΩ, I_{CC}CTRL is in power-up state, no AC signals applied, V_{CC} = +2.7V to +3.3V, V_{BAT} = +2.7V to +4.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{BAT} = +2.8V, T_A = +25°C, and operating modes are defined in Table 9.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}			2.7		3.3	V
	V_{BAT}			2.7		4.5	
Operating Supply Current	PCS mode	V_{GC} = 0.6V			50	82	mA
		V_{GC} = 1.95V			55	90	
		MPL = 0	P_{RFH0} = +5dBm		114		
			P_{RFH1} = +5dBm		121		
		MPL = 1	P_{RFH0} = +8dBm		137		
			P_{RFH1} = +8dBm		146		
	Cellular mode	V_{GC} = 0.6V			48	78	
		V_{GC} = 1.95V			53	86	
		MPL = 0, P_{RFL} = +5dBm			102		
		MPL = 1, P_{RFL} = +8dBm			126		
	FM mode	V_{GC} = 1.95V			75	85	
		MPL = 1, P_{RFL} = +11dBm			87		
	Addition for IFLO buffer				3.4	7.7	
	$\overline{IDLE}$ = low, PSS = 0				6	10	
	$\overline{IDLE}$ = low, PSS = 1				7.2	12.2	
	$\overline{TXGATE}$ = low, RFPLL off				11	17	
Leakage Current	$\overline{SHDN}$ = low, RFH_, RFL, V_{CCDRV}				0.5	20	µA
Logic High				0.7V_{CC}			V
Logic Low						0.3V_{CC}	V
Logic Input Current				-5		+5	µA
GC Input Current					6	11	µA
GC Input Resistance During Shutdown	$\overline{SHDN}$ = low			215	340		kΩ
Lock Indicator High	100kΩ pullup load			V_{CC} - 0.4			V
Lock Indicator Low	100kΩ pullup load					1.0	V

ELECTRICAL CHARACTERISTICS

(**MAX2361/MAX2363/MAX2365 EV kit**, 50Ω system, operating modes as defined in Table 9, TEMP_COMP = 10, input voltage at I and Q = 600mV$_{P-P}$ differential, 300kHz quadrature CW tones, RF and IF synthesizers locked, V_{REF} = 200mV$_{P-P}$ at 19.68MHz, V_{CC} = V_{BAT} = $\overline{SHDN}$ = IDLE = $\overline{CS}$ = $\overline{TXGATE}$ = 2.8V, LOH, LOL input power = -10dBm, f_{LOL} = 966.38MHz, f_{LOH} = 1750MHz, f_{RFH0} = f_{RFH1} = 1880.38MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
MODULATOR, QUADRATURE MODES (CDMA, PCS, FM_IQ)						
IF Frequency Range	IF_SEL = 0			120–235		MHz
	IF_SEL = 1			120–380		
I/Q Common-Mode Input Voltage	V_{CC} = +2.7V to +3.3V (Notes 1, 2, 3)		1.35	V_{CC} / 2	V_{CC} - 1.25	V
I_/Q_ Input Current	Common-mode voltage = 1.4V				6	µA
IF Gain-Control Range	V_{GC} = 0.6V to 2.4V, IFG = 100			85		dB
IF Output Power at IFOUTL and IFOUTH	IFG = 100, ACPR = -60dBc (Note 4)			-7		dBm
Gain Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C (Note 1)		-1		+1	dB
Carrier Suppression	V_{GC} = 2.4V, IFG = 100, f_{IFOUTL} = 130.38MHz (Note 1)		35	43		dB
Sideband Suppression	V_{GC} = 2.4V, IFG = 100, f_{IFOUTL} = 130.38MHz (Note 1)		35	45		dB
IF Output Noise	V_{GC} = 2.4V, noise measured at 20MHz offset			-143		dBm/ Hz
MODULATOR, FM MODE						
Output Power at IFOUTL	V_{GC} = 2.4V, IFG = 100, I/Q modulation			-9		dBm
	V_{GC} = 2.4V, IFG = 100, direct VCO modulation			-4		
UPCONVERTER AND PREDRIVER						
IF Frequency Range	IF_SEL = 0			120–235		MHz
	IF_SEL = 1			180–380		
RFL Frequency Range	RFL port			800–1000		MHz
RFH_ Frequency Range	RFH0 and RFH1 ports			1700–2000		MHz
LOL Frequency Range				800–1150		MHz
LOH Frequency Range				800–2360		MHz
LO Input Power	LOL, LOH		-10	-7		dBm
RFPLL Frequency Range	PSS = 0				1300	MHz
	PSS = 1				2360	
Conversion Gain	MPL = 0, T_A = -40°C to +85°C	RFL		19.2		dB
		RFH0		18.9		
		RFH1		17.6		
	MPL = 1, T_A = -40°C to +85°C	RFL		22.4		
		RFH0		22.8		
		RFH1		21.4		
RF Gain-Control Range	V_{GC} = 0.6V to 2.4V			40		dB
Image Signal	At maximum output power			-35		dBc

ELECTRICAL CHARACTERISTICS (continued)

(**MAX2361/MAX2363/MAX2365 EV kit**, 50Ω system, operating modes as defined in Table 9, TEMP_COMP = 10, input voltage at I and Q = 600mV$_{P-P}$ differential, 300kHz quadrature CW tones, RF and IF synthesizers locked, V_{REF} = 200mV$_{P-P}$ at 19.68MHz, V_{CC} = V_{BAT} = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{CS}$ = $\overline{TXGATE}$ = 2.8V, LOH, LOL input power = -10dBm, f_{LOL} = 966.38MHz, f_{LOH} = 1750MHz, f_{RFH0} = f_{RFH1} = 1880.38MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CASCADED MODULATOR, UPCONVERTER, AND PREDRIVER						
RFL Output Power	MPL = 1, T_A = -40°C to +85°C, meets ACPR specifications (Note 1)		6.8	9		dBm
RFH0 Output Power	MPL = 1, T_A = -40°C to +85°C, meets ACPR specifications (Note 1)		7.7	10.7		dBm
RFH1 Output Power	MPL = 1, T_A = -40°C to +85°C, meets ACPR specifications (Note 1)		6.6	9.7		dBm
RFL Adjacent Channel Power Ratio	f_{OFFSET} = ±885kHz in 30kHz bandwidth				-52	dBc
RFL Alternate Channel Power Ratio	f_{OFFSET} = ±1.98MHz in 30kHz bandwidth				-65	dBc
RFH_ Adjacent Channel Power Ratio	f_{OFFSET} = ±1.25MHz in 30kHz bandwidth				-52	dBc
RFH_ Alternate Channel Power Ratio	f_{OFFSET} = ±1.98MHz in 30kHz bandwidth				-68	dBc
RX Band Noise Power (Note 1)	MPL =1, P_{RFL} = +8dBm	Noise measured at +45MHz offset		-131	-128	dBm/Hz
	MPL =0, P_{RFL} = +5dBm			-134	-131	
	MPL =1, $P_{RFH\_}$ = +8dBm	Noise measured at +80MHz offset		-131	-128	
	MPL =0, $P_{RFH\_}$ = +5dBm			-133	-130	
Output Power Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C			±1		dB
IF_PLL						
Reference Frequency			5		30	MHz
Reference Frequency Signal Level			0.1		0.6	V_{P-P}
IF Main Divide Ratio			256		16383	
IF Reference Divide Ratio			2		2047	
VCO Operating Range	VCO_SEL =0			240–470		MHz
	VCO_SEL =1			240–760		
Charge-Pump Source/Sink Current	ICP = 00		114	139	178	µA
	ICP = 01		158	192	246	
	ICP = 10		228	278	356	
	ICP = 11		319	390	499	

ELECTRICAL CHARACTERISTICS (continued)

(**MAX2361/MAX2363/MAX2365 EV kit**, 50Ω system, operating modes as defined in Table 9, TEMP_COMP = 10, input voltage at I and Q = 600mV$_{P-P}$ differential, 300kHz quadrature CW tones, RF and IF synthesizers locked, V_{REF} = 200mV$_{P-P}$ at 19.68MHz, V_{CC} = V_{BAT} = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{CS}$ = $\overline{TXGATE}$ = 2.8V, LOH, LOL input power = -10dBm, f_{LOL} = 966.38MHz, f_{LOH} = 1750MHz, f_{RFH0} = f_{RFH1} = 1880.38MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

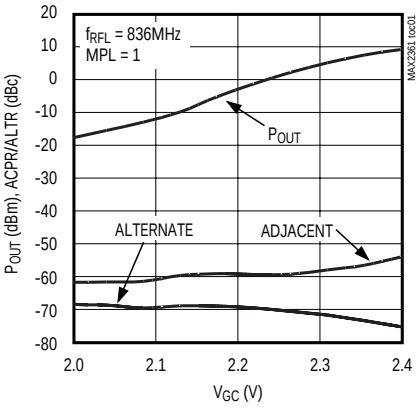
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Turbolock Boost Current	ICP_MAX = 1	632	774	987	µA
Charge-Pump Source/Sink Matching	All values of ICP, over specified compliance range			6	%
IF Charge-Pump Compliance		0.5		V_{CCIFCP} - 0.5	V
Charge-Pump High-Z Leakage	Over specified compliance range		20		pA
RF_PLL					
Reference Frequency		5		30	MHz
RF Main Divide Ratio		4096		262143	
RF Reference Divide Ratio		2		8191	
Charge-Pump Source/Sink Current	RCP = 00	266	325	416	µA
	RCP = 01	533	650	832	
	RCP = 10	605	738	945	
	RCP = 11	872	1063	1361	
Turbolock Boost Current	(Note 5)	1388	1694	2168	µA
Charge-Pump Source/Sink Matching	All values of RCP, over specified compliance range			6	%
RF Charge Pump Compliance		0.5		V_{CCRFCP} - 0.5	V
Phase Detector Noise Floor	RCP = 11, RCP_TURBO1 = RCP_TURBO2 = 0, 30kHz comparison frequency		-162		dBc/Hz
Charge-Pump High-Z Leakage	Over specified compliance range		20		pA
RFPLL Input Sensitivity		160			MV$_{P-P}$

Note 1: Guaranteed by design and characterization to 3 sigma (includes board and component variations).
Note 2: ACPR is met over the specified V_{CM} range.
Note 3: V_{CM} must be supplied by the I/Q baseband source with ±8µA capability.
Note 4: IQ_LEVEL = 0, $V_{Q\_}$ = $V_{I\_}$ = 87mV$_{RMS}$ differential, IS98 reverse channel modulation at 415mVp-p differential with 0.1% 4.5dB peak-to-average ratio.
Note 5: When enabled with RCP_TURBO1 and RCP_TURBO2 (see Tables 2 and 3), the total charge-pump current is specified. For all values of RCP, the total turbolock current is 1.63 times the corresponding nonturbo current value.

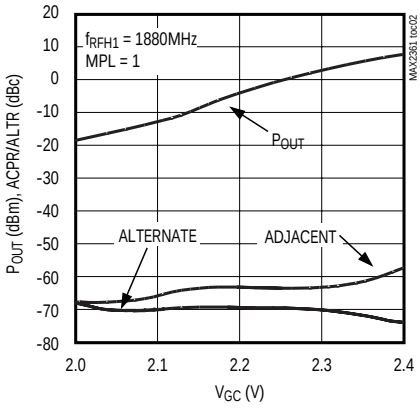
Typical Operating Characteristics

(MAX2361 EV kit, V_{CC} = V_{BAT} = +2.8V, T_A = +25°C, unless otherwise noted.)

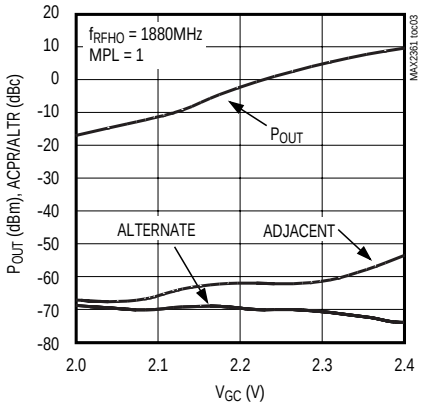
OUTPUT POWER, ACPR vs. V_{GC} (RFL)



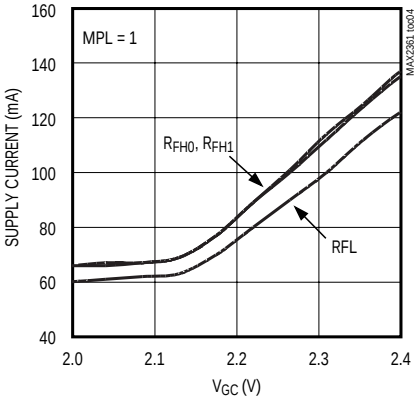
OUTPUT POWER, ACPR vs. V_{GC} (RFH1)



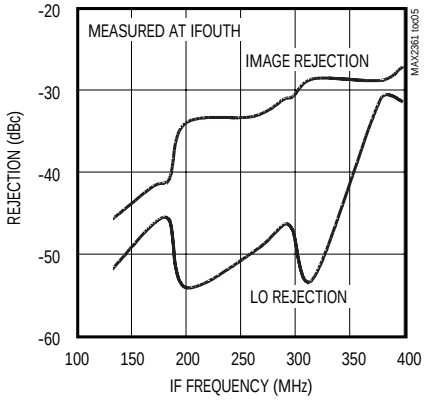
OUTPUT POWER, ACPR vs. V_{GC} (RFH0)



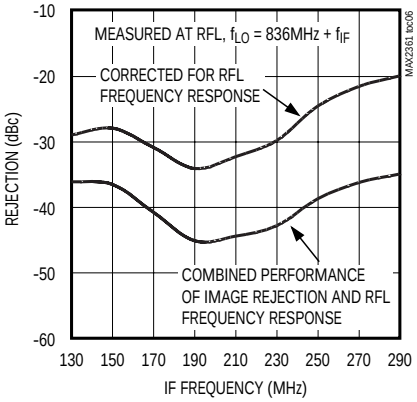
SUPPLY CURRENT vs. V_{GC}



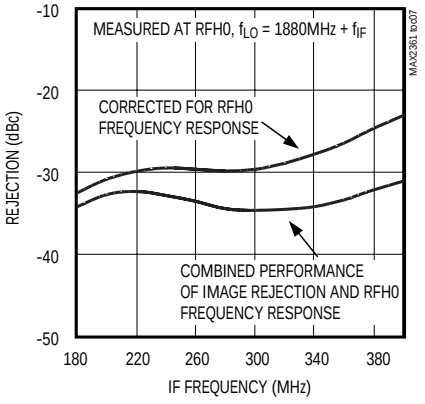
IF IMAGE REJECTION



RF IMAGE REJECTION FROM IFINL



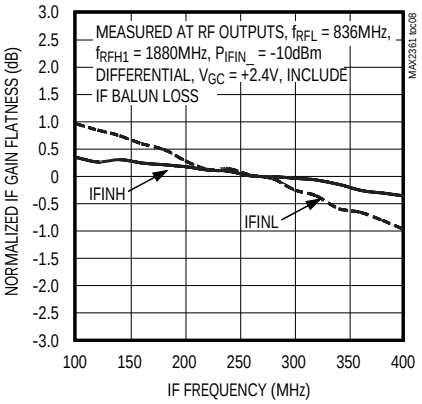
RF IMAGE REJECTION FROM IFINH



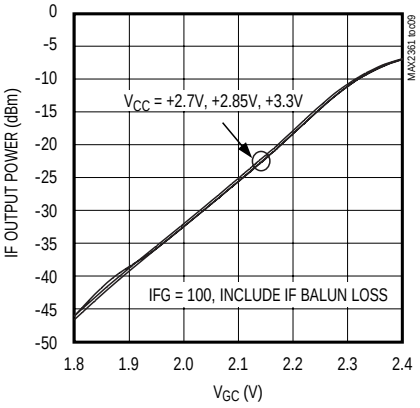
Typical Operating Characteristics (continued)

(MAX2361 EV kit, V_{CC} = V_{BAT} = +2.8V, T_A = +25°C, unless otherwise noted.)

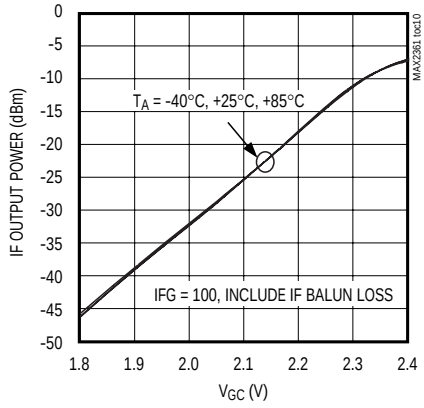
IF GAIN FLATNESS vs. FREQUENCY



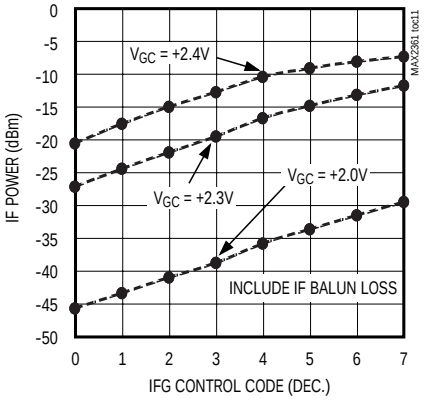
IF OUTPUT POWER vs. V_{GC}



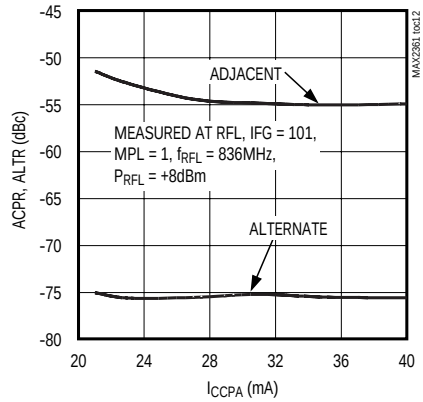
IF OUTPUT POWER vs. V_{GC}



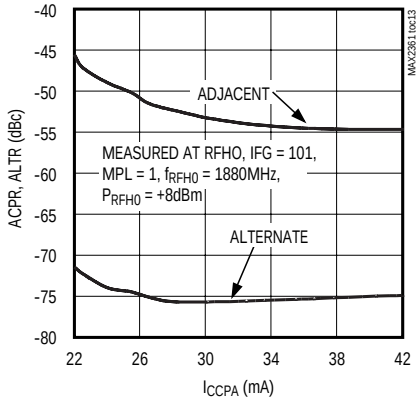
IF POWER vs. IFG SETTING



CASCADED ACPR AND ALTR vs. I_{CCPA} (RFL)



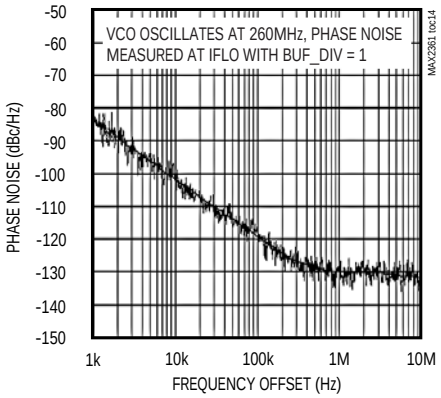
CASCADED ACPR AND ALTR vs. I_{CCPA} (RFH0)



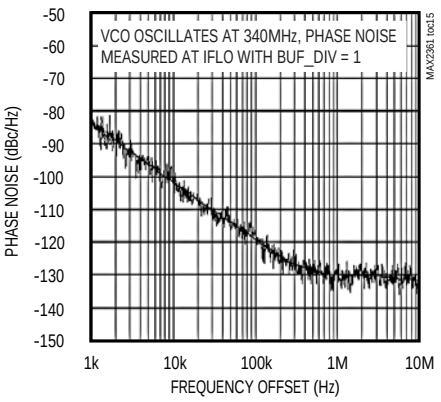
Typical Operating Characteristics (continued)

(MAX2361 EV kit, V_{CC} = V_{BAT} = +2.8V, T_A = +25°C, unless otherwise noted.)

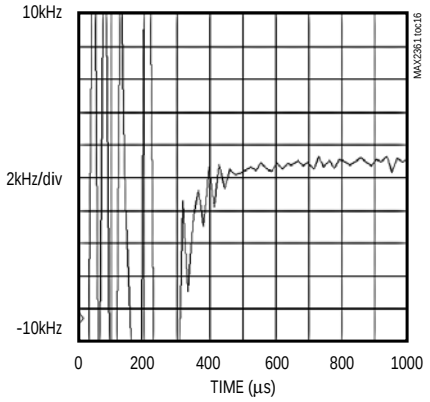
**PHASE NOISE vs. FREQUENCY OFFSET
TANKL OSCILLATOR**



**PHASE NOISE vs. FREQUENCY OFFSET
TANKH OSCILLATOR**

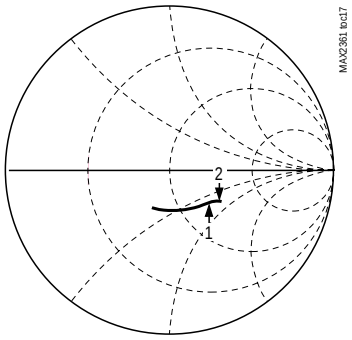


IF PLL LOCK TIME



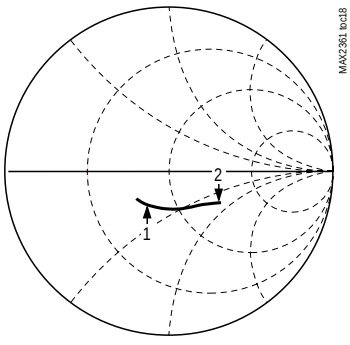
ICP = 11, ICP_MAX = 0
f_{COMP} = 240kHz, f_{IF} = 263.64MHz
LOOP FILTER: 20kΩ IN SERIES WITH 2.2nF, 220pF PARALLEL
LOOP BW = 10kHz

LOL PORT S_{11}



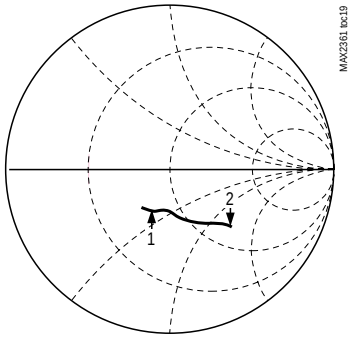
START: 700MHz
STOP: 2.5GHz
1: 1GHz: 74.9Ω - j34.4Ω
2: 800MHz: 81Ω - j37.4Ω

LOH PORT S_{11}



START: 700MHz
STOP: 2.5GHz
1: 2.36GHz: 37.2Ω - j16.8Ω
2: 800MHz: 80Ω - j38.9Ω

RFPLL PORT S_{11}



START: 700MHz
STOP: 2.5GHz
1: 2.36GHz: 38.3Ω - j20.2Ω
2: 800MHz: 70.4Ω - j61.6Ω

Pin Description

PIN			NAME	FUNCTION
MAX2361	MAX2363	MAX2365		
1	—	1	RFL	Transmitter RF Output for Cellular Band (800MHz to 1000MHz)—for both FM and digital modes. This open-collector output requires a pullup inductor to the supply voltage, which may be part of the output matching network and can be connected directly to the battery.
2	2	—	RFH0	Transmitter RF Output for PCS Band (1700MHz to 2000MHz). This open-collector output requires a pullup inductor to the supply voltage. The pullup inductor may be part of the output matching network and may be connected directly to the battery. For split band PCS application, use RFH0 for the 1880MHz–1910MHz range.
3	3	3	LOCK	Open-Collector Output Indicating Lock Status of the IF and/or the RF PLLs. Requires a pullup resistor. Control using configuration register bits LD_MODE.
4	4	4	V_{CCDRV}	Supply Pin for the Driver Stage. May be connected directly to the battery. Bypass to PC board ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch.
5	5	5	$\overline{IDLE}$	Digital Input, Drive to Logic High for Normal Operation. A logic low on $\overline{IDLE}$ shuts down everything except the RF PLL and associated registers. A small R-C lowpass can be used to filter digital noise.
6	6	6	V_{CC}	Supply Pin for the Upconverter Stage. V_{CC} must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch.
7	7	7	$\overline{TXGATE}$	Digital Input, Drive to Logic High for Normal Operation. A logic low on $\overline{TXGATE}$ shuts down everything except the RF PLL, IF PLL, IF VCO, and serial bus and registers. This mode is used for gated transmission.
8, 9	—	8, 9	IFINL+, IFINL-	Differential Inputs to the RF Upconverter. These pins are internally biased. The input impedance for these ports is nominally 400Ω differential. The IF filter should be AC-coupled to these ports. Keep the differential lines as short as possible to minimize stray pickup and shunt capacitance.
10, 11	10, 11	—	IFINH+, IFINH-	Differential Inputs to the RF Upconverter. These pins are internally biased. The input impedance for these ports is nominally 400Ω differential. The IF filter should be AC-coupled to these ports. Keep the differential lines as short as possible to minimize stray pickup and shunt capacitance.
12	12	12	BIAS	Bias Resistor Pin. BIAS is internally biased to approximately 600mV. An external resistor between this pin to GND sets the bias current for the upconverters and PA driver stages. The nominal resistor value is 10kΩ. This value can be altered to optimize the linearity of the driver stage.
13, 14, 15	13, 14, 15	13, 14, 15	CLK, DI, $\overline{CS}$	Input Pins from the 3-Wire Serial Bus (SPI/QSPI/MICROWIRE compatible)

Pin Description (continued)

PIN			NAME	FUNCTION
MAX2361	MAX2363	MAX2365		
16, 17	16, 17	—	IFOUTH-, IFOUTH+	Differential IF Outputs. These ports are active when the register bit IF_SEL is 1. They do not support FM mode. These pins must be inductively pulled up to V_{CC}. A differential IF bandpass filter is connected between this port and IFINH+ or IFINH-. The pullup inductors can be part of the filter structure. The differential output impedance of this port is nominally 600Ω. The transmission lines from these pins should be short to minimize the pickup of spurious signals and noise.
18, 19	—	18, 19	IFOUTL-, IFOUTL+	Differential IF Outputs. These ports are active when the register bit IF_SEL is 0. These pins must be inductively pulled up to V_{CC}. A differential IF bandpass filter is connected between this port and IFINL+ and IFINL-. The pullup inductors can be part of the filter structure. The differential output impedance of this port is nominally 600Ω. The transmission lines from these pins should be short to minimize the pickup of spurious signals and noise.
20	20	20	GC	RF and IF Gain Control Analog Input. Apply 0.6V to 2.4V to control the gain of the RF and IF stages. An RC filter on this pin should be used to reduce DAC noise or PDM clock spurs from this line.
21	21	21	V_{CC}	Supply Pin for the IF VGA. Bypass with a capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches.
22	22	22	V_{CC}	Supply for the I/Q Modulator. Bypass with a capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches.
23, 24	23, 24	23, 24	Q+, Q-	Differential Q-Channel Baseband Inputs to the Modulator. These pins go directly to the bases of a differential pair and require an external common-mode bias voltage.
25, 26	25, 26	25, 26	I+, I-	Differential I-Channel Baseband Inputs to the Modulator. These pins go directly to the bases of a differential pair and require an external common-mode bias voltage.
27	27	27	$\overline{SHDN}$	Shutdown Input, Drive to Logic High for Normal Operation. A logic low on $\overline{SHDN}$ shuts down the entire IC except the serial interface and retains the information in all registers. An R-C lowpass can be used to filter digital noise.
28	28	28	V_{CC}	Supply Pin to the VCO Section. Bypass as close to the pin as possible. The bypass capacitor should not share its vias with any other branches.
29	29	29	IFLO	Buffered LO Output. Control the output buffer using register bit BUF_EN and the divide ratio using the register bit BUF_DIV.
30, 31	—	30, 31	TANKL-, TANKL+	Differential Tank Pins for the Low-Frequency IF VCO. These pins are internally biased. VCO_SEL = 0 selects this IF VCO.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX2361	MAX2363	MAX2365		
32, 33	32, 33	—	TANKH-, TANKH+	Differential Tank Pins for the High-Frequency IF VCO. These pins are internally biased. VCO_SEL = 1 selects this IF VCO.
34, 35	1, 8, 9, 18, 19, 30, 31, 34, 35, 44	2, 10, 11, 16, 17, 32–35 43, 47	N.C.	No Connection. Make no connection to these pins.
36	36	36	REF	Reference Frequency Input. REF is internally biased and must be AC-coupled to the reference source. This is a high-impedance port (25kΩ ‖ 3pF).
37	37	37	V_{CCIFCP}	Supply for the IF Charge Pump. This supply can differ from the system V_{CC}. Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branches.
38	38	38	IFCP	High-Impedance Output of the IF Charge Pump. Connect to the tune input of the IF VCOs through the IF PLL loop filter. Keep the line from IFCP to the tune input as short as possible to prevent spurious pick-up, and connect the loop filter as close to the tune input as possible.
39	39	39	V_{CC}	Supply Pin for Digital Circuitry. Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branch.
40	40	40	RFCP	High-Impedance Output of the RF Charge Pump. Connect to the tune input of the RF VCOs through the RF PLL loop filter. Keep the line from this pin to the tune input as short as possible to prevent spurious pickup, and connect the loop filter as close to the tune input as possible.
41	41	41	V_{CCRFCP}	Supply for the RF Charge Pump. This supply can differ from the system V_{CC}. Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branches.
42	42	42	RFPLL	RF PLL Input. AC-couple this port to the RF VCO. RFPLL is internally biased.
43	43	—	LOH	High-band RF LO Input Port. AC-couple to this port.
44	—	44	LOL	Low-band RF LO Input Port. AC-couple to this port.
45, 46, 48	45, 46, 48	45, 46, 48	GND	Isolation GND. No internal connection. Connect to PC board ground plane for better isolation.
47	47	—	RFH1	Transmitter RF Output for PCS Band (1700MHz to 2000MHz). This open-collector output requires a pullup inductor to the supply voltage. The pullup inductor may be part of the output matching network and can be connected directly to the battery. For split band PCS application, use RFH1 for the 1850MHz–1880MHz range.
EP	EP	EP	GND	DC and AC GND Return for the IC. Connect to PC board ground plane using multiple vias.

Detailed Description

The MAX2361 complete quadrature transmitter accepts differential I/Q baseband inputs with external common-mode bias. A modulator upconverts this to IF frequency in the 120MHz to 380MHz range. A gain-control voltage pin (GC) controls the gain of both the IF and RF VGAs simultaneously to achieve the best current consumption and linearity performance. The IF signal is brought off-chip for filtering, then fed to a single sideband upconverter followed by the RF VGA and PA driver. The RF upconverter requires an external VCO for operation. The IF PLL, RF PLL, and operating mode can be programmed by an SPI/QSPI/MICROWIRE-compatible 3-wire interface.

The following sections describe each block in the MAX2361 *Functional Diagram.*

I/Q Modulator

Differential in-phase (I) and quadrature-phase (Q) input pins are designed to be DC-coupled and biased with the baseband output from a digital-to-analog converter (DAC). I and Q inputs need a DC bias of $V_{CC}/2$ and a current-drive capability of 8µA. The I and Q inputs capacitance is typically 0.3pF differential. Common-mode voltage works within a 1.35V to (V_{CC} - 1.25V) range. The IF VCO output is fed into a divide-by-two/quadrature generator block to derive quadrature LO components to drive the IQ modulator. The output of the modulator is fed into the VGA.

IF VCOs

There are two VCOs to support high IF and low IF frequencies. The VCOs oscillate at twice the desired IF frequency. Oscillation frequency is determined by external tank components (see *Applications Information*). Typical phase-noise performance for the tank is as shown in the *Typical Operating Characteristics*. The high-band and low-band VCOs can be selected independently of the IF port being used.

IFLO Output Buffer

IFLO provides a buffered LO output when BUF_EN is 1. The IFLO output frequency is equal to the VCO frequency when BUF_DIV is 0, and half the VCO frequency when BUF_DIV is 1. The output power is -12dBm. This output is intended for applications where the receive IF is the same frequency as the transmit IF.

IF/RF PLL

The IF/RF PLL uses a charge-pump output to drive a loop filter. The loop filter typically is passive second-order lead lag filter. Outside the filter's bandwidth, phase noise is determined by the tank components. The two components that contribute most significantly to phase noise are the inductor and varactor. Use high-Q inductors and varactors to maximize equivalent parallel resistance. The IF_TURBO_CHARGE, RCP_TURBO1, and RCP_TURBO2 bits can be set to enable turbo mode. Turbo mode provides maximum charge-pump current during frequency acquisition. Turbo mode is disabled after frequency acquisition is achieved. When turbo mode is disabled, charge-pump current returns to the programmed levels as set by ICP and RCP bits in the CONFIG register (Table 3).

The PSS bit selects the RFPLL prescaler speed independent of the MODE bits. This enables PCS band VCO locking when transmitting in the cellular band. For VCO frequency above 1300MHz, set PSS to 1.

IF VGA

The IF VGA allows varying an IF output level that is controlled by GC voltage. The voltage range on GC of 0.6V to 2.4V provides a gain-control range of 85dB. There are two differential IF output ports from the VGA. IFOUTL+/IFOUTL- are optimized for low IF operation (120MHz to 235MHz); IFOUTH+/IFOUTH- support high IF operation (120MHz to 380MHz). IFOUTL supports FM mode by providing higher IF output level when MODE is set to 00.

Single Sideband Mixer

The RF transmit mixer uses a single sideband architecture to eliminate an off-chip RF filter. The single sideband mixer has IF input stages that correspond to IF output ports of the VGA. The mixer is followed by the RF VGA. The RF VGA is controlled by the same GC pin as the IF VGA to provide optimum current consumption and linearity performance. The total power-control range is >100dB.

PA Driver

The MAX2361 includes three power-amplifier (PA) drivers. Each is optimized for the desired operating frequency. RFL is optimized for cellular-band operation. RFH0 and RFH1 are optimized for split-band PCS operation. Use RFH0 in single high-band output such as TDMA or W-CDMA. The PA drivers have open-collector outputs and require pullup inductors. The pullup inductors can act as the shunt element in a shunt series match.

Programmable Registers

The MAX2361/MAX2363/MAX2365 include eight programmable registers consisting of four divide registers, a configuration register, an operational control register, a current control register, and a test register. Each register consists of 24 bits. The 4 least significant bits (LSBs) are the register's address. The 20 most significant bits (MSBs) are used for register data. All registers contain some "don't care" bits. These can be either a "0" or a "1" and will not affect operation (Figure 1). Data is shifted in MSB first, followed by the 4-bit address. When $\overline{CS}$ is low, the clock is active and data is shifted with the rising edge of the clock. When $\overline{CS}$ transitions to high, the shift register is latched into the register selected by the contents of the address bits. Power-up defaults for the eight registers are shown in Table 1. The dividers and control registers are programmed from the SPI/QSPI/MICROWIRE-compatible serial port.

The RFM register sets the main frequency divide ratio for the RF PLL. The RFR register sets the reference frequency divide ratio. The RF VCO frequency can be determined by the following:

$$\text{RF VCO frequency} = f_{REF} \times (\text{RFM} / \text{RFR})$$

IFM and IFR registers are similar:

$$\text{IF VCO frequency} = f_{REF} \times (\text{IFM} / \text{IFR})$$

where f_{REF} is the external reference frequency.

The operational control register (OPCTRL) controls the state of the MAX2361/MAX2363/MAX2365. See Table 2 for the function of each bit.

The configuration register (CONFIG) sets the configuration for the RF/IF PLL and the baseband I/Q input levels. See Table 3 for a description of each bit.

The current control register modifies the bias current to accommodate different operation modes. In the high-power mode, MPL = 1 sets the bias current and conversion gain to deliver a minimum of +8dBm output power from the PA drivers. In the low-power mode, MPL = 0 sets the bias current and conversion gain to deliver a minimum of +5dBm output power from the PA drivers. I_MULT sets the current multiplication factor for the PA driver stages according to Table 5. THROTTLE_BACK sets the rate of bias current changes when the output power changes according to Table 6. For example, when THROTTLE_BACK = 011 (default), the PA driver bias current reduces by 1dBmA for every 1dB reduction in output power. THROTTLE_BACK = 000 setting gives a more aggressive current reduction (1.3dBmA/dB power) at the expense of linearity. THROTTLE_BACK setting does not affect the bias current at maximum power level.

The test register has to be 100hex for normal operation. The best way to ensure this is to program the test register to 100hex.

Power Management

Bias control is distributed among several functional sections and can be controlled to accommodate many different power-down modes as shown in Table 8.

The serial interface remains active during shutdown. Setting SHDN_BIT = 0 or $\overline{SHDN}$ = GND powers down the device. In either case, PLL programming and register information is retained.

Signal Flow Control

Table 9 shows an example of key registers for triple-mode operation, assuming half-band PCS and IF frequencies of 228.6MHz/263.6MHz.

Applications Information

The MAX2361 is designed for use in dual-band, triple-mode systems. It is recommended for triple-mode handsets (Figure 2). The MAX2363 is designed for use in CDMA PCS handset or W-CDMA systems (Figure 3). The MAX2365 is designed for use in dual-mode cellular systems (Figure 4).

Table 1. Register Power-Up Default States

REGISTER	DEFAULT	ADDRESS	FUNCTION
RFM	32214 dec	0000_b	RF M divider count
RFR	656 dec	0001_b	RF R divider count
IFM	6519 dec	0010_b	IF M divider count
IFR	0492 dec	0011_b	IF R divider count
OPCTRL	090F hex	0100_b	Operational control settings
CONFIG	D03F hex	0101_b	Configuration and setup control
I_{CC}CTRL	0038 hex	0110_b	Current multiplication factor, PLL band
TEST	100 hex	0111_b	Test-mode control

	MSB																			LSB			
	24 BIT REGISTER																						
	DATA 20 BITS																			ADDRESS 4 BITS			
	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	A3	A2	A1	A0
RFM DIVIDE REGISTER			RFM DIVIDE RATIO (18)																		ADDRESS			
	X	X	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
RFR DIVIDE REGISTER								RFR DIVIDE RATIO (13)													ADDRESS			
	X	X	X	X	X	X	X	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	1
IFM DIVIDE REGISTER							IFM DIVIDE RATIO (14)														ADDRESS			
	X	X	X	X	X	X	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	1	0
IFR DIVIDE REGISTER										IFR DIVIDE RATIO (11)											ADDRESS			
	X	X	X	X	X	X	X	X	X	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	1	1
CONTROL REGISTER					OPERATION CONTROL BITS (16)																ADDRESS			
	X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	0	0
CONFIGURATION REGISTER					CONFIGURATION BITS (16)																ADDRESS			
	X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	0	1
CURRENT CONTROL REGISTER					CURRENT CONTROL BITS (16)																ADDRESS			
	X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	1	0
TEST REGISTER												TEST BITS (9)									ADDRESS			
	X	X	X	X	X	X	X	X	X	X	X	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	1	1

X = DON'T CARE

Figure 1. Register Configuration

Cascaded Performance

Tables 11 and 12 show the typical cascaded performance for TDMA and W-CDMA systems.

3-Wire Interface

Figure 5 shows the 3-wire interface timing diagram. The 3-wire bus is SPI/QSPI/MICROWIRE compatible.

Electromagnetic Compliance Considerations

Two major concepts should be employed to produce a low-spur and EMC-compliant transmitter: minimize circular current-loop area to reduce H-field radiation. To minimize circular current-loop area, bypass as close to the part as possible and use the distributed capacitance of a ground plane. To minimize voltage drops, make V_{CC} traces short and wide, and make RF traces short.

Program only the necessary bits in any register to minimize clock cycles. RC filtering can also be used to slow the clock edges on the 3-wire interface, reducing high-frequency spectral content. RC filtering also provides for transient protection against IEC802 testing by shunting high frequencies to ground, while the series resistance attenuates the transients for error-free operation. The same applies to the logic input pins ($\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$).

Table 2. Operation Control Register (OPCTRL)

BIT NAME	POWER-UP STATE	BIT LOCATION (0 = LSB)	FUNCTION
LO_SEL	0	15	0 selects LOL input port; 1 selects LOH port.
RCP_TURBO1	0	14	Works in conjunction with RCP_TURBO2 (CONFIG register) to set the turbo-charge pump mode. (See Table 7)
ICP_MAX	0	13	1 keeps IF turbo-mode current active even when frequency acquisition is achieved. This mode is used when high operating IF charge-pump current is needed.
MODE	01	12, 11	Sets operating mode according to the following: 00 = FM mode 01 = Cellular digital mode, RFL is selected 10 = Lower half-band PCS mode, RFH1 is selected 11 = Upper half-band PCS, RFH0 is selected
IF_SEL	0	10	1 selects IFINH and IFOUTH; 0 selects IFINL and IFOUTL. For FM mode (MODE = 00), set IF_SEL to 0.
VCO_SEL	0	9	1 selects high-band IF VCO; 0 selects low-band IF VCO.
IFG	100	8, 7, 6	3-Bit IF gain Control. Alters IF gain by approximately 2dB per LSB (0 to 14dB). Provides a means for adjusting balance between RF and IF gain for optimized linearity.
SIDE_BAND	0	5	When this bit is 1, the upper sideband is selected (LO below RF). When this bit is 0, the lower sideband is selected (LO above RF).
BUF_EN	0	4	0 turns IFLO buffer off; 1 turns IFLO buffer on.
MOD_TYPE	1	3	0 selects direct VCO modulation. (IF VCO is externally modulated and the I/Q modulator is bypassed); 1 selects quadrature modulation.
$\overline{\text{STBY}}$	1	2	0 shuts down everything except registers and serial interface.
$\overline{\text{TXSTBY}}$	1	1	0 shuts down modulator and upconverter, leaving PLLs locked and registers active. This is the programmable equivalent to the $\overline{\text{TXGATE}}$ pin.
SHDN_BIT	1	0	0 shuts down everything except serial interface, and also retains all register settings.

Table 3. Configuration Register (CONFIG)

BIT NAME	POWER-UP STATE	BIT LOCATION (0 = LSB)	FUNCTION
IF_PLL_SHDN	1	15	0 shuts down the IF PLL. This mode is used with an external IF PLL.
RF_PLL_ SHDN	1	14	0 shuts down the RF PLL. This mode is used with an external RF PLL.
ZERO_BIAS	0	13	0 for normal operation, 1 turns off the bias current to RFH0 output driver.
IQ_LEVEL	1	12	1 selects 200mV$_{RMS}$ input mode; 0 selects 100mV$_{RMS}$ input mode.
BUF_DIV	0	11	1 selects ÷2 on IFLO port; 0 bypasses the divider.
VCO_BYPASS	0	10	1 bypasses IF VCO and enables a buffered input for external VCO use.
ICP	00	9, 8	A 2-bit register sets the IF charge-pump current as follows: 00 = 139µA 01 = 192µA 10 = 278µA 11 = 390µA
RCP	00	7, 6	A 2-bit register sets the RF charge-pump current as follows: 00 = 325µA 01 = 650µA 10 = 738µA 11 = 1063µA
IF_PD_POL	1	5	IF phase-detector polarity; 1 selects positive polarity (increasing tuning voltage on the VCO produces increasing frequency); 0 selects negative polarity (increasing tuning voltage on the VCO produces decreasing frequency).
RF_PD_POL	1	4	RF phase-detector polarity; 1 selects positive polarity (increasing tuning voltage on the VCO produces increasing frequency); 0 selects negative polarity (increasing voltage on the VCO produces decreasing frequency).
IF_TURBO_ CHARGE	1	3	1 activates turbocharge feature, providing an additional IF charge-pump current during frequency acquisition.
RCP_TURBO2	1	2	Works in conjunction with RCP_TURBO1 (OPCTRL register) to set the turbocharge current mode. (See Table 7).
LD_MODE	11	1, 0	Determines output mode for LOCK detector pin as follows: 00 = test mode, LD_MODE cannot be 00 for normal operation 01 = IF PLL lock detector 10 = RF PLL lock detector 11 = logical AND of IF PLL and RF PLL lock detectors

Table 4. Current Control Register (I_{CC}CTRL)

BIT NAME	POWER-UP STATE	BIT LOCATION (0 = LSB)	FUNCTION
RESERVED	00	15, 14	Must be set to 00 for normal operation.
PSS	0	13	Prescaler speed select. 0 selects the lower frequency band RFPLL prescaler. 1 selects the higher frequency band prescaler.
RESERVED	0	12	Must be set to 0 for normal operation.
MPL	0	11	Sets the maximum output power level. 0 selects +6.5dBm, 1 selects +10dBm output power modes.
TEMP_COMP	00	10, 9	Sets current scale factor to compensate temperature variations. Set to 10 for best linearity over temperature.
RESERVED	0	8	Must be set to 0 for normal operation.
MOD_BYPASS	0	7	1 routes differential signal at pins 30 and 31 directly to the IF VGA and bypasses the IF modulator. This mode is used with external modulator.
THROTTLE_BACK	011	6, 5, 4	Throttle back rate (Table 6)
I_MULT	1000	3, 2, 1, 0	Sets current scale factor for PA drivers (Table 5)

Table 5. Current Scale Factors Set By I_MULT Bits

BIT NAME	BITS	CURRENT SCALE
I_MULT	0000	0.50
	0001	0.56
	0010	0.62
	0011	0.69
	0100	0.75
	0101	0.81
	0110	0.88
	0111	0.94
	1000 (default)	1.00
	1001	1.13
	1010	1.25
	1011	1.38
	1100	1.50
	1101	1.63
	1110	1.75
	1111	1.88

Table 6. Throttle-Back Rate Set By THROTTLE_BACK Bits

BIT NAME	BITS	RATE	UNIT
THROTTLE_BACK	000	1.3	dBmA/dB
	001	1.2	
	010	1.1	
	011 (default)	1.0	
	100	0.9	
	101	0.8	
	110	0.7	
	111	0.6	

Table 7. RF Turbo Charge-Pump Current Setting

RCP_TURBO1	RCP_TURBO2	
0	0	No turbo current. Charge-pump current is set by RCP bits.
0	1	Turbo current turns on every time RFPLL is reprogrammed. Turbo current is automatically turned off after RFPLL is locked.
1	0	Turbo current is always on.
1	1	Turbo current is turned on every time RFPLL is out of lock.

Table 8. Power-Down Modes

POWER-DOWN MODE	COMMENTS	UPCONVERTER	MODULATOR	RF_PLL	IF VCO	IF_PLL
$\overline{\text{SHDN}}$ Pin	Ultra-low shutdown current	X	X	X	X	X
$\overline{\text{IDLE}}$ Pin	RX only mode	X	X		X	X
$\overline{\text{TXGATE}}$ Pin	For punctured TX mode	X	X			
RF PLL SHDN	For external RF PLL use			X		
IF PLL SHDN	For external IF PLL use					X
$\overline{\text{TXSTBY}}$ Bit	TX is OFF, but IF and RF LOs stay locked	X	X			

X = Off

Table 9. Register and Control Pin States for Key Operating Modes

MODE	DESCRIPTION	OPCTRL REGISTER								CONFIG REGISTER		CONTROL PINS		
		LO_SEL	MODE	IF_SEL	VCO_SEL	MOD_TYPE	$\overline{STBY}$	$\overline{TXSTBY}$	SHDN_BIT	IF_PLL_SHDN	RF_PLL_SHDN	$\overline{IDLE}$	$\overline{TXGATE}$	$\overline{SHDN}$
PCS High	PCS upper half-band, RFH0 selected	1	11	1	1	1	1	1	1	1	1	H	H	H
PCS Low	PCS lower half-band, RFH1 selected	1	10	1	1	1	1	1	1	1	1	H	H	H
Cellular Digital	RFL selected	0	01	0	0	1	1	1	1	1	1	H	H	H
FM	Direct VCO modulation, RFL selected	0	00	0	0	0	1	1	1	1	1	H	H	H
PCS Idle	Listen for pages RX ON, TX OFF	1	1X	1	1	1	1	X	1	X	1	L	H	H
Cellular Idle	Listen for pages RX ON, TX OFF	0	0X	0	0	X	1	X	1	X	1	L	H	H
PCS TXGATE	Gated transmission, PCS	1	1X	1	1	1	1	X	1	1	1	H	L	H
Cellular TXGATE	Gated transmission, cellular digital	0	01	0	0	1	1	X	1	1	1	H	L	H
Sleep	Ultra-Low Current	X	XX	X	X	X	X	X	X	X	X	X	X	L

X = Don't care

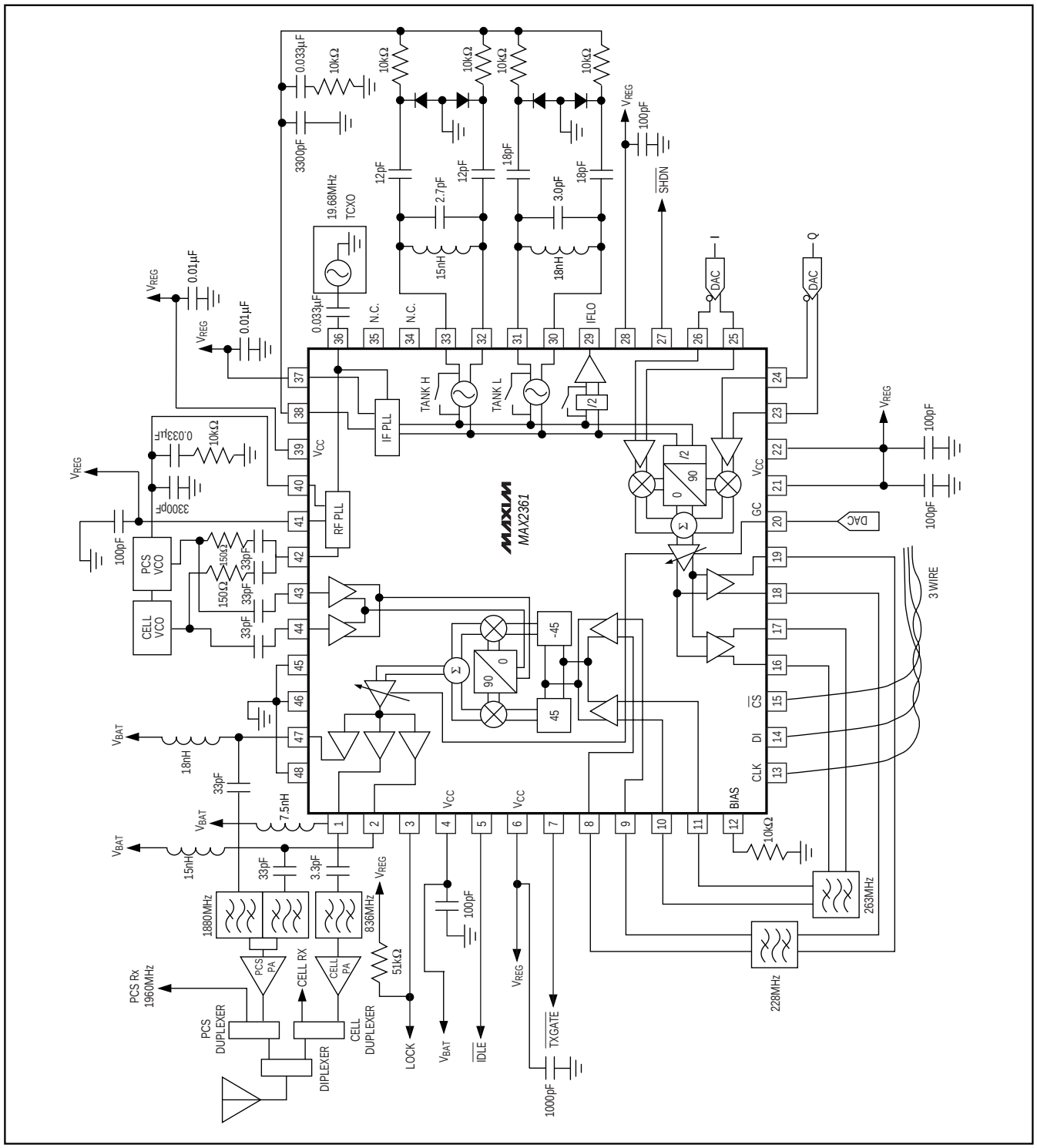


Figure 2. MAX2361 Typical Application Circuit

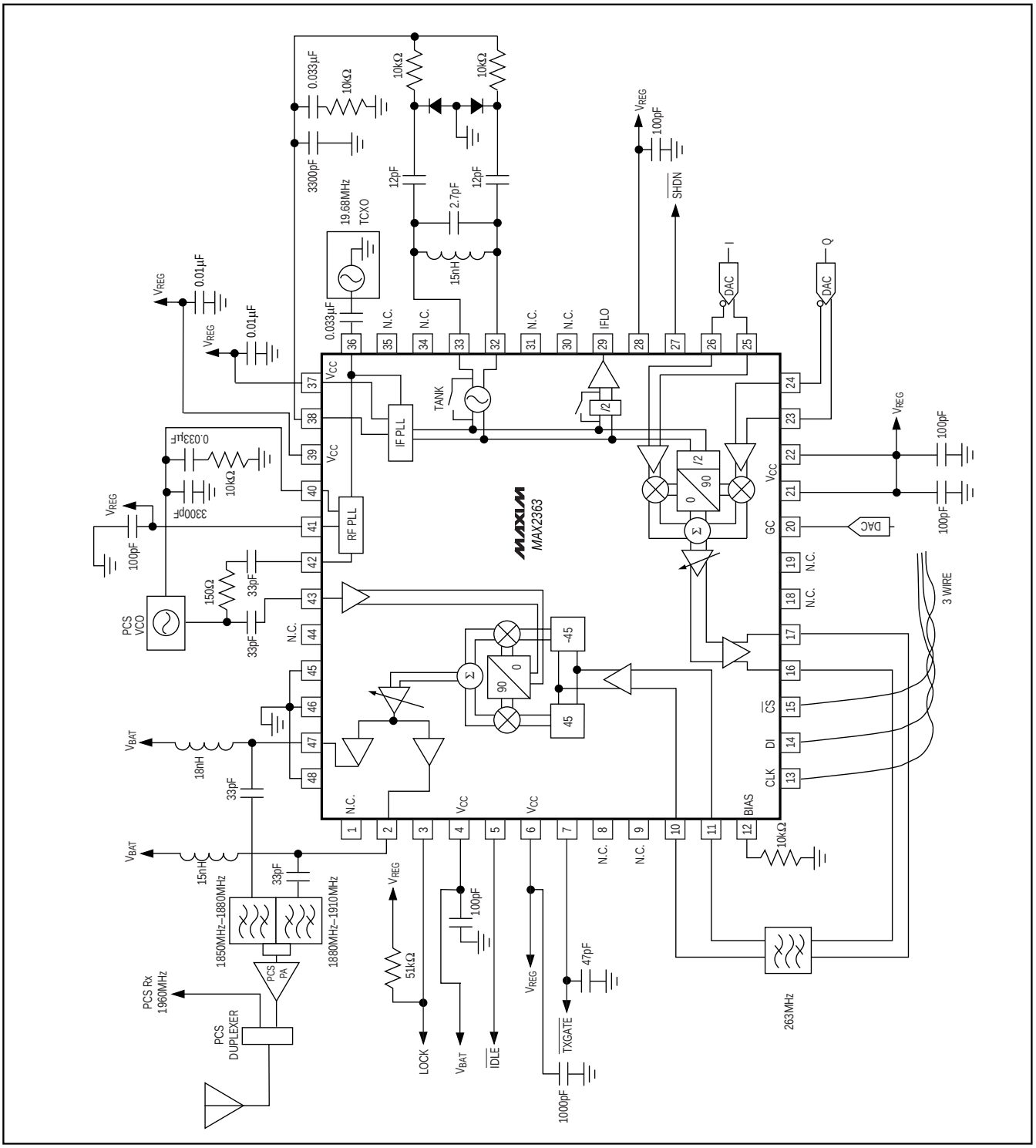


Figure 3. MAX2363 Typical Application Circuit

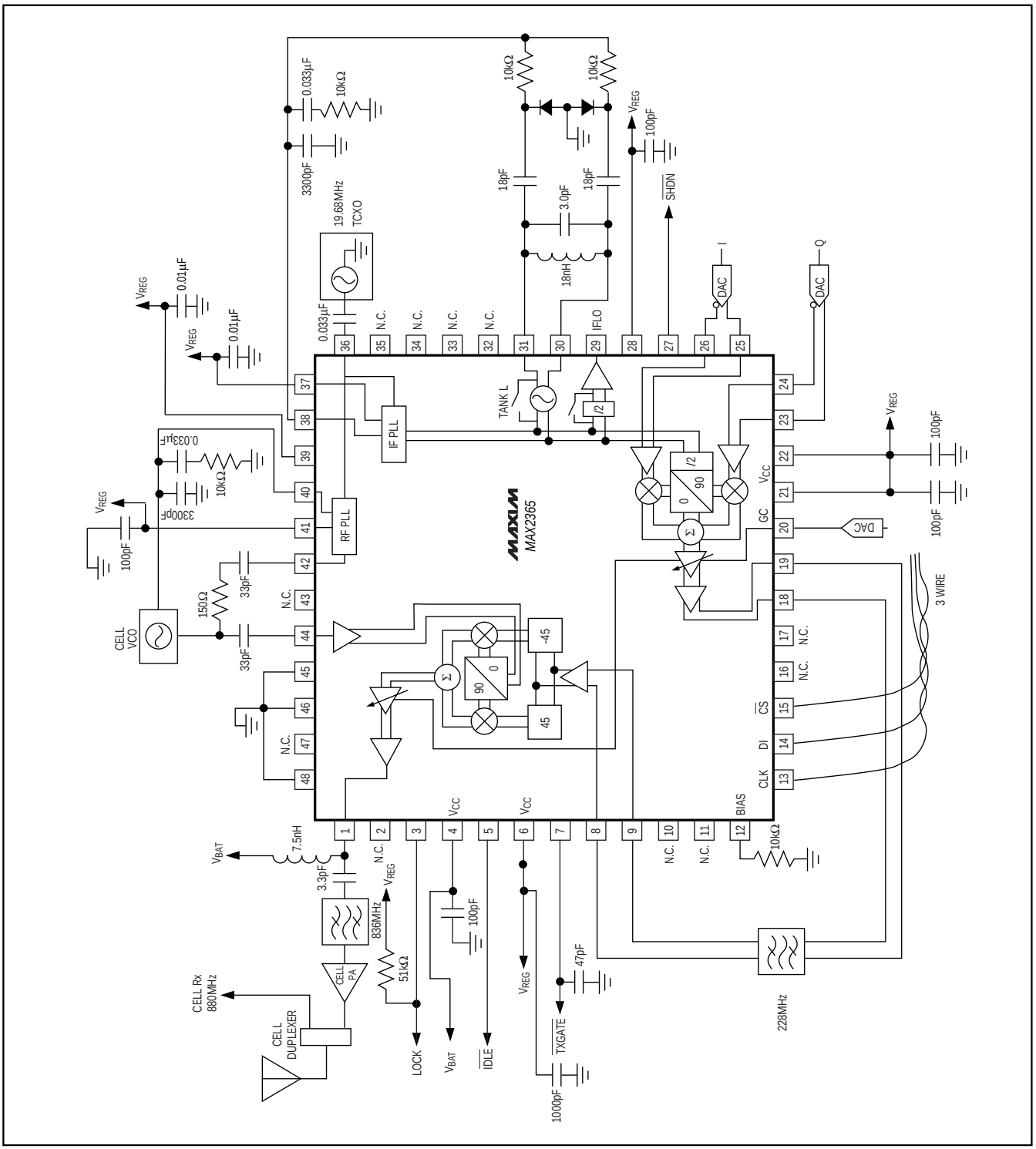


Figure 4. MAX2365 Typical Application Circuit

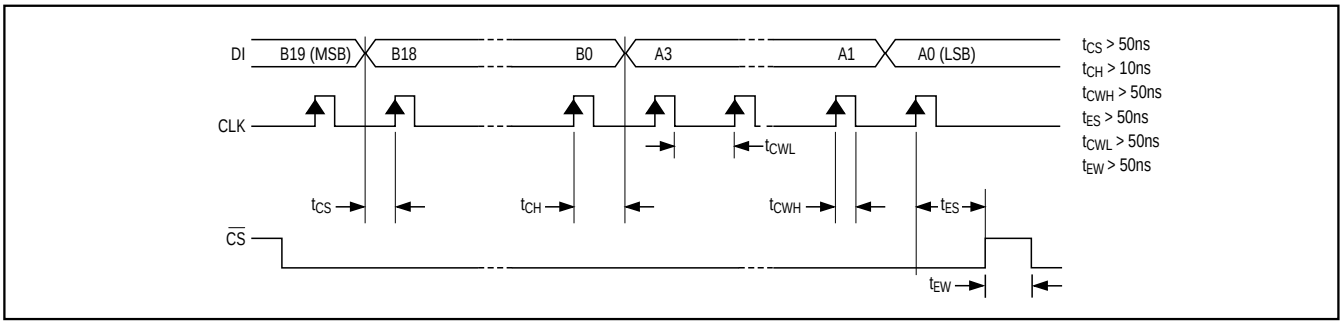


Figure 5. 3-Wire Interface Diagram

High-frequency bypass capacitors are required close to the pins with a dedicated via to ground. The 48-pin QFN-EP package provides minimal inductance ground by using an exposed paddle under the part. Provide at least five low-inductance vias under the paddle to ground, to minimize ground inductance. Use a solid ground plane wherever possible. Any cutout in the ground plane may act as slot radiator and reduce its shield effectiveness.

Keep the RF LO traces as short as possible to reduce LO radiation and susceptibility to interference.

IF Tank Design

The low-band tank (TANKL+, TANKL-) and high-band tank (TANKH+, TANKH-) are fully differential. The external tank components are shown in Figure 6. The frequency of oscillation is determined by the following equation:

$$f_{OSC} = \frac{1}{2\pi \sqrt{(C_{INT} + C_{CENT} + C_{VAR} + C_{PAR})\ L}}$$

$$C_{VAR} = \frac{C_D \times C_C}{2\ (C_D + C_C)}$$

C_{INT} = Internal capacitance of TANK port

C_D = Capacitance of varactor

C_{VAR} = Equivalent variable tuning capacitance

C_{PAR} = Parasitic capacitance due to PC board pads and traces

C_{CENT} = External capacitor for centering oscillation frequency

C_C = External coupling capacitor to the varactor

Table 10 shows possible component values for various oscillation frequencies.

Internal to the IC, the charge pump will have a leakage of less than 10nA. This is equivalent to a 300MΩ shunt resistor. The charge-pump output must see an extremely high DC resistance of greater than 300MΩ. This minimizes charge-pump spurs at the comparison frequency. Make sure there is no solder flux under the varactor or loop filter.

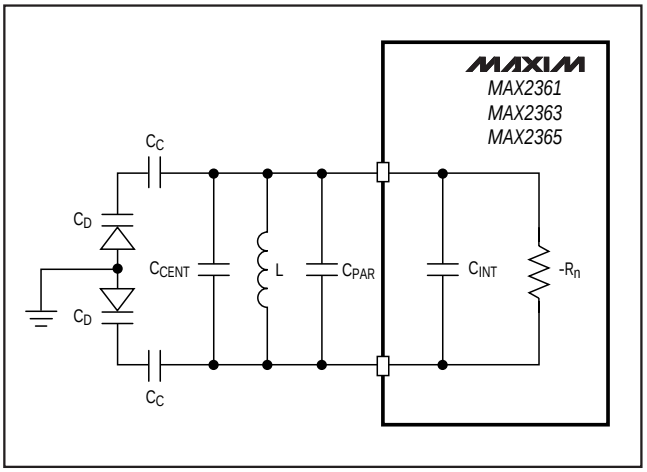


Figure 6. Tank Port Oscillator

Layout Issues

The MAX2361/MAX2363/MAX2365 EV kit can be used as a starting point for layout. For best performance, take into consideration power-supply issues as well as the RF, LO, and IF layout.

Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the MAX2361/MAX2363/MAX2365 circuit. At the end of each trace is a bypass capacitor with impedance to ground less than 1Ω at the frequency of interest. This arrangement pro-

Table 10. Suggested Component Values for the IF Oscillators

	OSC. FREQ. (MHz)	L (nH)	C_{CENT} (pF)	C_C (pF)	C_D
TANKL	260.76	39	2.4	18	SMV1763-079
	400.0	30	3.3	18	SMV1763-079
	457.2	18	3.0	18	SMV1763-079
TANKH	330.0	22	4.3	12	SMV1763-079
	527.2	15	2.7	12	SMV1763-079
	760.0	11	1.2	9	SMV1763-079

Table 11. Cascaded TDMA Performance

(From I/Q input to PA driver output, IQ_LEVEL = 0, $V_{I\_} = V_{Q\_} = 104mV_{RMS}$, IS136 NADC modulation or $415mV_{P-P}$ differential with 0.1% 3dB peak-average ratio.)

PARAMETER	CONDITION	VALUE	UNITS
IFL Frequency	IF_SEL = 0	228.6	MHz
IFH Frequency	IF_SEL = 1	263.6	MHz
RFL Frequency Range		824–849	MHz
RFH0 Frequency Range		1850–1910	MHz
LOL Frequency Range		1052.6–1077.6	MHz
LOH Frequency Range		2113.6–2173.6	MHz
LO Input Level	LOL or LOH	-7	dBm
RFL Output Power	V_{GC} = 2.4V, MPL = 0	+7	dBm
	V_{GC} = 2.4V, MPL = 1	+10	
RFH0 Output Power	V_{GC} = 2.4V, MPL = 0	+6	dBm
	V_{GC} = 2.4V, MPL = 1	+10	
Adjacent Channel Power Ratio	f_{OFFSET} = ±30kHz in 25kHz BW	-33	dBc
Alternate Channel Power Ratio	f_{OFFSET} = ±60kHz in 25kHz BW	-52	dBc
Receive Band Noise Power	MPL = 0, P_{RFH0} = +6dBm, f_{RFH0} = 1910MHz, measured at 1930MHz	-134	dBm/Hz
	MPL = 1, P_{RFH0} = +10dBm, f_{RFH0} = 1910MHz, measured at 1930MHz	-131	
	MPL = 0, P_{RFL} = +7dBm, f_{RFL} = 849MHz, measured at 869MHz	-134	
	MPL = 1, P_{RFL} = +10dBm, f_{RFL} = 849MHz, measured at 869MHz	-131	

Table 12. Cascaded WCDMA Performance.

(From I/Q input to PA driver output, IQ_LEVEL = 1, $V_{I\_}$ = $V_{Q\_}$ = 146mV_{RMS}, uplink 3GPP modulation or 600mVp-p differential with 0.1% 3.25dB peak-average ratio.)

PARAMETER	CONDITIONS	VALUE	UNITS
Intermediate Frequency	IF_SEL = 1	380	MHz
RFH0 Frequency Range		1920–1980	MHz
LOH Frequency Range		2300–2360	MHz
LO Input Level	LOH	-7	dBm
Maximum RFH0 Output Power	V_{GC} = 2.4V, MPL = 1	8	dBm
Minimum RFH0 Output Power	ZERO_BIAS = 1, SNR = 20dB	-75	dBm
Zero Bias Gain Step	From ZERO_BIAS = 1 to ZERO_BIAS = 0, V_{GC} = 2.0V	27	dB
Adjacent Channel Power Ratio	f_{OFFSET} = ±3.5MHz in 30kHz BW	-60	dBc
	f_{OFFSET} = ±5MHz in 3.84MHz BW	-45	
	f_{OFFSET} = ±10MHz in 3.84MHz BW	-58	
Receive Band Noise Power	MPL= 1, P_{RFH0} = +8dBm, f_{RFH0} = 1950MHz, measured at 2140MHz	-134	dBm/Hz

vides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Also, connect the exposed paddle to PC board GND with multiple vias to provide the lowest inductance possible.

Matching Network Layout

The layout of a matching network can be very sensitive to parasitic circuit elements. To minimize parasitic inductance, keep all traces short and place components as close to the IC as possible. To minimize parasitic capacitance, a cutout in the ground plane (and any other planes) below the matching network components can be used.

On the high-impedance ports (e.g., IF inputs and outputs), keep traces short to minimize shunt capacitance.

Tank Layout

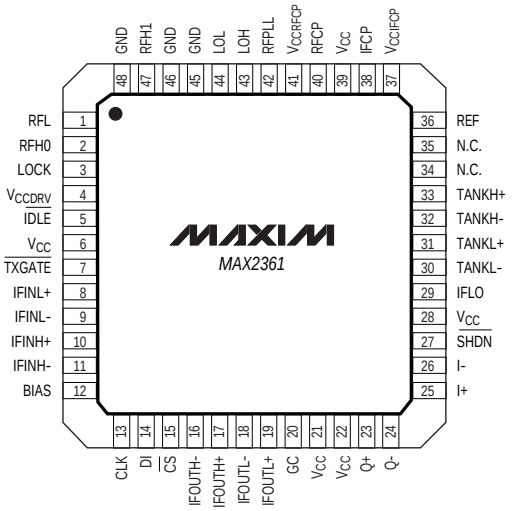
Keep the traces coming out of the tank short to reduce series inductance and shunt capacitance. Keep the inductor pads and coupling capacitor pads small to minimize stray shunt capacitance.

Selector Guide

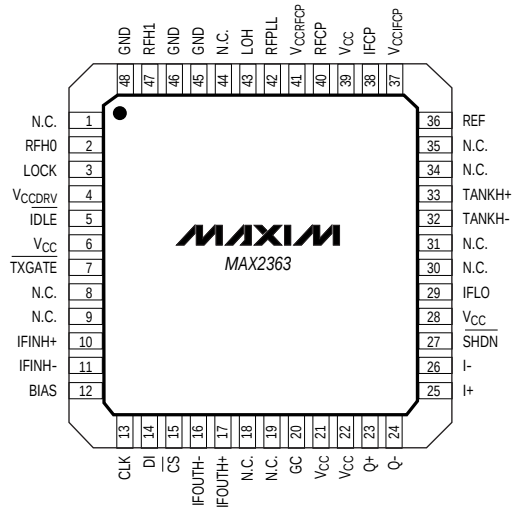
PART	IF RANGE (MHz)	RF LO RANGE (MHz)	RF RANGE (MHz)
MAX2361	120 to 235	800 to 1150	800 to 1000
	120 to 380	1400 to 2360	1700 to 2000
MAX2363	120 to 380	1400 to 2360	1700 to 2000
MAX2365	120 to 235	800 to 1150	800 to 1000

Pin Configurations

TOP VIEW



(T) QFN-EP



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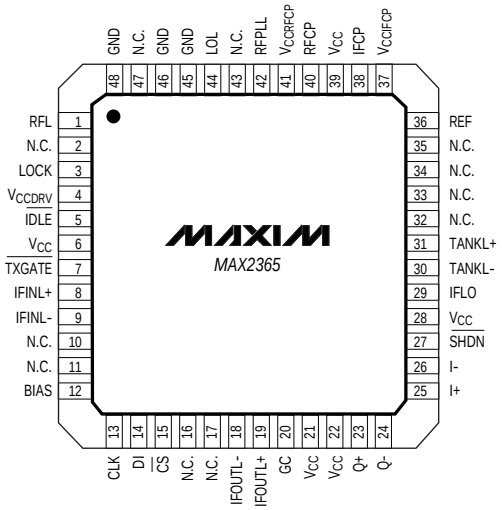


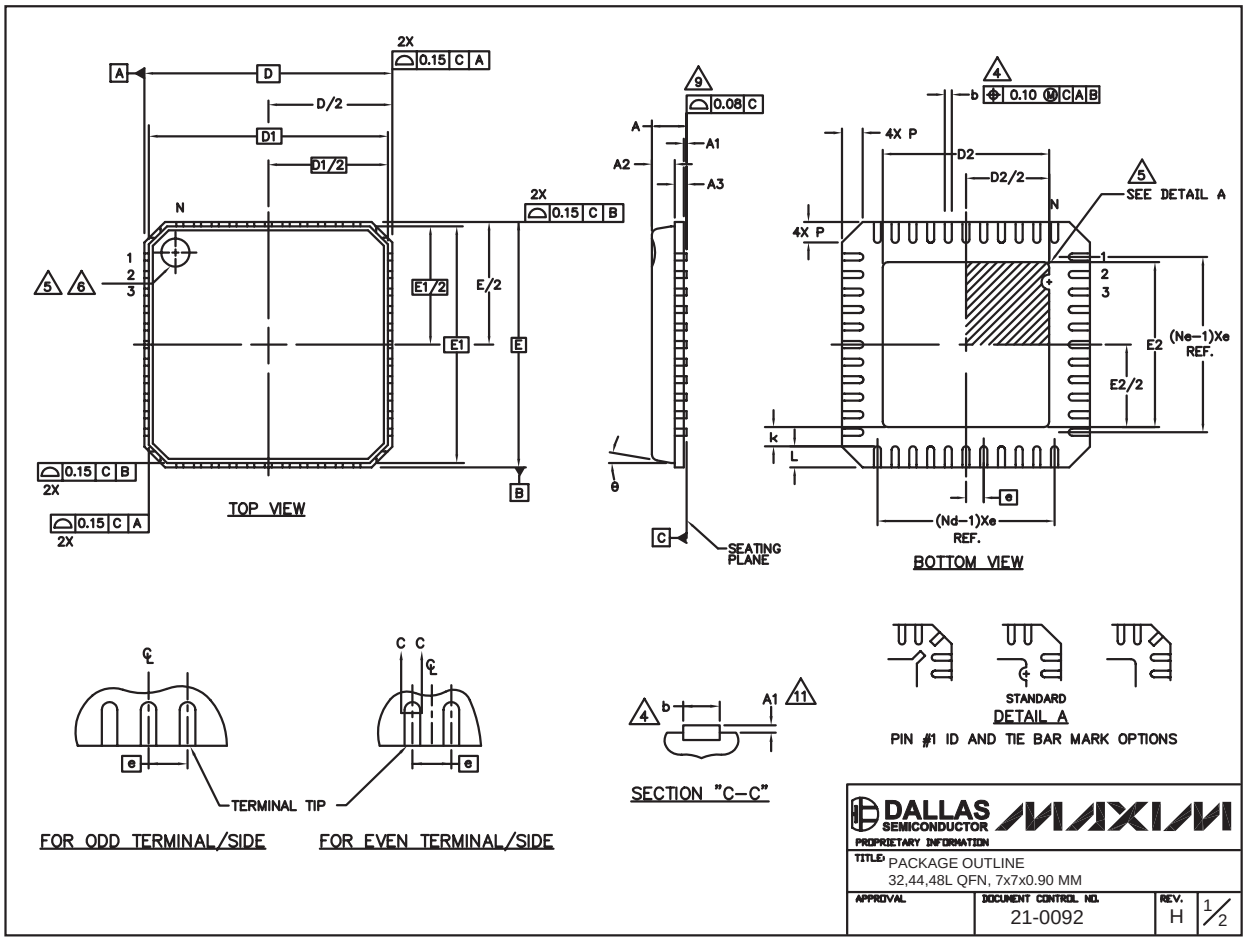
EXPOSED-PADDLE GND

(T) QFN-EP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



Complete Dual-Band Quadrature Transmitters

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG	32L 7x7			44L 7x7			48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF		
b	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
D1	6.75 BSC			6.75 BSC			6.75 BSC		
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E1	6.75 BSC			6.75 BSC			6.75 BSC		
e	0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	32			44			48		
Nd	8			11			12		
Ne	8			11			12		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
U	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G3277-2	4.55	4.70	4.85	4.55	4.70	4.85
G4477-1	3.65	3.80	3.95	3.65	3.80	3.95
G4477-2	4.55	4.70	4.85	4.55	4.70	4.85
G4477-3	3.15	3.30	3.45	3.15	3.30	3.45
G4877-1	4.95	5.10	5.25	4.95	5.10	5.25
G4877-2	5.45	5.60	5.75	5.45	5.60	5.75

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.08mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220 EXCEPT DIMENSION "b" MINIMUM.
11. APPLY ONLY FOR TERMINAL.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION(STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

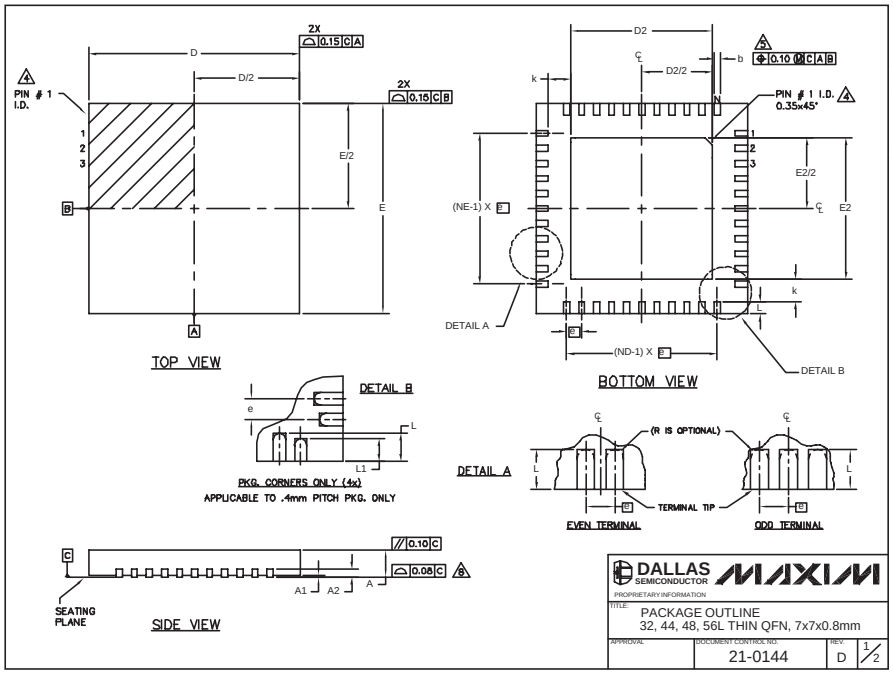
TITLE: PACKAGE OUTLINE, 32,44,48L QFN, 7x7x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0092	H	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0144 | REV. D | 1/2

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-1	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T4477-1	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-2	–	5.46	5.60	5.63	5.46	5.60	5.63	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.45	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T3277–1; T4877–1/–2/–3/–4/–5/–6 & T5677–1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0144 | REV. D | 2/2

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