Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE}) 7.5V
All Other Pins ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration ..... Continuous
(Short to Either Supply)
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
6-Bump UCSP (derate 3.9mW/°C above +70°C) 308mW
6-Pin SOT23 (derate 7.1mW/°C Above + 70°C) 571mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C) 330mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
14-Pin SO (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Range
MAX432_E__ ..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Bump Reflow Temperature ..... +235°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—T_A = +25°C

(V_{CC} = 5.0V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, R_L connected to V_{CC}/2, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} or V_{CC}	MAX432_ESA/ MAX4327ESD			±0.7	±2.0	mV
			All other packages			±1.2	±2.50	
Input Bias Current	I_B	V_{CM} = V_{EE} or V_{CC}				±50	±150	nA
Input Offset Current	I_{OS}	V_{CM} = V_{EE} or V_{CC}				±1	±12	nA
Differential Input Resistance	R_{IN}	-1.5V < V_{DIFF} < +1.5V				500		kΩ
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test			V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ V_{CC}	MAX432_ESA/ MAX4327ESD		62	94		dB
			All other packages		60	91		
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.4V to 6.5V			66	100		dB
Output Resistance	R_{OUT}	A_V = +1V/V				0.1		Ω
Large-Signal Voltage Gain	A_V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ				106		dB
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω			70	86		
Output Voltage Swing	V_O	MAX4322/ MAX4323	R_L = 100kΩ	V_{CC} - V_{OH}		12		mV
				V_{OL} - V_{EE}		20		
			R_L = 250Ω	V_{CC} - V_{OH}		200	300	
				V_{OL} - V_{EE}		100	200	
		MAX4326/ MAX4327/ MAX4329	R_L = 100kΩ	V_{CC} - V_{OH}		15		
				V_{OL} - V_{EE}		25		
			R_L = 250Ω	V_{CC} - V_{OH}		220	350	
				V_{OL} - V_{EE}		120	250	
Output Short-Circuit Current	I_{SC}					50		mA
$\overline{SHDN}$ Logic Threshold	V_{IL}	MAX4323/MAX4327		Low			0.8	V
	V_{IH}			High	2.0			
$\overline{SHDN}$ Input Current		MAX4323/MAX4327				±1	±4	µA

DC ELECTRICAL CHARACTERISTICS—T_A = +25°C (continued)

(V_{CC} = 5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, R_L connected to V_{CC}/2, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Inferred from PSRR test		2.4		6.5	V
Supply Current per Amplifier	I_{CC}	V_{CM} = V_{OUT} = V_{CC}/2	V_{CC} = 2.4V		650		µA
			V_{CC} = 5V		725	1100	
Shutdown Supply Current per Amplifier	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ ≤ 0.8V, MAX4323/MAX4327	V_{CC} = 2.4V		25		µA
			V_{CC} = 5V		40	60	

DC ELECTRICAL CHARACTERISTICS—T_A = -40°C to +85°C

(V_{CC} = 5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, R_L connected to V_{CC}/2, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} or V_{CC}	MAX432_ESA/ MAX4327ESD				±3.0	mV
			All other packages				±6.0	
Input Offset Voltage Tempco	TCV_{OS}					±2		µV/°C
Input Bias Current	I_B	V_{CM} = V_{EE} or V_{CC}					±180	nA
Input Offset Current	I_{OS}	V_{CM} = V_{EE} or V_{CC}					±20	nA
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test			V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ V_{CC}	MAX432_ESA/ MAX4327ESD		59			dB
			All other packages		54			
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.4V to 6.5V			62			dB
Large-Signal Voltage Gain	A_V	V_{OUT} = 0.4V to 4.6V, R_L = 250Ω			66			dB
Output Voltage Swing	V_O	MAX4322/ MAX4323	R_L = 250Ω	V_{CC} - V_{OH}			350	mV
				V_{OL} - V_{EE}			250	
		MAX4326/ MAX4327/ MAX4329	R_L = 250Ω	V_{CC} - V_{OH}			400	
				V_{OL} - V_{EE}			300	
$\overline{SHDN}$ Logic Threshold	V_{IL}	MAX4323/MAX4327		Low			0.8	V
	V_{IH}			High	2.0			
$\overline{SHDN}$ Input Current		MAX4323/MAX4327					±5	µA
Operating Supply Voltage Range	V_{CC}				2.4		6.5	V
Supply Current per Amplifier	I_{CC}	V_{CM} = V_{OUT} = V_{CC}/2					1200	µA
Shutdown Supply Current per Amplifier	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ ≤ 0.8V, MAX4323/MAX4327					70	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{OUT} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

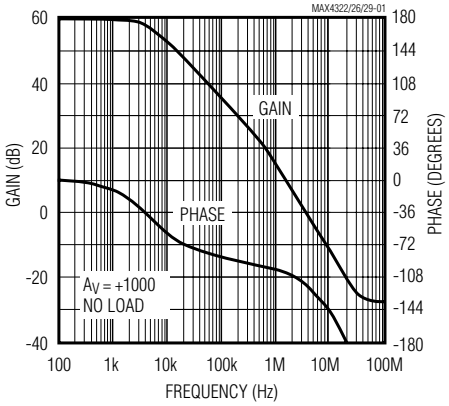
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP				5		MHz
Phase Margin	ϕ_M				64		Degrees
Gain Margin	G_M				12		dB
Total Harmonic Distortion	THD	f = 10kHz, V_{OUT} = $2V_{P-P}$, A_V = +1V/V			0.003		%
Slew Rate	SR				2		V/µs
Settling Time to 0.01%	t_S	A_V = +1V/V, V_{OUT} = 2V step			2.0		µs
Turn-On Time	t_{ON}	V_{CC} = 0 to 3V step			1		µs
$\overline{SHDN}$ Delay		MAX4323/MAX4327	Enable		1		µs
			Disable		0.2		
Input Capacitance	C_{IN}				3		pF
Input Noise-Voltage Density	e_n	f = 1kHz			22		nV/√Hz
Input Noise-Current Density	i_n	f = 1kHz			0.4		pA/√Hz
Amp-Amp Isolation					135		dB
Capacitive-Load Stability	C_L	A_V = +1V/V			250		pF

Note 1: All devices are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.

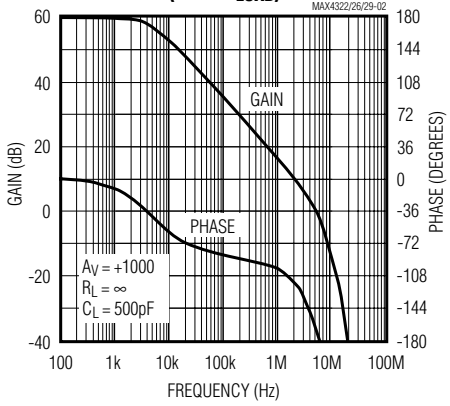
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

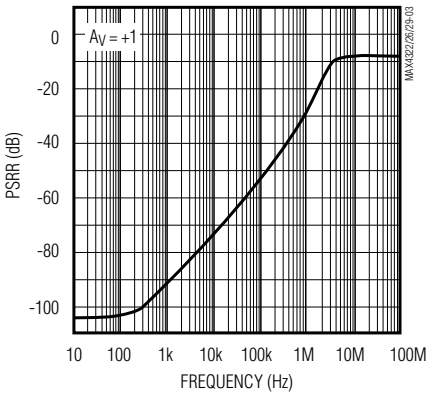
GAIN AND PHASE vs. FREQUENCY



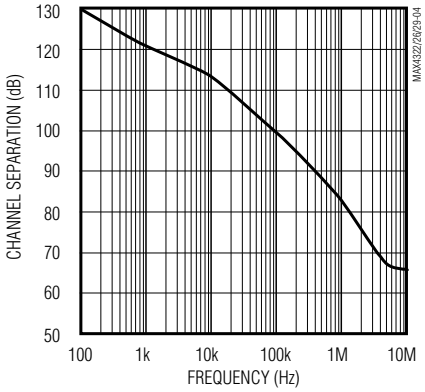
GAIN AND PHASE vs. FREQUENCY (WITH C_{LOAD})



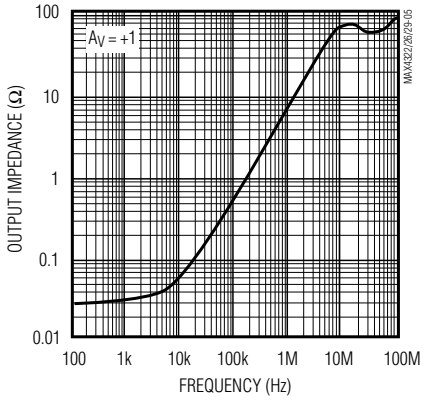
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



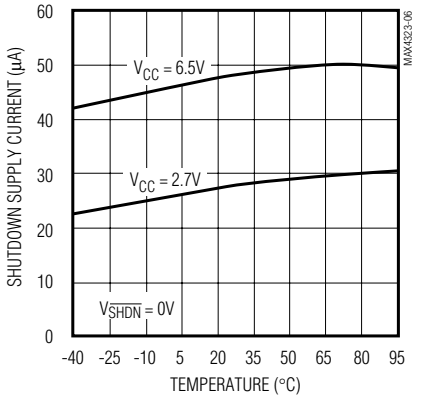
MAX4326/MAX4327/MAX4329 CHANNEL SEPARATION vs. FREQUENCY



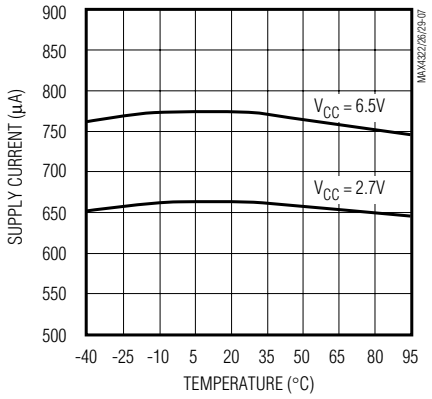
OUTPUT IMPEDANCE vs. FREQUENCY



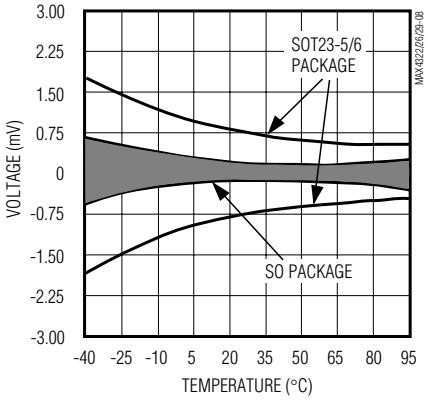
MAX4323/MAX4327 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



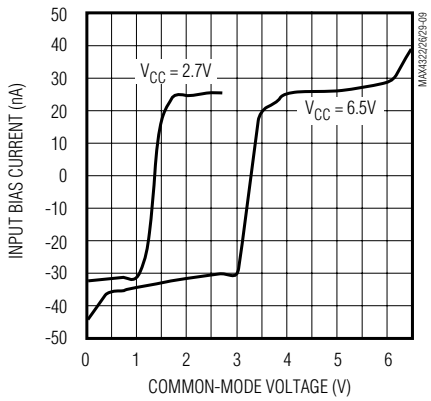
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE

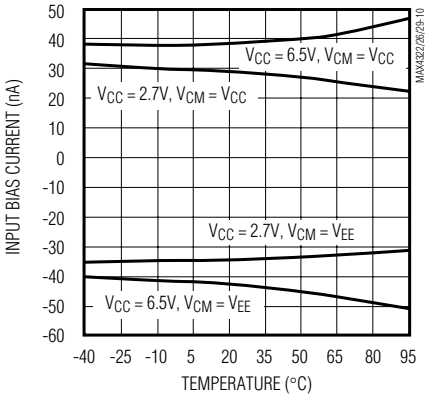


Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

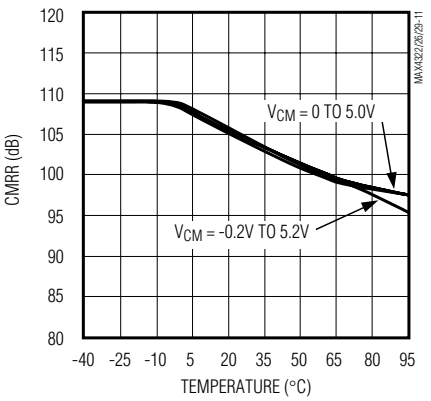
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

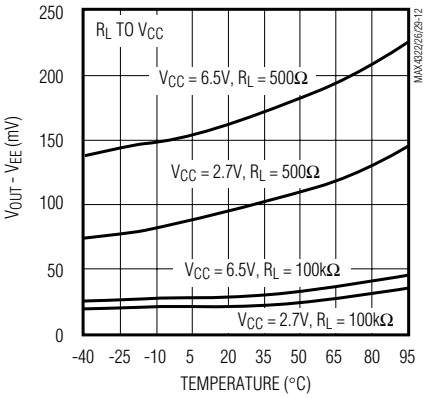
INPUT BIAS CURRENT vs. TEMPERATURE



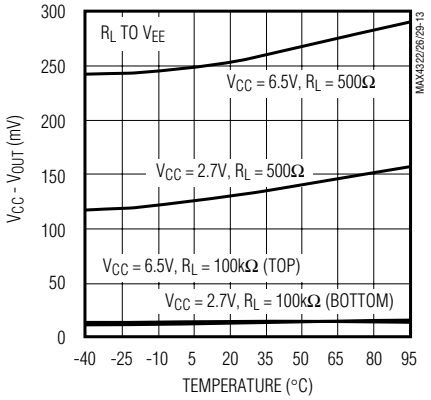
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



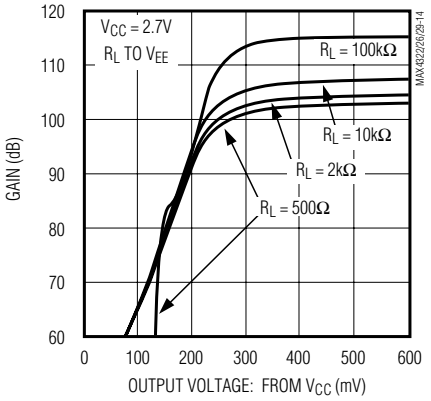
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



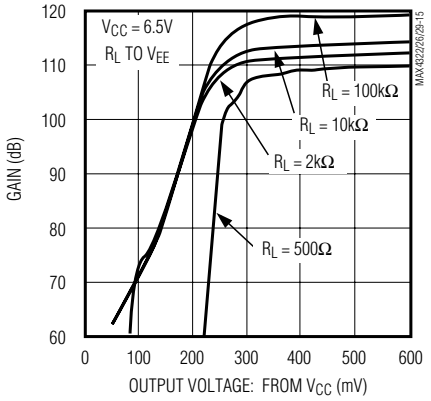
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



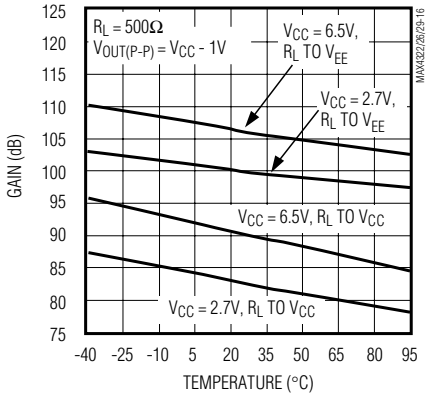
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



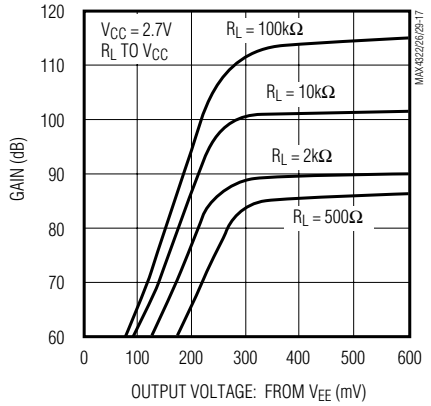
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



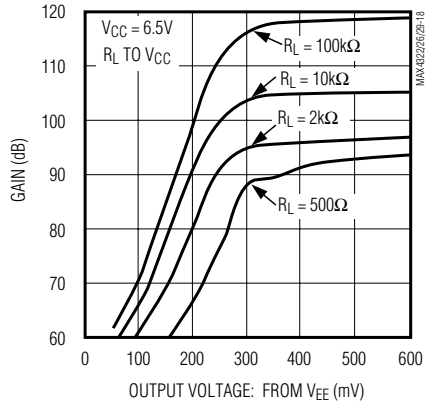
LARGE-SIGNAL GAIN vs. TEMPERATURE



LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



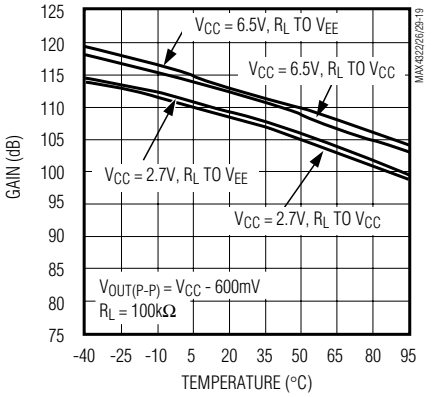
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



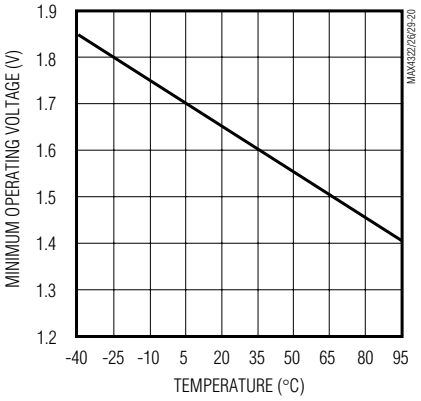
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

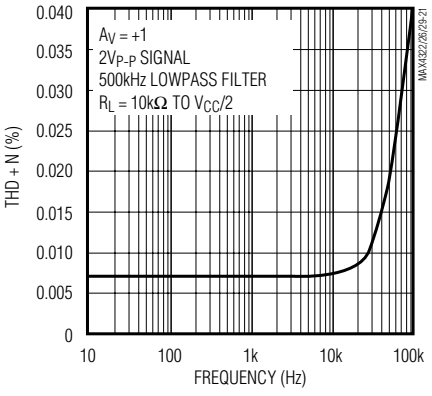
LARGE-SIGNAL GAIN vs. TEMPERATURE



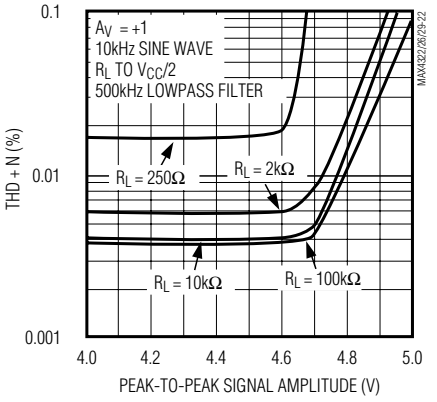
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



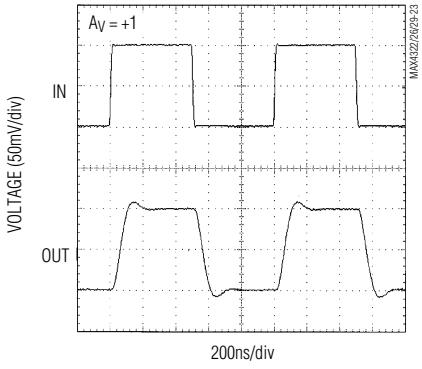
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



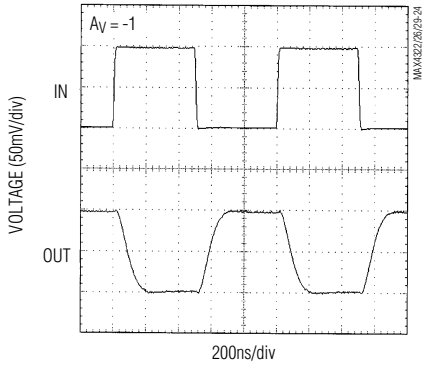
TOTAL HARMONIC DISTORTION PLUS NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



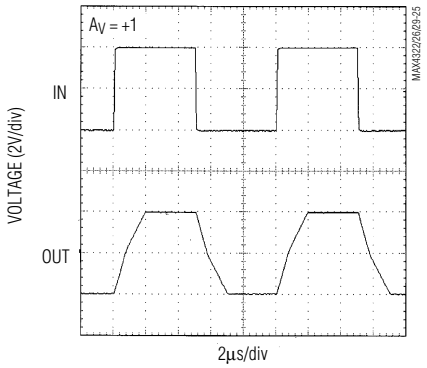
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



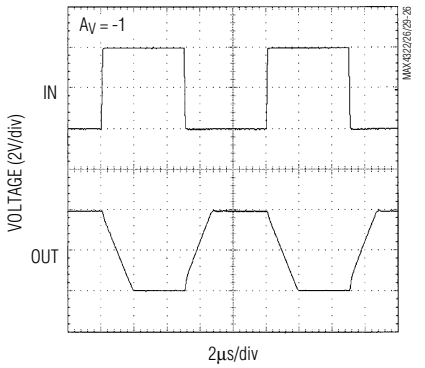
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Pin Description

PIN									NAME	FUNCTION
MAX4322		MAX4323			MAX4326	MAX4327		MAX4329		
SOT23	SO/µMAX	SOT23	SO/µMAX	UCSP		µMAX	SO			
1	6	1	6	A2	—	—	—	—	OUT	Output
2	4	2	4	A1	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	—	3	3	B1	—	—	—	—	IN+	Noninverting Input
4	—	4	2	B2	—	—	—	—	IN-	Inverting Input
5	7	6	7	A3	8	10	14	4	V_{CC}	Positive Supply
—	1, 5, 8	—	1, 5	—	—	—	5, 7, 8 , 10	—	N.C.	No Connection. Not internally connected.
—	—	5	8	B3	—		—	—	$\overline{SHDN}$	Shutdown Control. Connected high or leave floating to enable amplifier.
—	—	—	—	—	1, 7	1, 9	1, 13	1, 7	OUT1, OUT2	Outputs for Amps 1 and 2
—	2	—	—	—	2, 6	2, 8	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for Amps 1 and 2
—	3	—	—	—	3, 5	3, 7	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for Amps 1 and 2
—	—	—	—	—	—	5, 6	5, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown Control for Amps 1 and 2. Connected high or leave floating to enable amplifier.
—	—	—	—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amps 3 and 4
—	—	—	—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amps 3 and 4
—	—	—	—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amps 3 and 4

Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which combine to provide an input common-mode range extending to the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 250µV. The switchover transition region, which occurs near $V_{CC}/2$, has been extended to minimize the slight degradation in CMRR caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision, low-voltage, data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. To reduce the offset error caused by input bias currents flowing through external source impedances, match the effective impedance seen by each input (Figures 1a, 1b). High-source impedances, together with the input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves the response.

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329s' inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, the input resistance is typically 500kΩ. For differential input voltages greater than 1.8V, the input resistance is approximately 2kΩ, and the input bias current is determined by the following equation:

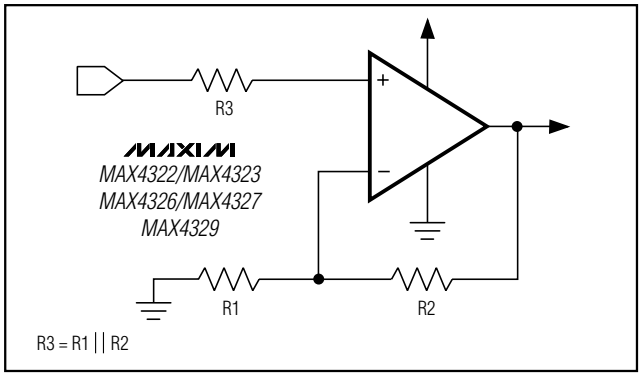


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

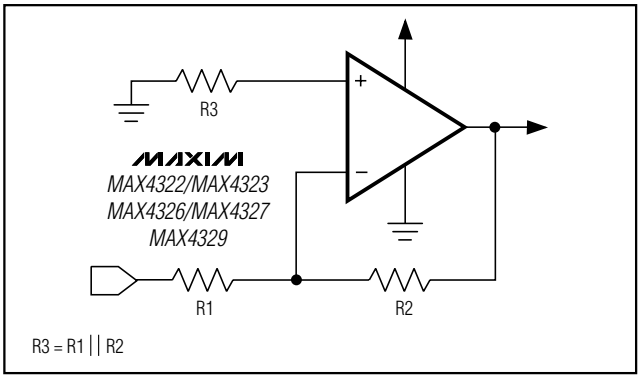


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

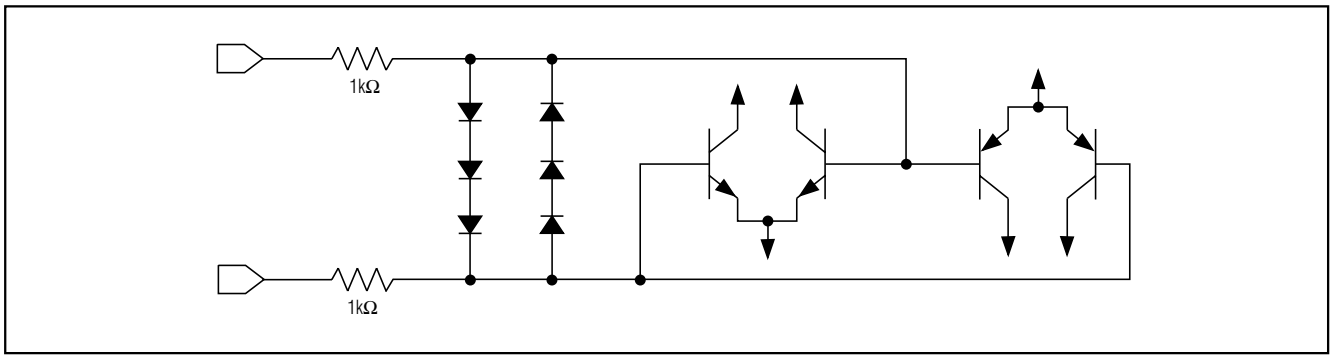


Figure 2. Input Protection Circuit

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

Rail-to-Rail Output Stage

The minimum output voltage is within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4322 connected as a voltage follower. With a 3V supply and the load tied to ground, the output swings from 0 to 2.90V. The maximum output voltage swing depends on the load, but is within 350mV of a 5V supply, even with the maximum load (500Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 500pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Power-Up and Shutdown Mode

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 amplifiers typically settle within 1µs after power-up.

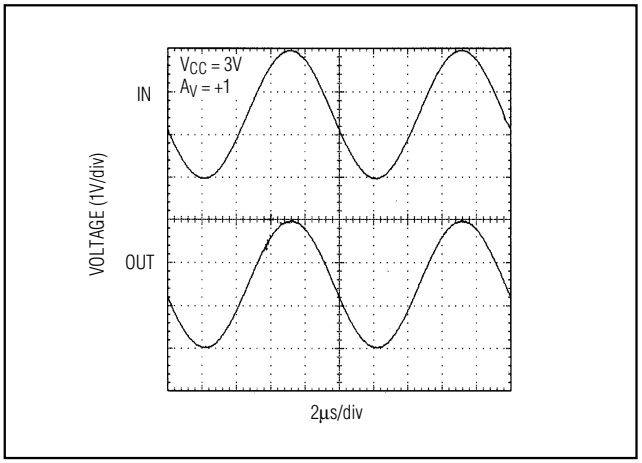


Figure 3. Rail-to-Rail Input/Output Voltage Range

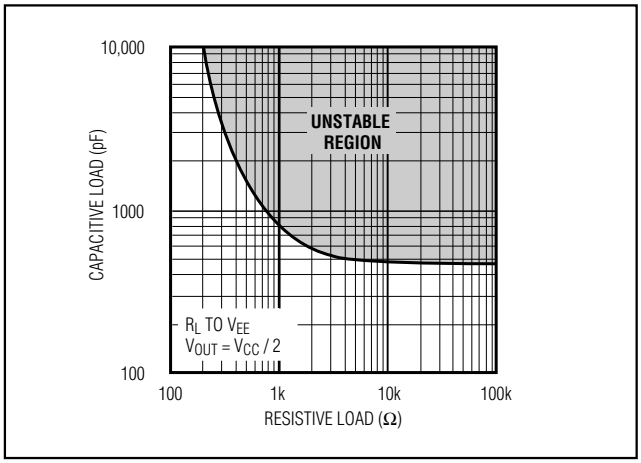


Figure 4. Capacitive-Load Stability

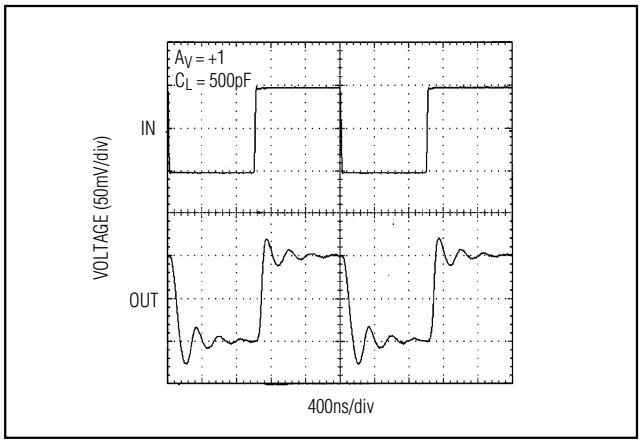


Figure 5. Small-Signal Transient Response with Capacitive Load

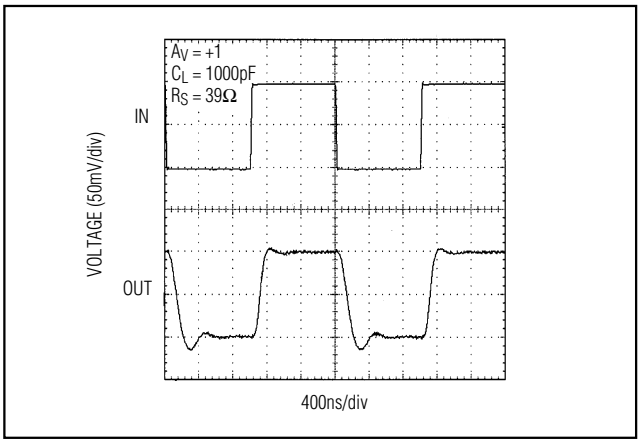


Figure 6. Transient Response to Capacitive Load with Isolation Resistor

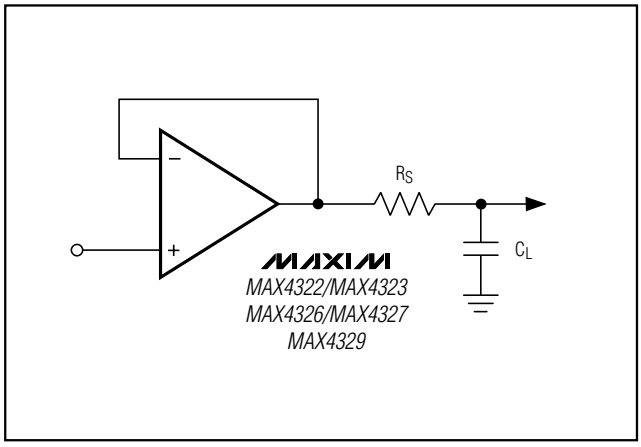


Figure 7. Capacitive-Load-Driving Circuit

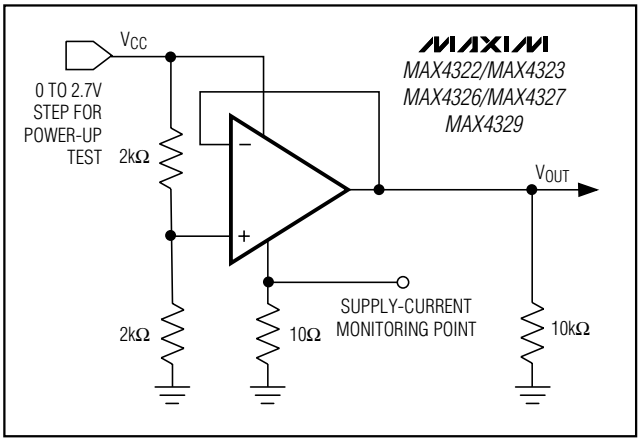


Figure 8. Power-Up Test Circuit

Figures 9 and 10 show the output voltage and supply current on power-up of the test circuit in Figure 8.

The MAX4323 and MAX4327 have a shutdown option. When shutdown ($\overline{SHDN}$) is pulled low, the supply current drops to 25µA per amplifier and the amplifiers are disabled with the outputs in a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating (1µA internal pullup) enables the amplifier. In the dual-amplifier MAX4327, the shutdown functions operate independently. Figures 11 and 12 show the output voltage and supply current responses of the MAX4323 to a shutdown pulse.

Power Supplies and Layout

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 operate from a single 2.4V to 6.5V power supply, or from dual supplies of ±1.2V to ±3.25V. For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor in parallel with at least 1µF. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths and resistor leads by placing external components close to the op amp.

UCSP Information

Layout Issues

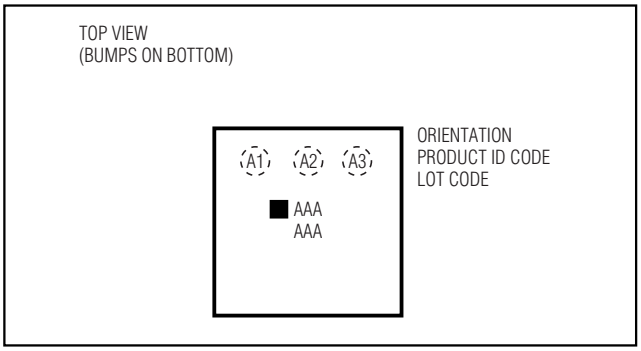
Design the layout for the device to be as compact as possible to minimize parasitics. The UCSP uses a bump pitch of 0.5mm (19.7mil) and a bump diameter of 0.33mm (~12mil). Therefore, lay out the solder-pad spacing on 0.5mm (19.7mil) centers, using a pad size of 0.25mm (~10mil) and a solder mask opening of 0.33mm (13mil). Round or square pads are permissible. Connect multiple vias from the ground plane as close to the ground connections as possible.

Install capacitors as close as possible to the device supply voltage input. Place the ground end of these capacitors near the ground plane to provide a low-impedance return path for the signal current.

Prototype Chip Installation

Alignment keys on the PC board, around the area where the chip is located, are helpful in the prototype assembly process. It is better to align the chip on the board before any other components are placed, and then place the board on a hot plate or hot surface until the solder starts melting. Remove the board from the hot plate without disturbing the position of the chip and let it cool down to room temperature before processing the board further.

MAX4323EBT (UCSP) Marking Information



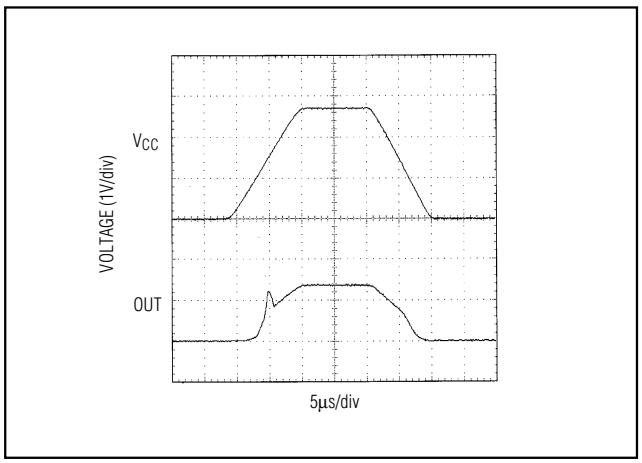


Figure 9. Power-Up Output Voltage

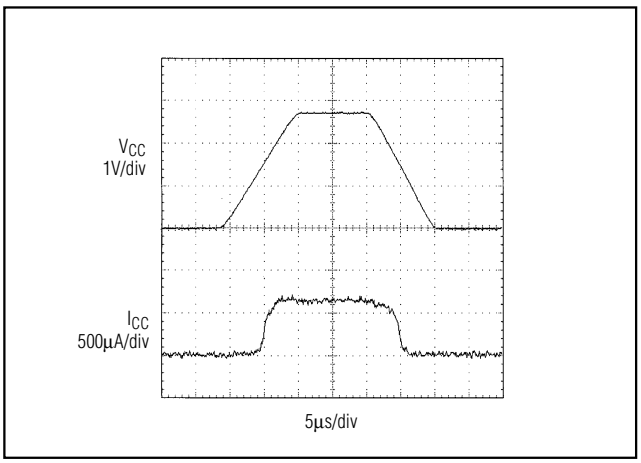


Figure 10. Power-Up Supply Current

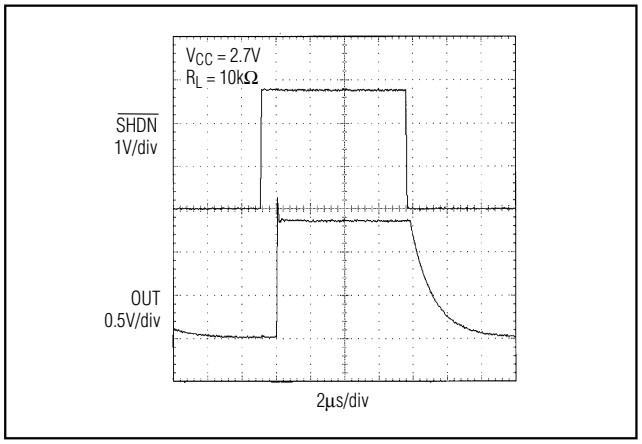


Figure 11. Shutdown Output Voltage

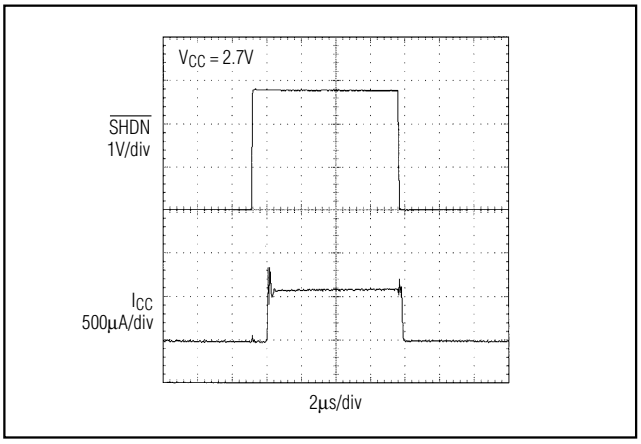
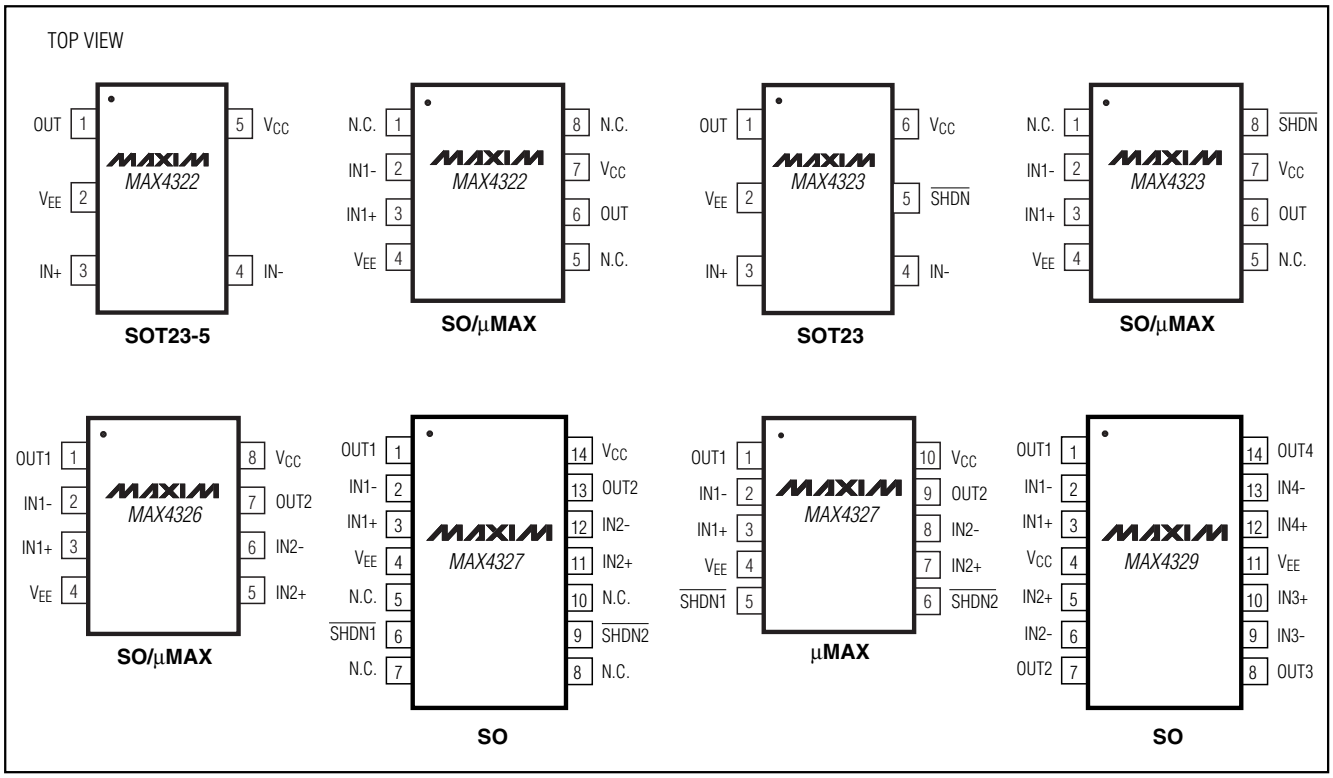


Figure 12. Shutdown Enable/Disable Supply Current

Pin Configurations (continued)



UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform as well as a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP.

Performance through operating-life test and moisture resistance remains uncompromised. The wafer-fabrication process primarily determines the performance. Mechanical stress performance is a greater consideration for UCSPs. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder-joint contact integrity must be considered. Comprehensive reliability tests have been performed and are available upon request. In conclusion, the UCSP performs reliably through environmental stresses.

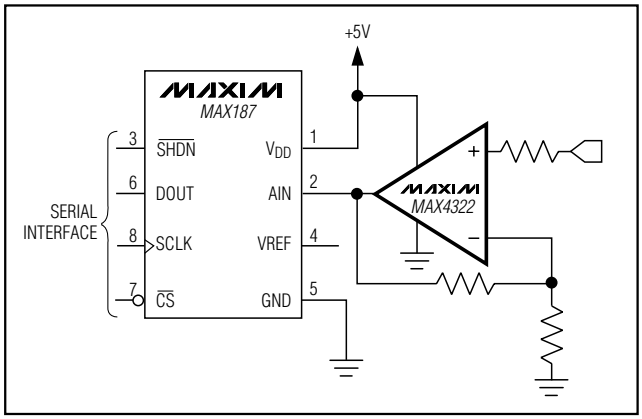
Ordering Information (continued)

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4323EBT-T*	-40°C to +85°C	6 UCSP-6	AAW
MAX4323EUT-T	-40°C to +85°C	6 SOT23-6	AAEC
MAX4323EUA	-40°C to +85°C	8 μMAX	—
MAX4323ESA	-40°C to +85°C	8 SO	—
MAX4326EUA	-40°C to +85°C	8 μMAX	—
MAX4326ESA	-40°C to +85°C	8 SO	—
MAX4327EUB	-40°C to +85°C	10 μMAX	—
MAX4327ESD	-40°C to +85°C	14 SO	—
MAX4329ESD	-40°C to +85°C	14 SO	—

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. See the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

Typical Operating Circuit



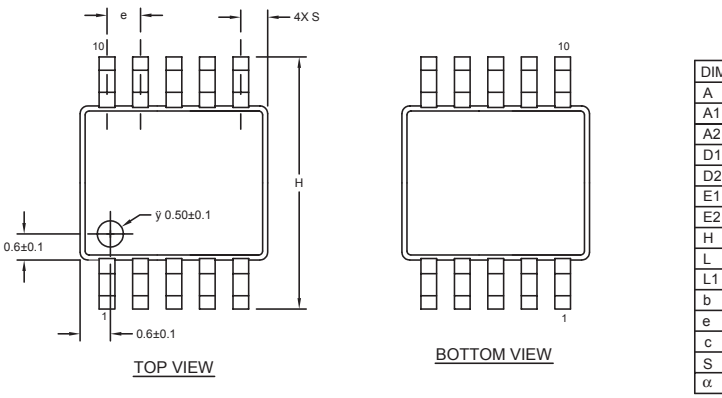
Chip Information

MAX4322 TRANSISTOR COUNT: 170
MAX4323 TRANSISTOR COUNT: 170
MAX4326 TRANSISTOR COUNT: 340
MAX4327 TRANSISTOR COUNT: 340
MAX4329 TRANSISTOR COUNT: 680
PROCESS: Bipolar
SUBSTRATE CONNECTED TO V_{EE}

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞

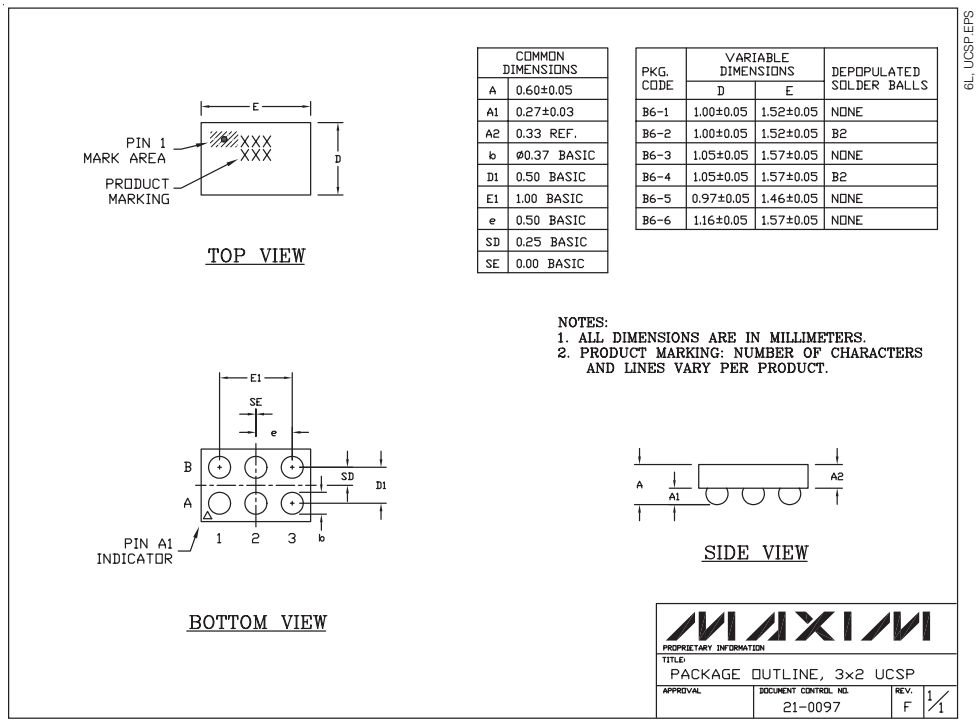
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP
APPROVAL | DOCUMENT CONTROL NO. 21-0061 | REV. I | 1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6L, UCSP.EPS

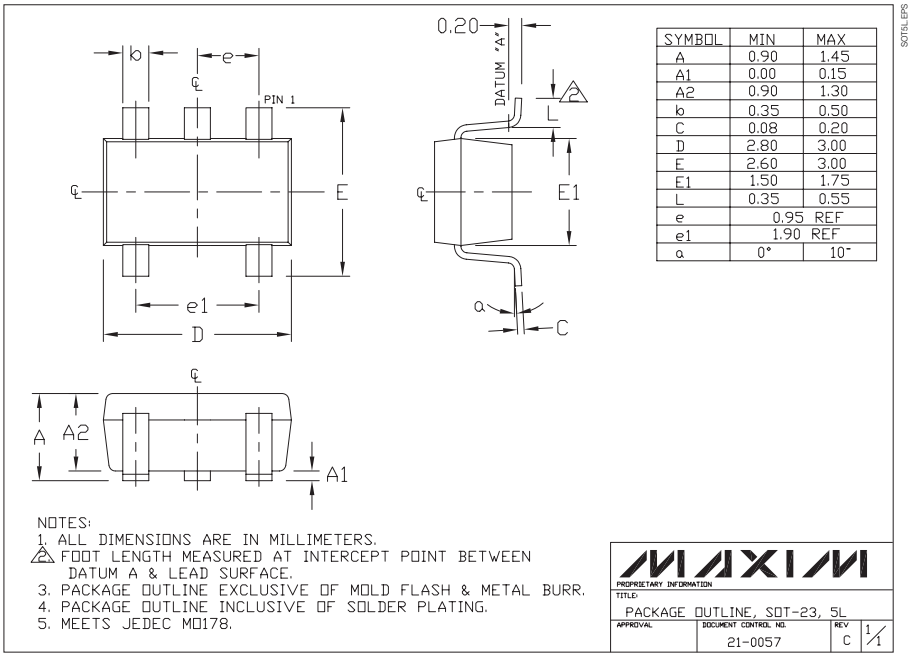


COMMON DIMENSIONS	
A	0.60±0.05
A1	0.27±0.03
A2	0.33 REF.
b	Ø0.37 BASIC
D1	0.50 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B6-1	1.00±0.05	1.52±0.05	NONE
B6-2	1.00±0.05	1.52±0.05	B2
B6-3	1.05±0.05	1.57±0.05	NONE
B6-4	1.05±0.05	1.57±0.05	B2
B6-5	0.97±0.05	1.46±0.05	NONE
B6-6	1.16±0.05	1.57±0.05	NONE

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

SOT5L.EPS



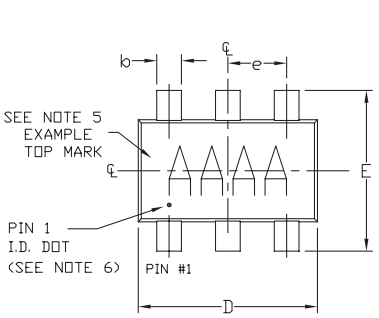
SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°

Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6LSOT.EPS

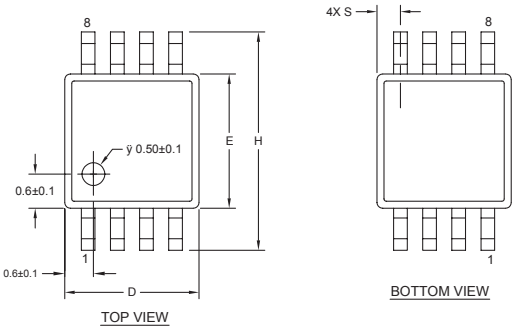


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT-23, 6L
APPROVAL | DOCUMENT CONTROL NO. 21-0058 | REV E | 1/1

8LUMAXD.EPS



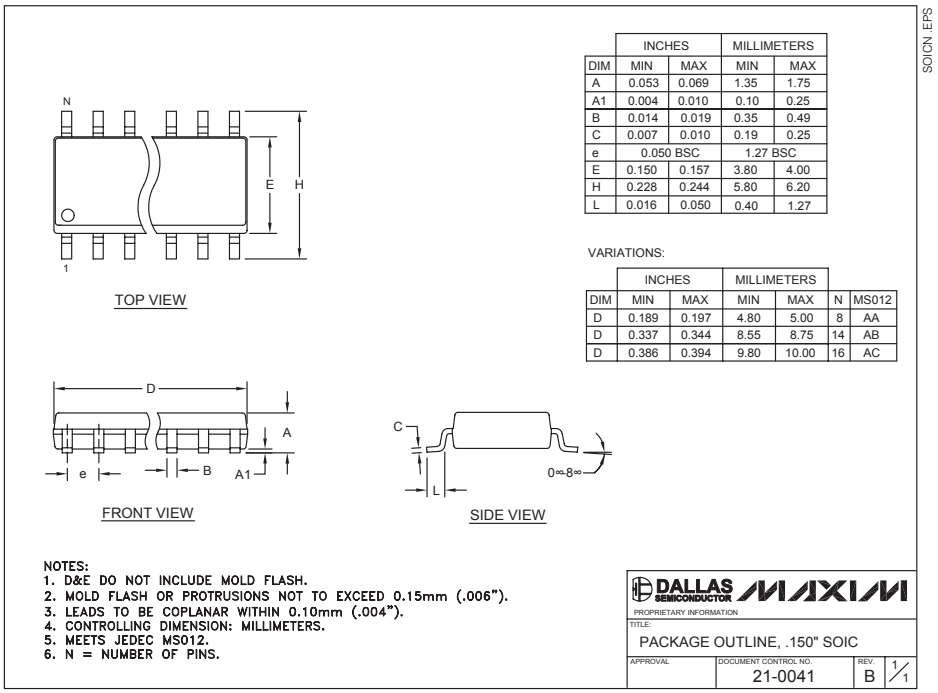
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV. J | 1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

Mouser Electronics

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