

1.3 General Parameters

The following general parameters apply to all part numbers described herein:

Core power supply:	2.0 V ± 100 mV dc (nominal; see Table 3 for recommended operating conditions)
I/O power supply	1.8 V ± 100 mV dc (processor bus interface only; not supported on L2 interface) or 2.0 V ± 100 mV dc (processor bus interface only; not supported on L2 interface) or 3.3 V ± 165 mV dc (input thresholds are configuration pin selectable)

Note that part revisions prior to Rev 2.8 (Rev E) do not support core voltages down to 1.8 V.

1.4.1 DC Electrical Characteristics

All part numbers affected by this specification support 3.3V and 1.8V/2.0V I/O voltages but do not support 2.5V I/O voltages. Table 2 describes the input threshold voltage settings. These settings apply to all device revisions prior to Rev. 2.8 (Rev E), including all part numbers described herein. Note that the MPC745 does not provide an L2 interface.

Table 2 Input Threshold Voltage Settings

BVSEL Signal	L2VSEL Signal	Processor Bus Interface Voltage	L2 Bus Interface Voltage
0	0	1.8V or 2.0V	1.8V or 2.0V
0	1	1.8V or 2.0V	3.3V
1	0	3.3V	1.8V or 2.0V
1	1	3.3V	3.3V

Caution: The input threshold selection must agree with the OVdd/L2OVdd voltages supplied.

Table 3 provides the recommended operating conditions for all device revisions prior to Rev. 2.8 (Rev E), including all part numbers described herein.

Table 3 Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	
Core supply voltage	Vdd	2.0 ± 100 mV	V	
PLL supply voltage	AVdd	2.0 ± 100 mV	V	
L2 DLL supply voltage	L2AVdd	2.0 ± 100 mV	V	
Processor bus supply voltage	BVSEL = 0	OVdd	1.8 ± 100 mV or 2.0 ± 100 mV	V
	BVSEL = 1	OVdd	3.3 ± 165 mV	V
L2 bus supply voltage	L2VSEL = 0	L2OVdd	1.8 ± 100 mV or 2.0 ± 100 mV	V
	L2VSEL = 1	L2OVdd	3.3 ± 165 mV	V

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 6 provides the DC electrical specifications for all device revisions prior to Rev. 2.8 (Rev E), including all part numbers described herein.

Table 6 DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage ¹	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8/2.0	V _{IH}	0.65 * (L2)OVdd	(L2)OVdd + 0.3	V	2,3
	3.3	V _{IH}	2.0	(L2)OVdd + 0.3	V	2,3
Input low voltage (all inputs except SYSCLK)	1.8/2.0	V _{IL}	-0.3	0.35 * (L2)OVdd	V	2
	3.3	V _{IL}	-0.3	0.8	V	
SYSCLK input high voltage	1.8/2.0	KV _{IH}	1.5	OVdd + 0.3	V	
	3.3	KV _{IH}	2.4	OVdd + 0.3	V	
SYSCLK input low voltage	1.8/2.0	KV _{IL}	-0.3	0.2	V	
	3.3	KV _{IL}	-0.3	0.4	V	
Output high voltage, I _{OH} = -6 mA	1.8/2.0	V _{OH}	(L2)OVdd - 0.45	—	V	
	3.3	V _{OH}	2.4	—	V	
Output low voltage, I _{OL} = 6 mA	1.8/2.0	V _{OL}	—	0.45	V	
	3.3	V _{OL}	—	0.4	V	

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OVdd. L2OVdd is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.

1.4.2.2 Processor Bus AC Specifications

All part numbers described herein have slower AC timing characteristics than later revisions of the part. The affected processor bus AC timing specifications are given in Table 10.

Table 10 Processor Bus AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbols	300, 350, 400 MHz		Unit
		Min	Max	
Input Hold Times: All Inputs	t _{IXKH}	0.6	—	ns
Valid Times: All Outputs	t _{KHOV}	—	4.5	ns

1.4.2.4 L2 Bus AC Specifications

The AC timing characteristics of the L2 bus interface in 3.3V mode are slower for parts affected by this specification than for later revisions of the part. Additionally, the AC timing of the L2 interface is not guaranteed in 1.8V/2.0V mode. These affect the following part numbers only:

- XPC755BRX300LD
- XPC755BRX350LD
- XPC755BRX400LD
- XPC755BPX300LD
- XPC755BPX350LD
- XPC755BPX400LD

Table 12 provides the L2 bus interface AC timing specifications for the MPC755 described in this Part Number Specification when the L2 bus interface is in 3.3V mode only. The L2 bus interface of the part described herein is not tested in 1.8V/2.0V mode and does not meet these specifications. The L2 interface output drivers display a non-linear, stepped behavior when switching that prolongs the rise and fall times in this mode. This delay is typically on the order of 2 ns but is not guaranteed. Freescale does not recommend or support the use of the L2 bus interface of the affected part numbers described herein in 1.8V/2.0V mode.

Table 12 L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	300 MHz		350 MHz		400 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Setup Times: Data and parity	t_{DVL2CH}	1.5	—	1.5	—	1.5	—	ns	2
Input Hold Times: Data and parity	t_{DXL2CH}	0.5	—	0.5	—	0.5	—	ns	2
Valid Times:	t_{L2CHOV}								
All outputs when L2CR[14-15] = 00		-	3.6	-	3.6	-	3.6		
All outputs when L2CR[14-15] = 01		-	3.8	-	3.8	-	3.8		
All outputs when L2CR[14-15] = 10		-	4.0	-	4.0	-	4.0		
All outputs when L2CR[14-15] = 11		-	4.2	-	4.2	-	4.2		
L2SYNC_IN to high impedance:	t_{L2CHOZ}								
All outputs when L2CR[14-15] = 00		-	3.5	-	3.5	-	3.5		
All outputs when L2CR[14-15] = 01		-	4.0	-	4.0	-	4.0		
All outputs when L2CR[14-15] = 10		-	4.2	-	4.2	-	4.2		
All outputs when L2CR[14-15] = 11		-	4.5	-	4.5	-	4.5		

Notes:
See General specifications.

1.10 Ordering Information

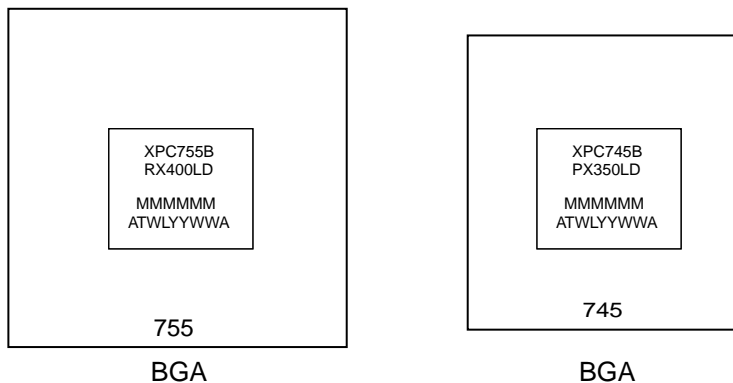
Table B provides the ordering information for the MPC755 part described in this Part Number Specification.

Table B. Ordering Information for the MPC755 Microprocessor

Package Type	Device Rev	Process	Mask Code	CPU Frequency (MHz)	Freescale Part Number
360 CBGA	2.7	HIP4DP	57K76D	300MHz	XPC755BRX300LD
				350MHz	XPC755BRX350LD
				400MHz	XPC755BRX400LD
360 PBGA	2.7	HIP4DP	57K76D	300MHz	XPC755BPX300LD
				350MHz	XPC755BPX350LD
				400MHz	XPC755BPX400LD
255 PBGA	2.7	HIP4DP	57K76D	300MHz	XPC745BPX300LD
				350MHz	XPC745BPX350LD

1.10.1 Part Marking

Parts are marked as the examples shown in Figure A.



Notes:

MMMMMM is the 6-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. (This space is left blank if parts are assembled in the United States.)

Figure A. Freescale Part Marking for BGA Device

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