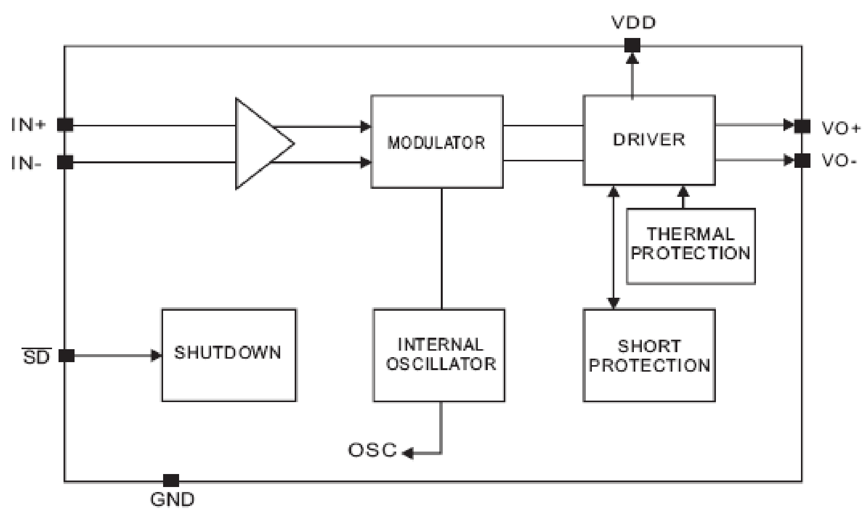
Pin Descriptions

Pin Number	Pin Name	Function
1	$\overline{SD}$	Shutdown Terminal (active low)
2	NC	No Connection
3	IN+	Positive Differential Input
4	IN-	Negative Differential Input
5	VO+	Positive BTL Output
6	VDD	Analog Power Supply
7	GND	Ground
8	VO-	Negative BTL Output

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage at No Input Signal	6.0	V
Input Voltage	-0.3 to V_{DD} +0.3	
Maximum Junction Temperature	150	°C
Storage Temperature	-65 to +150	
Soldering Temperature	300, 5sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Suppy Voltage Range	2.0 to 5.5	V
Operation Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	°C

Thermal Information

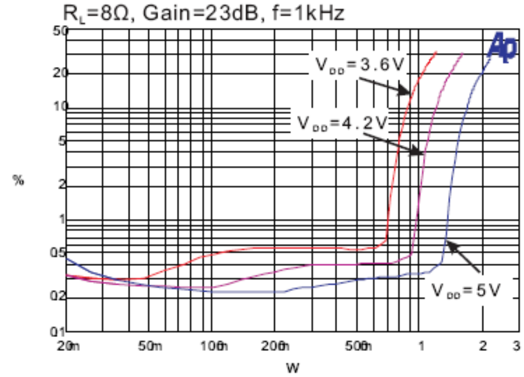
Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Case)	MSOP-8	θ_{JC}	75	°C/W
	DFN3x3-8		20	
Thermal Resistance (Junction to Ambient)	MSOP-8	θ_{JA}	180	°C/W
	DFN3x3-8		50	
Internal Power Dissipation @ T_A = +25°C	MSOP-8	P_D	550	mW
	DFN3x3-8		2000	

Electrical Characteristics (@T_A = +25°C, V_{IN} = 3.6V, V_O = 1.8V, C_{IN} = 10µF, C_{OUT} = 10µF, L = 4.7µH, unless otherwise specified.)

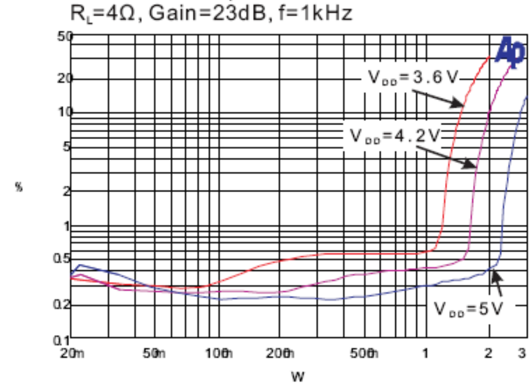
Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Supply Voltage Range	V_{DD}			2.5		5.5	V
Quiescent Current	I_Q	No Load			4	8	mA
Shutdown Current	I_{SHDN}	V_{SHDN} = 0V				1	µA
Output Power	P_O	f = 1kHz, R_L = 4Ω, THD+N = 10%	V_{DD} = 5V	2.25	2.50		W
			V_{DD} = 3.6V	1.10	1.25		
		f = 1kHz, R_L = 4Ω, THD+N = 1%	V_{DD} = 5V	1.80	2.00		
			V_{DD} = 3.6V	0.86	0.95		
		f = 1kHz, R_L = 8Ω, THD+N = 10%	V_{DD} = 5V	1.35	1.50		
			V_{DD} = 3.6V	0.72	0.80		
		f = 1kHz, R_L = 8Ω, THD+N = 1%	V_{DD} = 5V	1.15	1.30		
			V_{DD} = 3.6V	0.6	0.65		
Peak Efficiency	η	f = 1kHz			85	88	%
Total Harmonic Distortion Plus Noise	THD+N	R_L = 8Ω, P_O = 0.1W, f = 1kHz			0.30	0.35	%
		R_L = 8Ω, P_O = 0.5W, f = 1kHz			0.45	0.50	
		R_L = 4Ω, P_O = 0.1W, f = 1kHz			0.35	0.40	
		R_L = 4Ω, P_O = 0.5W, f = 1kHz			0.40	0.45	
Gain	G_V			22.5	24.0	25.5	dB
Power Supply Ripple Rejection	PSRR	No Inputs, f = 1kHz, V_{PP} = 200mV		45	50		dB
Dynamic Range	DYN	f = 20 to 20kHz		85	90		dB
Signal to Noise Ratio	SNR	f = 20 to 20kHz		75	80		dB
Noise	V_N	No A-Weighting			180	300	µV
		A-Weighting			120	200	
Oscillator Frequency	f_{OSC}			200	250	300	kHz
Drain-Source On-State Resistance	$R_{DS(ON)}$	I_{DS} = 100mA	P MOSFET		0.45	0.50	Ω
			N MOSFET		0.20	0.25	
$\overline{SHDN}$ Input High	V_{SH}			1.2			V
$\overline{SHDN}$ Input Low	V_{SL}					0.4	
Over Temperature Protection	OTP	Junction Temperautre		120	135		°C
Over Temperature Hysterisis	OTH				30		°C

Typical Performance Characteristics (@T_A = +25°C, unless otherwise specified.)

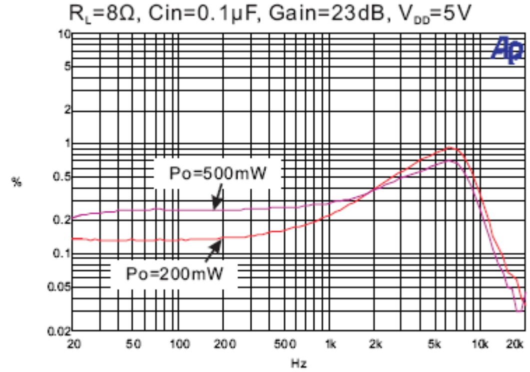
THD+N VS Output Power
R_L=8Ω, Gain=23dB, f=1kHz



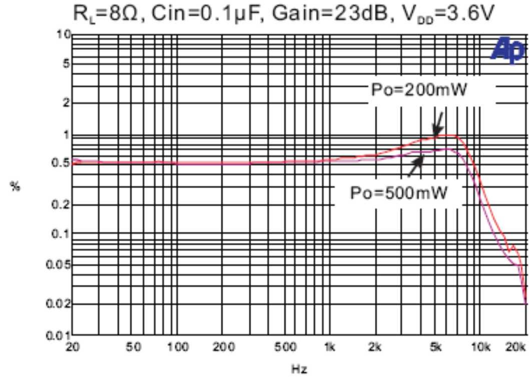
THD+N VS Output Power
R_L=4Ω, Gain=23dB, f=1kHz



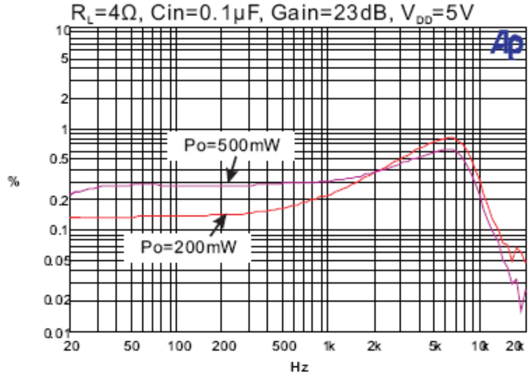
THD+N VS Frequency
R_L=8Ω, Cin=0.1μF, Gain=23dB, V_{DD}=5V



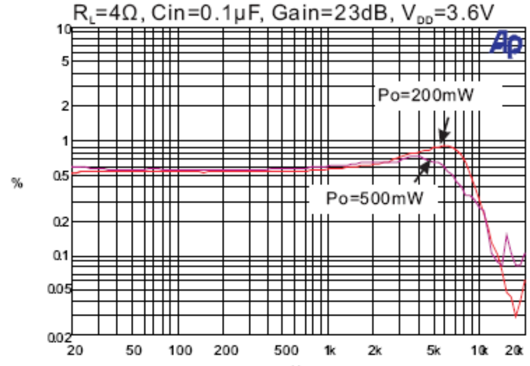
THD+N VS Frequency
R_L=8Ω, Cin=0.1μF, Gain=23dB, V_{DD}=3.6V



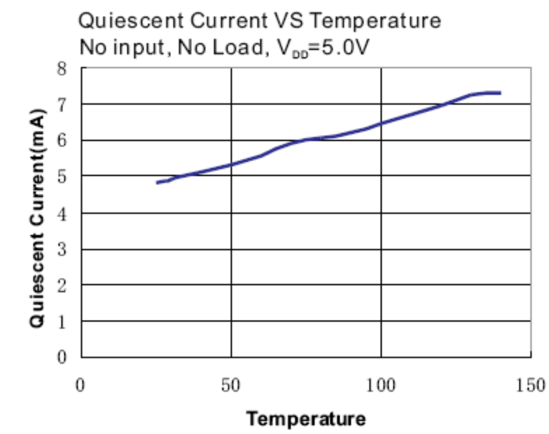
THD+N VS Frequency
R_L=4Ω, Cin=0.1μF, Gain=23dB, V_{DD}=5V

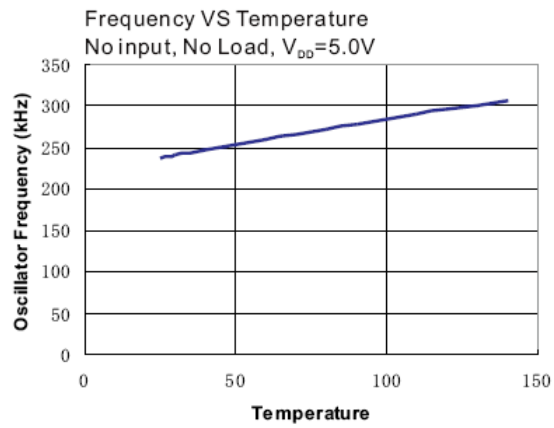


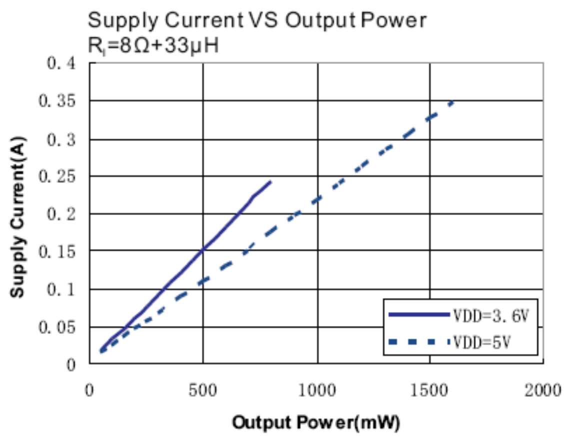
THD+N VS Frequency
R_L=4Ω, Cin=0.1μF, Gain=23dB, V_{DD}=3.6V

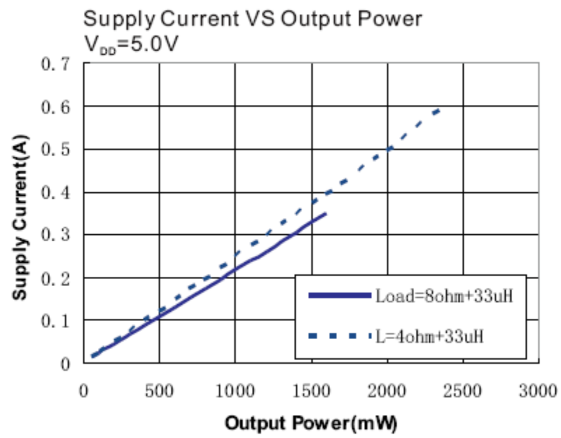


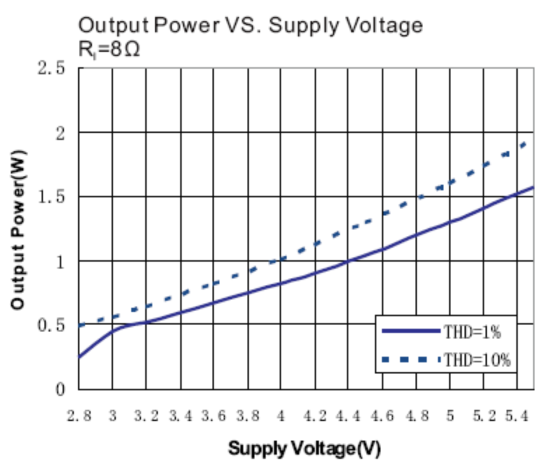
Typical Performance Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)

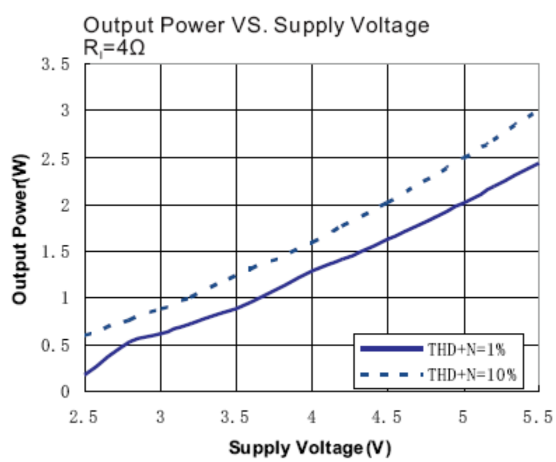




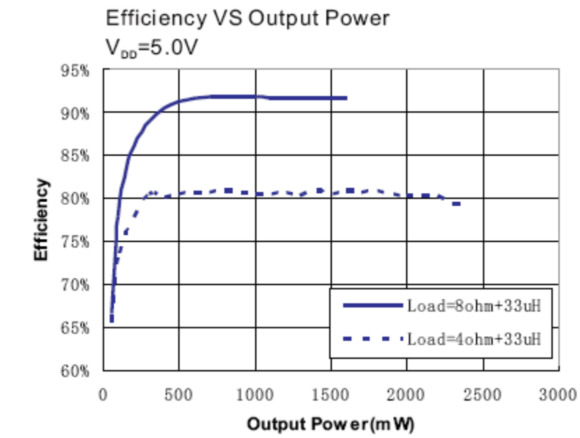


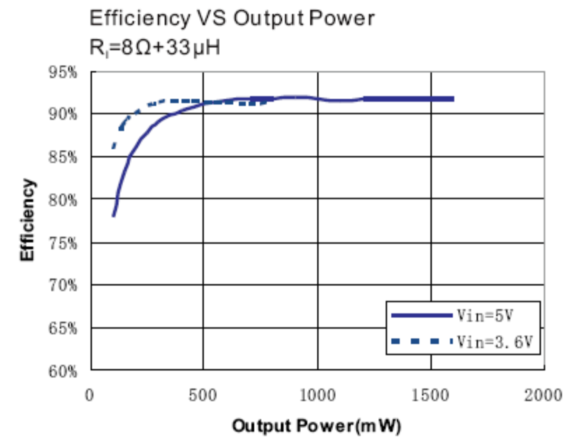


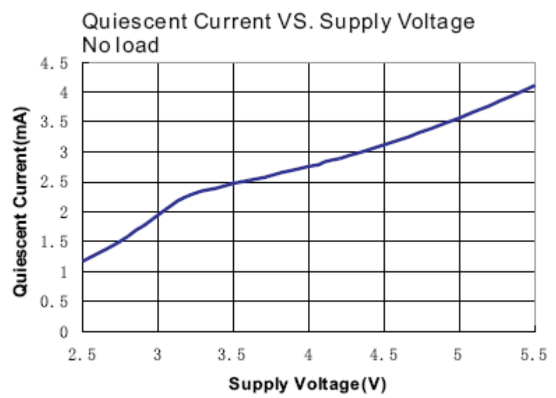


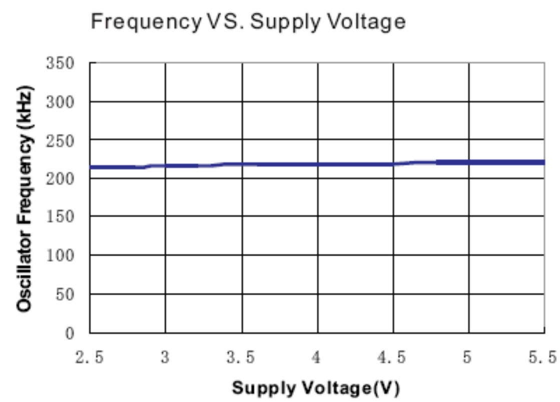


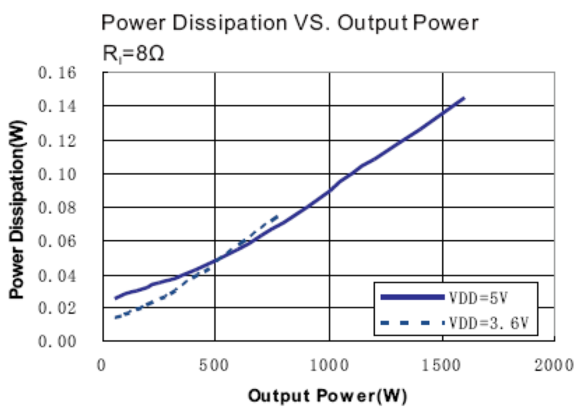
Typical Performance Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)





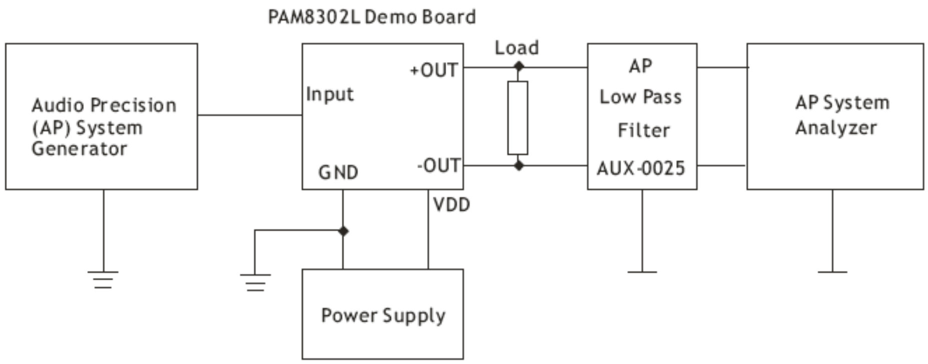






Application Information

Test Setup for Performance Testing



Notes: 1. The Audio Precision (AP) AUX-0025 low pass filter is necessary for every Class-D amplifier measurement with AP analyzer.
2. Two 22µH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Maximum Gain

As shown in block diagram (Page 2), the PAM8302L has two internal amplifier stages. The first stage's gain is externally con figurable, while the second stage's is internally fixed. The closedloop gain of the first stage is set by selecting the ratio of R_F to R_I while the second stage's gain is fixed at 2x.The output of amplifier one serves as the input to amplifier two, thus the two amplifiers produce signals identical in magnitude, but different in phase by 180°. Consequently, the differential gain for the IC is

$$A = 20*\log [2*(R_F/R_I)]$$

The PAM8302L sets maximum R =80kΩ, minimum R_I =10kΩ, so the maximum closed-gain is 24dB.

Input Capacitor (C_I)

Intypical application, an input capacitor, C_I is required to allow the amplifier to bias input signals to a proper DC level for optimum operation. In this case, C_I and the minimum input impedance R_I (10k internal) form a high pass filter with a corner frequeny determind by the following equation:

$$f_C = \frac{1}{2\Pi R_I C_I}$$

It is important to choose the value of C_I as it directly affects low frequency performance of the circuit, for example, when an application requires a flat bass response as loas as 100Hz,. Equation is reconfigured as follows:

$$C_I = \frac{1}{2\Pi R_I f_I}$$

As the input reisitance is varible, for the C_I value of 0.16µF, one should actually choose the C_I within the range of 0.1µF to 0.22µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, R_F, C_I) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain application. For this reason, a low leakage tantalum or ceramic capacitor is the best choice. When a polarized capacitior is used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Application Information (cont.)

Power Supply Decoupling (C_S)

The PAM8302L is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR as low as possible. Power supply decoupling affects low frequency response. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typicall 1.0µF is good, placing it as close as possilbe to the device V_{DD} terminal. For filtering lower frequency noise signals, capacitor of 10µF or larger, closely located to near the audio power amplifier is recommended.

Shutdown Operation

In order to reduce shutdown power consumption, the PAM8302L contains shutdown circuitry for turn to turn off the amplifier. This shutdown feature turns the amplifier off when a logic low is apllied on the $\overline{SD}$ pin. By switching the shutdown pin over to GND, the PAM8302L supply current draw will be minimized inidle mode.

For the best power on/off pop performance, the amplifier should be set in the shutdown mode prior to power on/off operation.

Under Voltage Lock-Out (UVLO)

The PAM8302L incorporates circuitry to detect low on or off voltage. When the supply voltage drops to 2.1V or below, the PAM8302L goes into a state of shutdown, and the device comes out of its shutdown state to normal operation by reset the power supply or SD pin.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000µF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (< 20CM). Most applications require a ferrite bead filter as shown at Figure 1. The ferrite filter depresses EMI of around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies and low impedance at low frequencies.

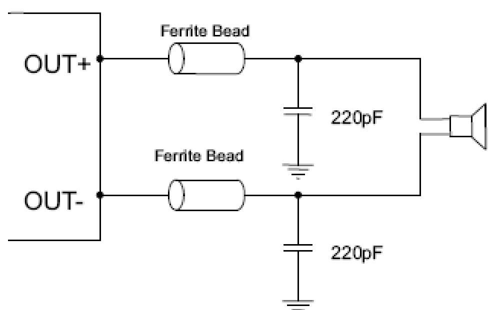


Figure 1. Ferrite Bead Filter to Reduce EMI

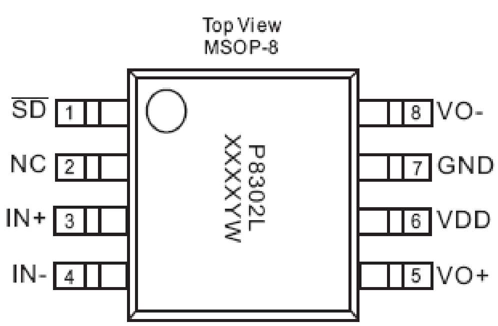
Ordering Information

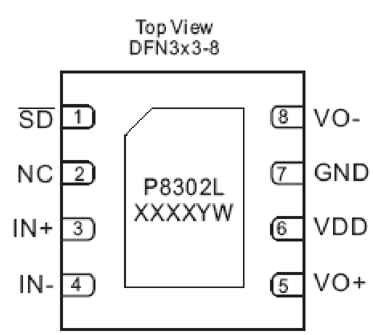
PAM8302L X X X X

Pin Configuration	Package Type	Number of Pins	Shipping Package
A: 1. SD 2. NC 3. IN+ 4. IN- 5. VO+ 6. VDD 7. GND 8. VO-	S: MSOP Y: DFN 3x3	C: 8	R: Tape&Reel

Part Number	Package Type	Standard Package
PAM8302LASCR	MSOP-8	2500 Units/Tape&Reel
PAM8302LAYCR	DFN3x3-8	3000 Units/Tape&Reel

Marking Information

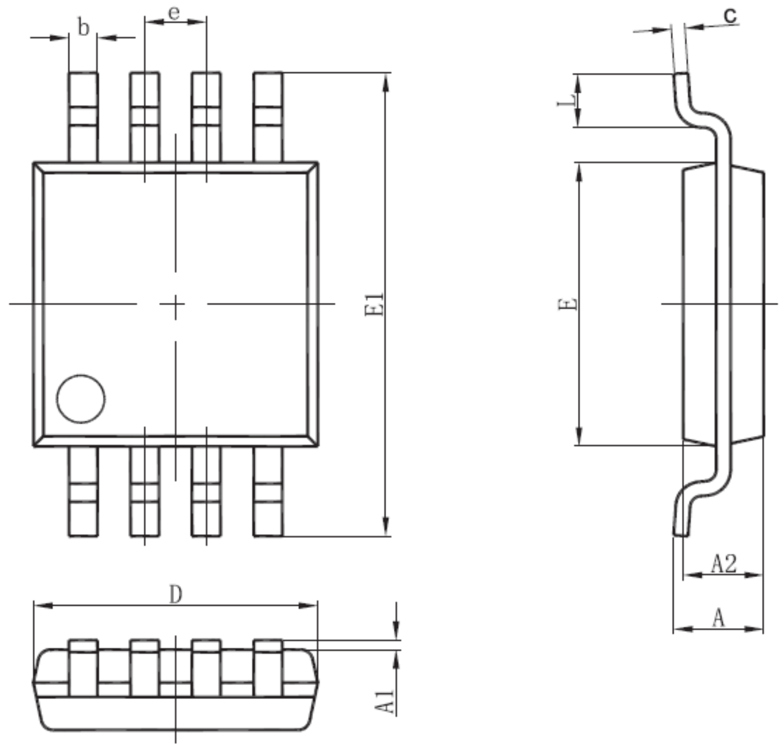




X: Internal Code
Y: Year
W: Week

Package Outline Dimensions (All dimensions in mm.)

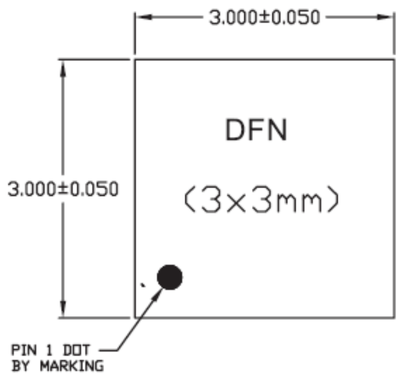
MSOP-8

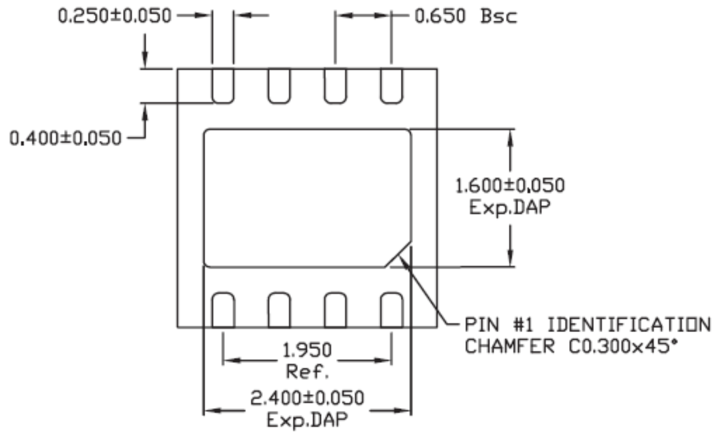


REF	Millimeter	
	Min	Max
A	--	1.10
A1	0.05	0.15
A2	0.78	0.94
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.75	5.05
e	0.65BSC	
L	0.40	0.70

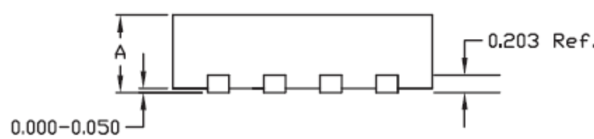
Package Outline Dimensions (cont.) (All dimensions in mm.)

DFN3x3-8





A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700



Note: All dimensions are in Millimeters.

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