DS4-XO Series Crystal Oscillators

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) .....-0.3V, +4V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-55°C to +85°C
Soldering Temperature Profile
(3 passes max of reflow) .....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	(Note 1)	3.135	3.3	3.465	V
Operating Current	I_{CC_D}	LVDS, output loaded or unloaded		52	75	mA
	I_{CC_PU}	LVPECL, output unloaded		49	70	
	I_{CC_PI}	LVPECL, output load 50Ω at V_{CC} - 2.0V		74	100	
Output Frequency	f_{OUT}			f_{NOM}		MHz
Oscillator Startup Time	$t_{STARTUP}$	(Note 2)			50	ms
Frequency Stability	Δf_{TOTAL}	Over temperature range, aging, load, supply, and initial tolerance (Note 3)	-50	f_{NOM}	+50	ppm
Frequency Stability Over Temperature with Initial Tolerance	Δf_{TEMP}	V_{CC} = 3.3V	-35		+35	ppm
Initial Tolerance	$\Delta f_{INITIAL}$	V_{CC} = 3.3V, T_A = +25°C		±20		ppm
Frequency Change Due to ΔV_{CC}	Δf_{VCC}	V_{CC} = 3.3V ±5%	-3		+3	ppm/V
Frequency Change Due to Load Variation	Δf_{LOAD}	±10% variation in termination resistance		±1		ppm
Aging (15 Years)	Δf_{AGING}		-7		+7	ppm
Jitter	J_{RMS}	Integrated phase RMS; 12kHz to 5MHz, V_{CC} = 3.3V, T_A = +25°C		0.7		ps
		Integrated phase RMS; 12kHz to 20MHz, V_{CC} = 3.3V, T_A = +25°C		0.7		
		Integrated phase RMS; 12kHz to 80MHz, V_{CC} = 3.3V, T_A = +25°C		1.0		
Input-Voltage High (OE)	V_{IH}	(Note 1)	0.7 x V_{CC}		V_{CC}	V
Input-Voltage Low (OE)	V_{IL}	(Note 1)	0		0.3 x V_{CC}	V
Input Leakage (OE)	I_{LEAK}	GND ≤ OE ≤ V_{CC}	-50		+5.0	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS						
Output High Voltage	$V_{OHLVDSO}$	100Ω differential load (Note 1)			1.475	V
Output Low Voltage	$V_{OLLVDSO}$	100Ω differential load (Note 1)	0.925			V
Differential Output Voltage	$\|V_{ODLVDSO}\|$	100Ω differential load	250		425	mV
Output Common-Mode Voltage Variation	$V_{LVDSOCOM}$	100Ω differential load			150	mV
Change in Differential Magnitude or Complementary Inputs	$\Delta\|V_{ODLVDSO}\|$	100Ω differential load			25	mV
Offset Output Voltage	$V_{OFFLVDSO}$	100Ω differential load (Note 1)	1.125		1.275	V
Differential Output Impedance	R_{OLVDSO}		80		140	Ω
Output Current	$I_{VSSLVDSO}$	OUTN or OUTP shorted to ground and measure the current in the shorting path			40	mA
	I_{LVDSO}	OUTN or OUTP shorted together		6.5		
Output Rise Time (Differential)	t_{RLVDSO}	20% to 80%		175		ps
Output Fall Time (Differential)	t_{FLVDSO}	80% to 20%		175		ps
Duty Cycle	D_{CYCLE_LVDS}		45		55	%
Propagation Delay from OE Going LOW to Logical 1 at OUTP	t_{PA1}				200	ns
Propagation Delay from OE Going HIGH to Output Active	t_{P1A}				200	ns
LVPECL						
Output High Voltage	V_{OH}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.085		V_{CC} - 0.88	V
Output Low Voltage	V_{OL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.825		V_{CC} - 1.62	V
Differential Voltage	V_{DIFF_PECL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	0.595	0.710		V
Rise Time	$t_{R\text{-}PECL}$			200		ps
Fall Time	$t_{F\text{-}PECL}$			200		ps
Duty Cycle	D_{CYCLE_PECL}		45		55	%
Propagation Delay from OE Going LOW to Output High Impedance	t_{PAZ}				200	ns
Propagation Delay from OE Going HIGH to Output Active	t_{PZA}				200	ns

Note 1: All voltages referenced to ground.
Note 2: AC parameters are guaranteed by design and not production tested.
Note 3: Frequency stability is calculated as: $\Delta f_{TOTAL} = \Delta f_{TEMP} + \Delta f_{VCC} \times (3.3 \times 5\%) + \Delta f_{LOAD} + \Delta f_{AGING}$.

DS4-XO Series Crystal Oscillators

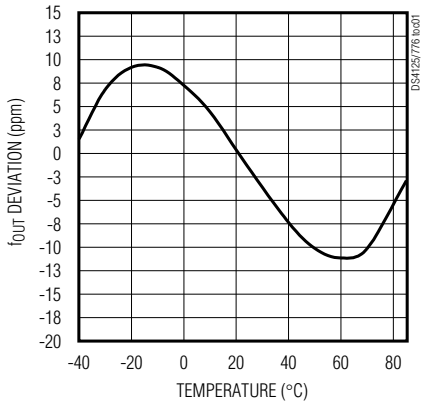
SINGLE-SIDEBAND PHASE NOISE AT $f_O = f_{NOM}$

f_M =	SINGLE-SIDEBAND PHASE NOISE AT $f_O = f_{NOM}$ (dBc/Hz)							
	77.76MHz	125.00MHz	155.52MHz	156.25MHz	160.00MHz	311.04MHz	312.5MHz	622.08MHz
10Hz	-60	-70	-70	-70	-70	-65	-65	-60
100Hz	-95	-100	-100	-100	-100	-95	-95	-90
1kHz	-122	-120	-120	-120	-120	-113	-113	-107
10kHz	-126	-120	-120	-120	-120	-113	-113	-107
100kHz	-131	-125	-125	-125	-125	-118	-118	-113
1MHz	-143	-142	-142	-142	-142	-137	-137	-131
10MHz	-149	-149	-149	-149	-149	-149	-149	-147
20MHz	-153	-153	-153	-153	-153	-153	-153	-150

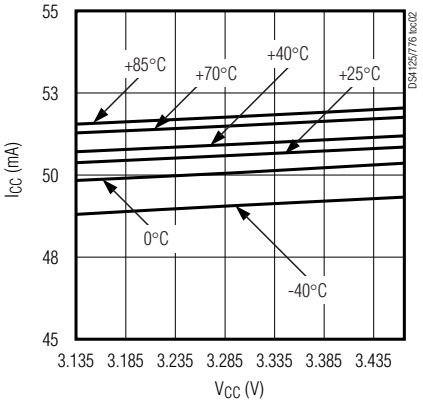
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

FREQUENCY vs. TEMPERATURE



OPERATING CURRENT (DS4155) vs. OPERATING VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	OE	Active-High Output Enable. Has an internal pullup 100kΩ resistor.
2, 7–10	N.C.	No Connection. Must be floated.
3	GND	Ground
4	OUTP	Positive Output for LVPECL or LVDS
5	OUTN	Negative Output for LVPECL or LVDS
6	V_{CC}	Supply Voltage
—	EP	Exposed Paddle. Do not connect this pad or place exposed metal under the pad.

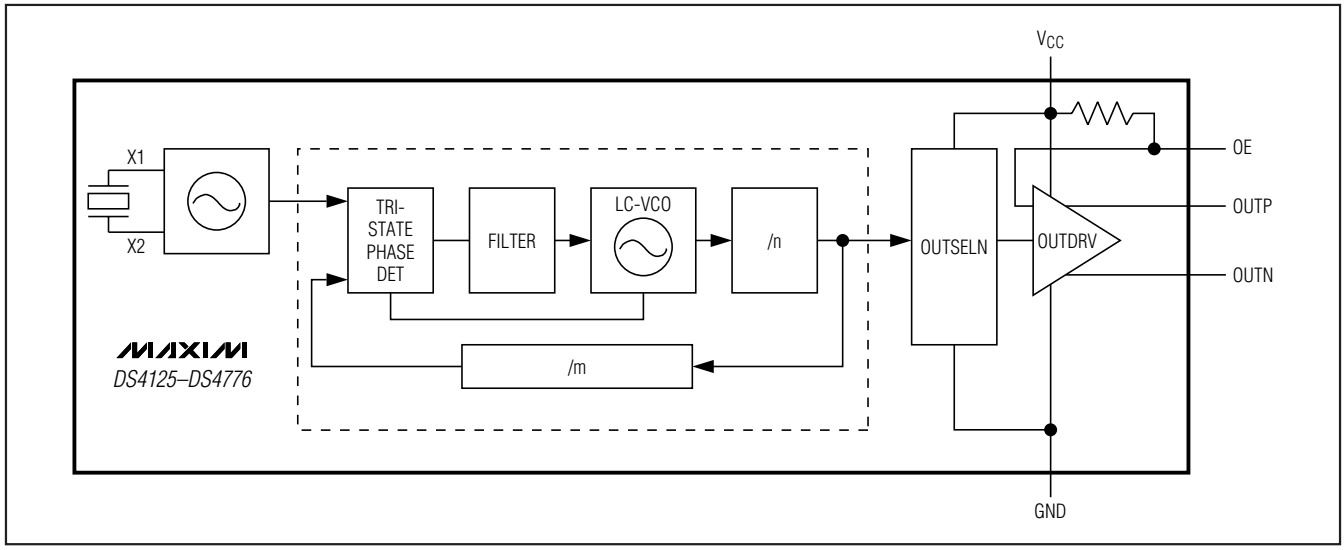


Figure 1. Functional Diagram

Detailed Description

The devices consist of a fundamental-mode, AT-cut crystal and a synthesizer IC that can synthesize any one of these frequencies: 77.76MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 160MHz, 250MHz, 300MHz, 311.04MHz, 312.5MHz, and 622.08MHz.

All devices support two types of differential output drivers: LVDS and LVPECL. When the OE signal is low, LVPECL outputs go to the PECL_BIAS level of V_{CC} - 2.0V, while the LVDS outputs are a logical one. See Figures 2 and 3 for an LVDS and LVPECL output timing diagram.

Additional Information

For more available frequencies, refer to the DS4106 data sheet at **www.maxim-ic.com/DS4106**.

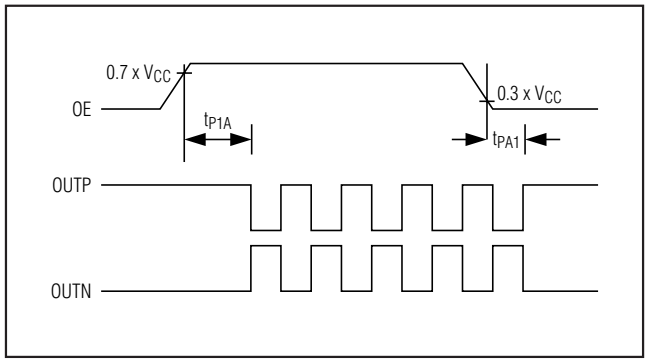


Figure 2. LVDS Output Timing Diagram When OE Is Enabled and Disabled

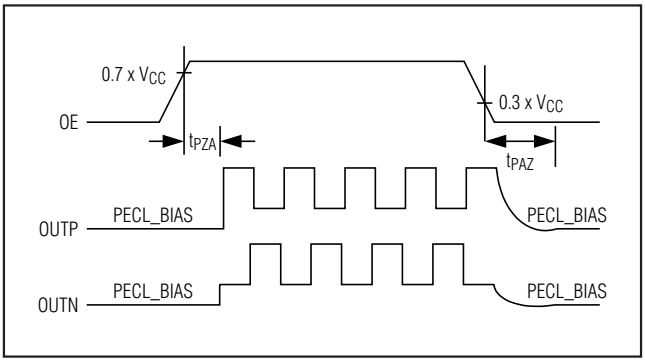


Figure 3. LVPECL Output Timing Diagram When OE Is Enabled and Disabled

DS4-XO Series Crystal Oscillators

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DS4311D+	-40°C to +85°C	10 LCCC
DS4311P+	-40°C to +85°C	10 LCCC
DS4312D+	-40°C to +85°C	10 LCCC
DS4312P+	-40°C to +85°C	10 LCCC
DS4622D+	-40°C to +85°C	10 LCCC
DS4622P+	-40°C to +85°C	10 LCCC
DS4776D+	-40°C to +85°C	10 LCCC
DS4776P+	-40°C to +85°C	10 LCCC

+Denotes a lead(Pb)-free/RoHS-compliant package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: BiPOLAR SiGe

Thermal Information

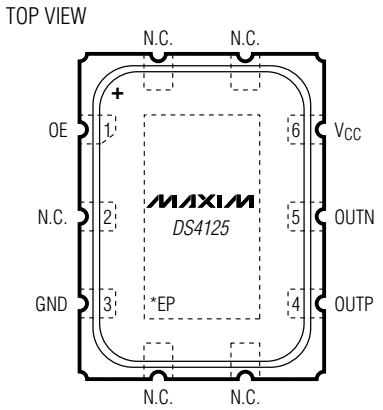
THETA-JA (°C/W)
90

Selector Guide

PART	FREQUENCY (NOM) (MHz)	FREQUENCY STABILITY (ppm)	OUTPUT TYPE	TOP MARK
DS4125D+	125.00	±50	LVDS	25D
DS4125P+	125.00	±50	LVPECL	25P
DS4150D+	150.00	±50	LVDS	50D
DS4150P+	150.00	±50	LVPECL	50P
DS4155D+	155.52	±50	LVDS	55D
DS4155P+	155.52	±50	LVPECL	55P
DS4156D+	156.25	±50	LVDS	56D
DS4156P+	156.25	±50	LVPECL	56P
DS4160D+	160.00	±50	LVDS	60D
DS4160P+	160.00	±50	LVPECL	60P
DS4250D+	250.00	±50	LVDS	T5D
DS4250P+	250.00	±50	LVPECL	T5P
DS4300D+	300.00	±50	LVDS	30D
DS4300P+	300.00	±50	LVPECL	30P
DS4311D+	311.04	±50	LVDS	31D
DS4311P+	311.04	±50	LVPECL	31P
DS4312D+	312.50	±50	LVDS	32D
DS4312P+	312.50	±50	LVPECL	32P
DS4622D+	622.08	±50	LVDS	62D
DS4622P+	622.08	±50	LVPECL	62P
DS4776D+	77.76	±50	LVDS	76D
DS4776P+	77.76	±50	LVPECL	76P

+Denotes a lead(Pb)-free/RoHS-compliant package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Pin Configuration



LCCC
(5.00mm × 3.20mm × 1.49mm)

*EXPOSED PAD

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 LCCC	L1053+H2	**21-0389**

DS4-XO Series Crystal Oscillators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release.	—
1	3/08	Added DS4150, DS4250, DS4300.	All
		Removed $\Delta f_{INITIAL}$ from the frequency stability calculation in Note 3.	3
		In the *Pin Description*, changed the EP description to indicate that it should not be connected and to avoid placing exposed metal under the pad location.	4
2	6/08	Removed future status from the DS4150, DS4250, and DS4300.	1, 6

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

DS4125P+ DS4312D+ DS4125D+ DS4150D+ DS4150P+ DS4155D+ DS4155P+ DS4156D+ DS4160D+ DS4160P+ DS4250D+ DS4250P+ DS4300D+ DS4300P+ DS4311D+ DS4311P+ DS4622D+ DS4622P+ DS4776D+ DS4776P+ DS4156P+