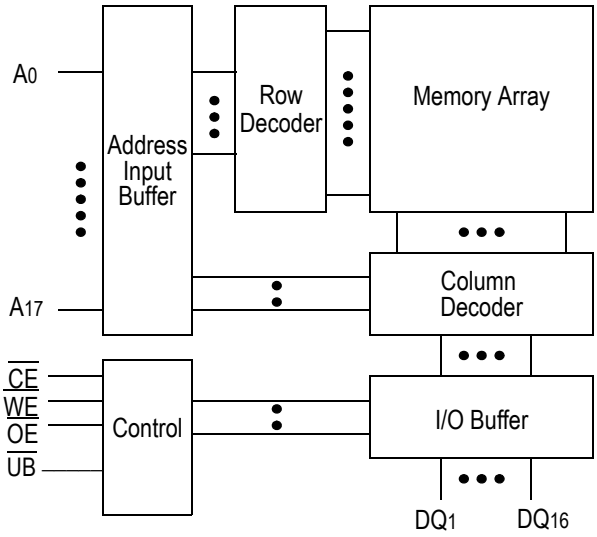
Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ1 to DQ8	DQ9 to DQ16	VDD Current
H	X	X	X	X	Not Selected	Not Selected	ISB1, ISB2
L	L	H	L	L	Read	Read	IDD
			L	H	Read	High Z	
			H	L	High Z	Read	
L	X	L	L	L	Write	Write	
			L	H	Write	Not Write, High Z	
			H	L	Not Write, High Z	Write	
L	H	H	X	X	High Z	High Z	
L	X	X	H	H	High Z	High Z	

X: “H” or “L”

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/-10/-12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{AI}	–40	—	85	°C

Notes:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	– 1 uA	1 uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—
Output Low Voltage	V_{OL}	I_{LO} = +4 mA	—	0.4 V

Power Supply Currents

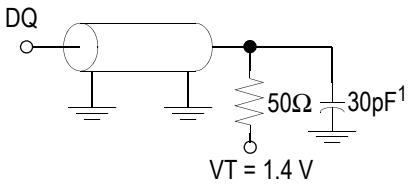
Parameter	Symbol	Test Conditions	0 to 70°C			–40 to 85°C			Unit
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns	
Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	130	105	90	140	115	100	mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	30	25	22	40	35	32	mA
Standby Current	I_{SB2}	$\overline{CE} \ge V_{DD}$ – 0.2 V All other inputs $\ge V_{DD}$ – 0.2 V or $\le$ 0.2 V	10			20			mA

AC Test Conditions

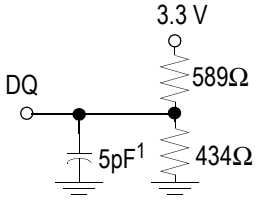
Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}

Output Load 1



Output Load 2



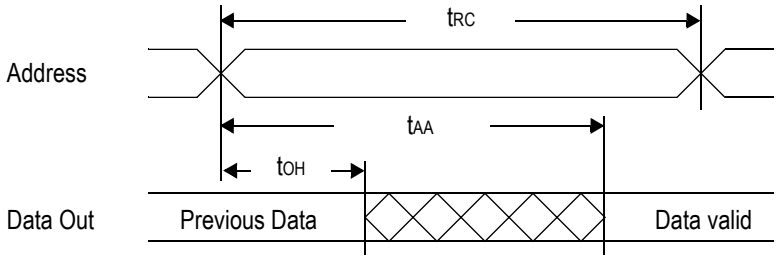
AC Characteristics

Read Cycle

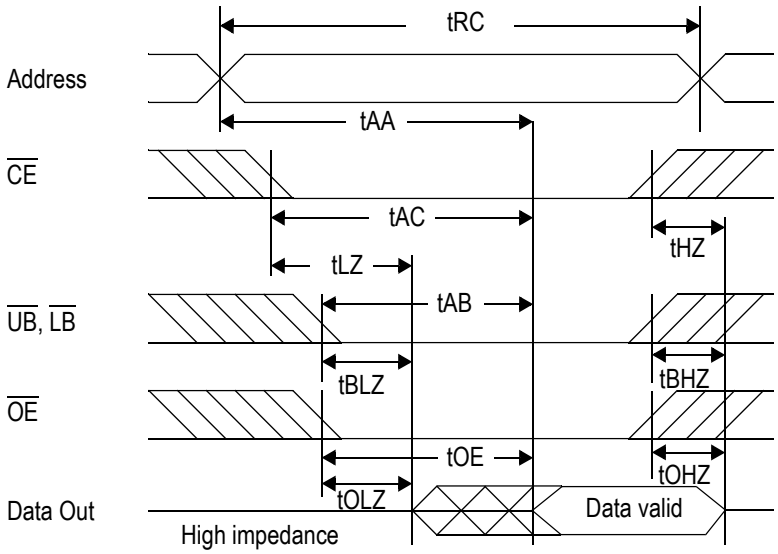
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	8	—	10	—	12	ns
Byte enable access time ($\overline{UB}$, $\overline{LB}$)	t_{AB}	—	3.5	—	4	—	5	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Byte enable to output in low Z ($\overline{UB}$, $\overline{LB}$)	t_{BLZ}*	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3.5	—	4	—	5	ns
Byte disable to output in High Z ($\overline{UB}$, $\overline{LB}$)	t_{BHZ}*	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{UB}$ and, or $\overline{LB}$ = V_{IL}



Read Cycle 2: $\overline{WE}$ = V_{IH}

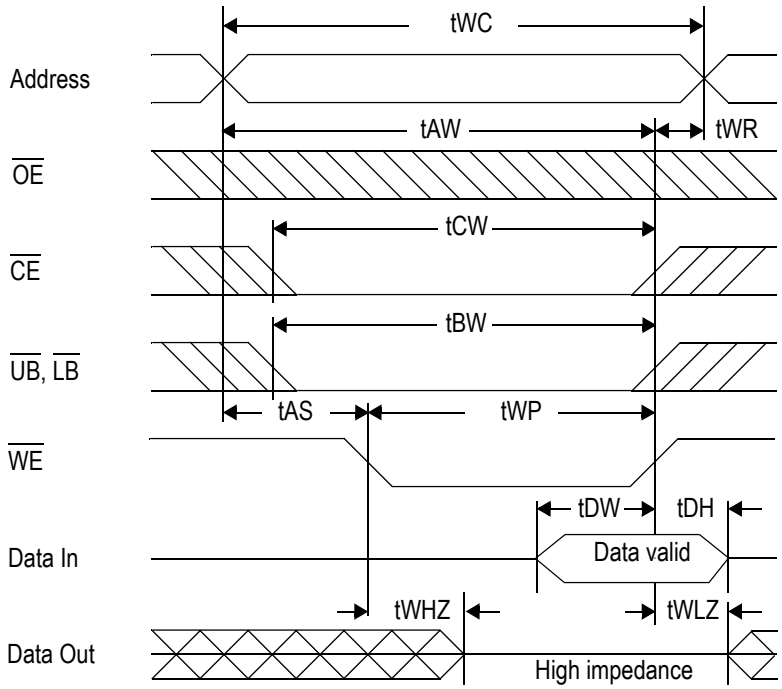


Write Cycle

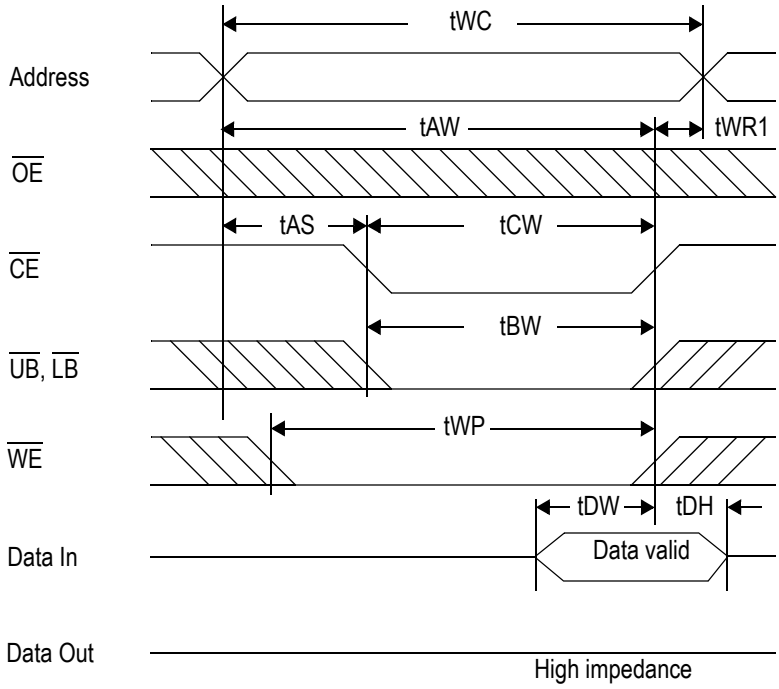
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5.5	—	7	—	8	—	ns
Byte enable to end of write	tBW	5.5	—	7	—	8	—	ns
Data set up time	tDW	4	—	4.5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	ns
Write pulse width	tWP	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

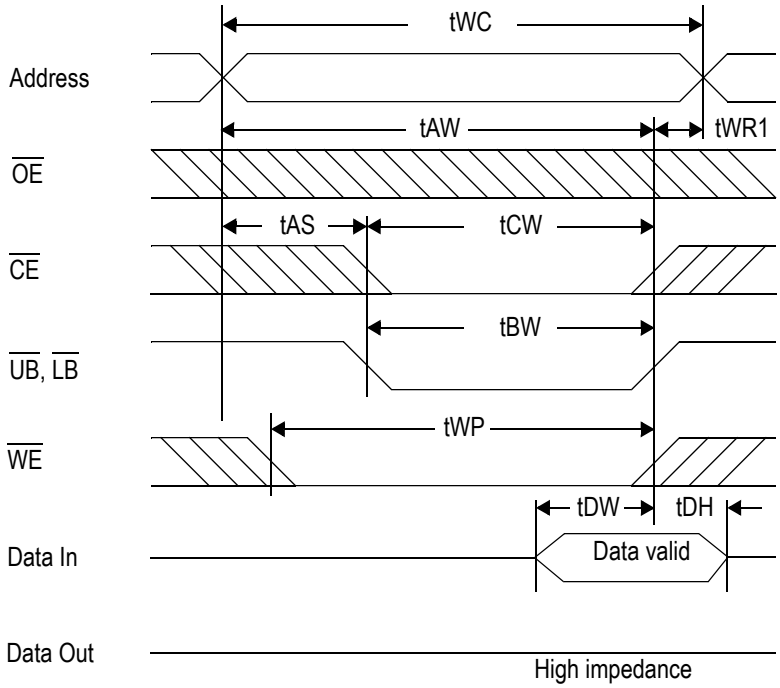
Write Cycle 1: $\overline{WE}$ control



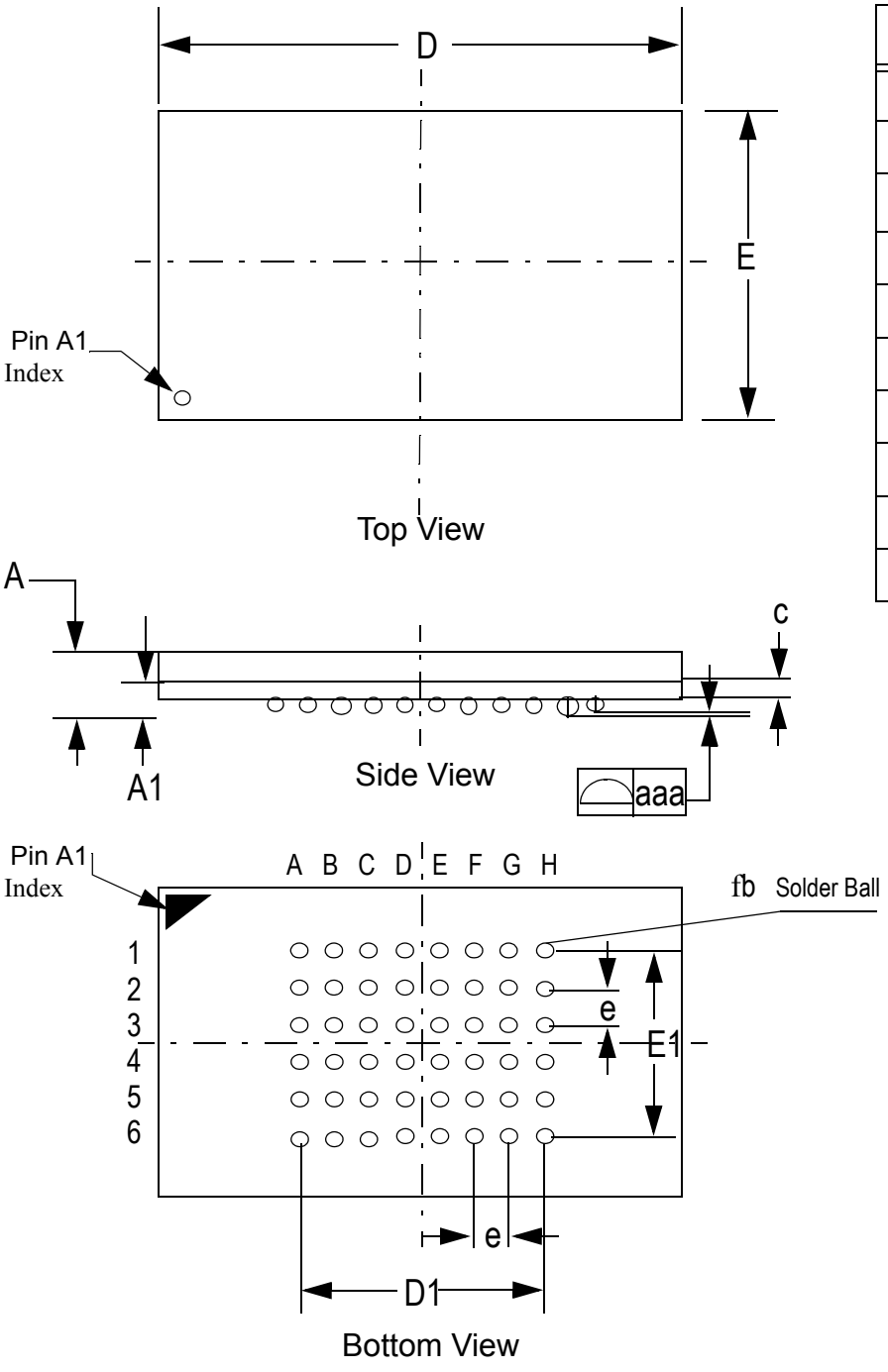
Write Cycle 2: $\overline{CE}$ control



Write Cycle 3: $\overline{UB}$, $\overline{LB}$ control



Package X—6 mm x 10 mm FP-BGA



Symbol	Unit: mm
A	1.10±0.10
A1	0.20~0.30
fb	f0.30~0.40
c	0.36(TYP)
D	10.0±0.05
D1	5.25
E	6.0±0.05
E1	3.75
e	0.75(TYP)
aaa	0.10

Ordering Information

Part Number*	Package	Access Time	Temp. Range
GS74117AX-8	6 mm x 10 mm BGA	8 ns	Commercial
GS74117AX-10	6 mm x 10 mm BGA	10 ns	Commercial
GS74117AX-12	6 mm x 10 mm BGA	12 ns	Commercial
GS74117AX-8I	6 mm x 10 mm BGA	8 ns	Industrial
GS74117AX-10I	6 mm x 10 mm BGA	10 ns	Industrial
GS74117AX-12I	6 mm x 10 mm BGA	12 ns	Industrial
GS74117AGX-8	Pb-free 6 mm x 10 mm BGA	8 ns	Commercial
GS74117AGX-10	Pb-free 6 mm x 10 mm BGA	10 ns	Commercial
GS74117AGX-12	Pb-free 6 mm x 10 mm BGA	12 ns	Commercial
GS74117AGX-8I	Pb-free 6 mm x 10 mm BGA	8 ns	Industrial
GS74117AGX-10I	Pb-free 6 mm x 10 mm BGA	10 ns	Industrial
GS74117AGX-12I	Pb-free 6 mm x 10 mm BGA	12 ns	Industrial

* Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS74117AX-8T

4Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
74117A_r1	Format/Content	• Creation of new datasheet
74117A_r1; 74117A_r1_01	Content	• Updated Recommended Operating Conditions table on page 3 • Updated Read Cycle and Write Cycle AC Characteristics tables
74117A_r1_01; 74117A_r1_02	Content	• Removed 6 ns speed bin from entire document
74117A_r1_02; 74117A_r1_03	Content	• Removed 7 ns speed bin from entire document
74117A_r1_03; 74117A_r1_04	Format	• Updated format
74117A_r1_04; 74117A_r1_05	Content	• Added Pb-free information for FP-BGA package • (Rev1.05a: Removed empty status column on ordering information table) • (Rev1.05b: Changed 6 x 10 mm Ball Pitch reference on page 1 to 6 x 10 mm Substrate)

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GSI Technology:

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