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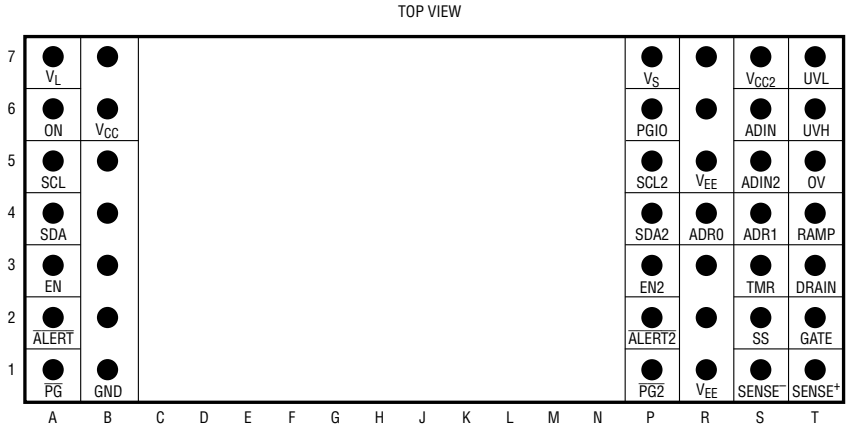
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{CC} to GND ..... –0.3V to 6V
V_L to GND ..... –0.3V to 6V
V_{CC2} to V_{EE} ..... –0.3V to 5.5V
V_S to V_{EE} (Note 3) ..... –0.3V to 10.65V
DRAIN to V_{EE} (Note 4) ..... –0.3V to 3.5V
$\overline{PG}$, $\overline{ALERT}$, EN, SDA, SCL,
ON to GND ..... –0.3V to (V_L + 0.3V)
SCL2, SDA2, ADR0, ADR1, $\overline{ALERT2}$, $\overline{PG2}$, ADIN, ADIN2,
RAMP, OV, SS, EN2,
TMR to V_{EE} ..... –0.3V to (V_{CC2} + 0.3V)
GATE to V_{EE} ..... –0.3V to (V_S + 0.3V)
UVL, UVH to V_{EE} ..... –0.3V to 10V
PGIO to V_{EE} ..... –0.3V to 80V
$SENSE^+$ to $SENSE^-$ ..... –0.3V to 0.3V
$SENSE^-$ to V_{EE} ..... –0.3V to 0.3V
Ambient Operating Temperature Range (Note 5)
LTM9100C ..... 0°C to 70°C
LTM9100I ..... –40°C to 85°C
LTM9100H ..... –40°C to 105°C
Maximum Internal Operating Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Body Reflow Temperature ..... 245°C

PIN CONFIGURATION



BGA PACKAGE
42-LEAD (22mm × 9mm × 5.16mm)

T_{JMAX} = 125°C, PCB = JESD51-9 2s2p: θ_{JA} = 25.6°C/W, θ_{JCtop} = 24.8°C/W, $\theta_{JCbottom}$ = 11.7°C/W, θ_{JB} = 12.1°C/W
HEAT FLOW: θ_{JA} = NORMAL, θ_{JCtop} = 100%, $\theta_{JCbottom}$ = 100%, θ_{JB} = 100% WEIGHT = 2g

ORDER INFORMATION

http://www.linear.com/product/LTM9100#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTM9100CY#PBF	SAC305 (RoHS)	LTM9100Y	e1	BGA	3	0°C to 70°C
LTM9100IY#PBF						–40°C to 85°C
LTM9100HY#PBF						–40°C to 105°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to www.linear.com/BGA-assy
- Recommended BGA PCB Assembly and Manufacturing Procedures: www.linear.com/BGA-assy
- BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/BGA-assy

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Input Supply Range		●	4.5		5.5	V
I_{CC}	Input Supply Current	ON = 0V ON = V_L, No Load	● ●		0 50	10 70	µA mA
V_L	Logic Input Supply Range		●	3		5.5	V
	Logic Input Supply Current	ON = 0V ON = V_L	● ●		0 3.2	10 4.5	µA mA
	V_L Undervoltage Lockout Threshold	V_L Rising	●	2.3		2.7	V
	V_L Undervoltage Lockout Hysteresis				100		mV
V_S	Regulated Output Voltage	I_{LOAD} = 0mA to 35mA	●	9.65	10.4	11.15	V
V_Z	Shunt Regulator Voltage at V_S	I_S = 10mA, V_{CC} = 0V	●	10.4	11.2	12	V
	Shunt Regulator Load Regulation	I_S = 10mA to 25mA, V_{CC} = 0V	●		370	600	mV
I_S	V_S Supply Current	V_S = 10.4V, V_{CC} = 0V	●		7	12	mA
	V_S Undervoltage Lockout Threshold	V_S Rising, V_{CC} = 0V	●	8.5	9	9.5	V
	V_S Undervoltage Lockout Hysteresis	V_{CC} = 0V	●	0.3	0.7	1.1	V
V_{CC2}	Regulated Output Voltage	I_{LOAD} = 0mA to 15mA	●	4.75	5	5.25	V
Gate Drive (EN = V_L, UVL = UVH = V_{CC2}, OV = 0V, unless otherwise noted)							
V_{GATEH}	GATE Pin Output High Voltage	V_S = 10.4V, V_{CC} = 0V	●	9.75	10	10.25	V
$I_{GATE(UP)}$	GATE Pin Pull-Up Current	V_{GATE} = 4V	●	–7.5	–11.5	–15.5	µA
$I_{GATE(OFF)}$	GATE Turn-Off Current	V_{SENSE} = 400mV, V_{GATE} = 4V EN = 0V, V_{GATE} = 4V	● ●	45 120	100 175	150 250	mA mA
$t_{PHL(SENSE)}$	SENSE High to Current Limit Propagation Delay	V_{SENSE} = 100mV to GATE Low V_{SENSE} = 300mV to GATE Low	● ●		0.5 0.2	1.5 0.5	µs µs
	GATE Off Propagation Delay	EN↓ to GATE Low OV↑, UVL↓ to GATE Low	● ●		0.2 1.4	0.5 2	µs µs
	Circuit Breaker Gate Off Delay	V_{SENSE} = 300mV to $\overline{PG2}$↑	●	440	530	620	µs
I_{RAMP}	RAMP Pin Current	V_{SS} = 2.56V	●	–18	–20	–22	µA
V_{SS}	SS Pin Clamp Voltage		●	2.43	2.56	2.69	V
	SS Pin Pull-Up Current	V_{SS} = 0V	●	–7	–10	–13	µA
	SS Pin Pull-Down Current	EN = 0V, V_{SS} = 2.56V	●	6	12	20	mA
Input Pins							
	EN, ON Input Threshold Voltage		●	0.33 • V_L		0.67 • V_L	V
	EN, ON Input Hysteresis	(Note 6)			150		mV
$V_{UVH(TH)}$	UVH Threshold Voltage	V_{UVH} Rising	●	2.518	2.56	2.598	V
$V_{UVL(TH)}$	UVL Threshold Voltage	V_{UVL} Falling	●	2.248	2.291	2.328	V
$\Delta V_{UV(HYST)}$	UV Hysteresis	UVH and UVL Tied Together	●	236	269	304	mV
δV_{UV}	UVH, UVL Hysteresis				15		mV
	UVL Reset Threshold Voltage	V_{UVL} Falling	●	1.12	1.21	1.30	V
	UVL Reset Hysteresis				60		mV
$V_{OV(TH)}$	OV Pin Threshold Voltage	V_{OV} Rising	●	1.735	1.770	1.805	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	OV Pin Hysteresis		●	18	37.5	62	mV
	Current Limit Sense Voltage Threshold	$SENSE^+ – SENSE^–$	●	45	50	55	mV
	PGIO Pin Input Threshold Voltage	V_{PGIO} Rising	●	1.10	1.25	1.40	V
	PGIO Pin Input Hysteresis				100		mV
	Input Current	ON, EN, UVH, UVL, OV, $SENSE^+$ $SENSE^–$	● ●		0 –10	±2 –20	µA µA
Timer							
	TMR Pin High Threshold	V_{TMR} Rising	●	2.43	2.56	2.69	V
	TMR Pin Low Threshold	V_{TMR} Falling	●	40	75	110	mV
	TMR Pin Pull-Up Current	Turn-On and Auto-Retry (Except OC) Delays, V_{TMR} = 0.2V	●	–7	–10	–13	µA
		Power Good and OC Auto-Retry Delays, V_{TMR} = 0.2V	●	–3.5	–5	–7	µA
	TMR Pin Pull-Down Current	Delays Except OC Auto-Retry, V_{TMR} = 2.56V	●	6	12	20	mA
		OC Auto-Retry Delays, V_{TMR} = 2.56V	●	3	5	7	µA
Output Pins							
V_{OH}	Output High Voltage	$\overline{ALERT}$, I_{LOAD} = –4mA, $\overline{PG}$, I_{LOAD} = –2mA	●	V_L – 0.4			V
V_{OL}	Output Low Voltage	$\overline{ALERT}$, I_{LOAD} = 4mA, $\overline{PG}$, I_{LOAD} = 2mA PGIO, I_{LOAD} = 3mA $\overline{ALERT2}$, $\overline{PG2}$, PGIO, I_{LOAD} = 500µA	● ● ●		 0.8 0.15	0.4 1.6 0.4	V V V
	Input Current	PGIO = 80V	●		0	10	µA
	Short-Circuit Current	$0V \le \overline{ALERT} \le V_L$ $0V \le \overline{PG} \le V_L$ $0V \le \overline{ALERT2}, \overline{PG2} \le V_{CC2}$ $0V \le EN2 \le V_{CC2}$	● ●		 ±30 ±30 	±85 ±2	mA mA mA mA
ADC							
	Resolution (No Missing Codes)	(Note 6)	●	10			Bits
INL	Integral Nonlinearity	SENSE ADIN, ADIN2	● ●		±0.5 ±0.25	±2.5 ±1.25	LSB LSB
	Offset Error	SENSE ADIN, ADIN2	● ●			±2.25 ±1.25	LSB LSB
	Full-Scale Voltage	SENSE ADIN, ADIN2	● ●	62.8 2.514	64 2.560	65.2 2.606	mV V
	Total Unadjusted Error	SENSE ADIN, ADIN2	● ●			±1.8 ±1.6	% %
	Conversion Rate		●	5.5	7.3	9	Hz
	ADIN, ADIN2 Pin Input Resistance	ADIN, ADIN2 = 1.28V	●	2	10		MΩ
	ADIN, ADIN2 Pin Input Current	ADIN, ADIN2 = 2.56V	●		0	±2	µA
I^2C Interface							
	ADR0, ADR1 Input High Threshold		●	V_{CC2} – 0.8	V_{CC2} – 0.5	V_{CC2} – 0.3	V
	ADR0, ADR1 Input Low Threshold		●	0.3	0.5	0.8	V
	ADR0, ADR1 Input Current	ADR0, ADR1 = 0V, V_{CC2} ADR0, ADR1 = 0.8V, (V_{CC2} – 0.8V)	● ●	 ±10		±80 	µA µA
	Input Threshold Voltage	SCL, SDA SDA2	● ●	0.3 • V_L 0.3 • V_{CC2}		0.7 • V_L 0.7 • V_{CC2}	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Current	SCL, SDA = V_L or 0V	●			±2	µA
	Input Hysteresis	SCL, SDA SDA2			0.05 • V_L 0.05 • V_{CC2}		mV mV
V_{OH}	Output High Voltage	SCL2, I_{LOAD} = –2mA	●	V_{CC2} – 0.4			V
V_{OL}	Output Low Voltage	SDA, I_{LOAD} = 3mA, SCL2, I_{LOAD} = 2mA SDA2, No Load, SDA = 0V	● ●			0.4 0.45	V V
	Input Pin Capacitance	SCL, SDA, SDA2 (Note 6)	●			10	pF
	Bus Capacitive Load	SCL2, Standard Speed (Note 6) SCL2, Fast Speed SDA, SDA2, SR ≥ 1V/µs, Standard Speed (Note 6) SDA, SDA2, SR ≥ 1V/µs, Fast Speed	● ● ● ●			400 200 400 200	pF pF pF pF
	Minimum Bus Slew Rate	SDA, SDA2		1			V/µs
	Short-Circuit Current	SDA2 = 0, SDA = V_L 0V ≤ SCL2 ≤ V_{CC2} SDA = 0, SDA2 = V_{CC2} SDA = V_L, SDA2 = 0	●		 ±30 6 –1.8	100	mA mA mA mA
ESD (HBM) (Note 6)							
	Isolation Boundary	(V_{CC2}, V_S, V_{EE}) to (V_{CC}, V_L, GND) in Any Combination			±20		kV
	Isolated Side Interface Pins	GATE to (V_S, V_{EE}) in Any Combination (RAMP, DRAIN, SENSE$^+$, SENSE$^-$) to (V_{CC2}, V_{EE}) in Any Combination			±8		kV
	All Other Pins				±3.5		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Timing							
t_{PHL}, t_{PLH}	Propagation Delay	($\overline{PG2}$, $\overline{ALERT2}$) to ($\overline{PG}$, $\overline{ALERT}$), C_L = 15pF (Figure 1) EN to EN2 (0.5 • V_L to 0.1 • V_{CC2}), C_L = 15pF (Figure 1)	●	35	60	150	ns
t_R, t_F	Rise and Fall Time	$\overline{ALERT}$, C_L = 15pF (Figure 1) $\overline{PG}$, C_L = 15pF (Figure 1)	● ●		7 30	30 50	ns ns
t_{PZH}, t_{PZL}	ON Enable Time	ON↑ to ($\overline{PG}$, $\overline{ALERT}$), R_L = 1kΩ, C_L = 15pF (Figure 2)	●			320	µs
t_{PHZ}, t_{PLZ}	ON Disable Time	ON↓ to ($\overline{PG}$, $\overline{ALERT}$), R_L = 1kΩ, C_L = 15pF (Figure 2)	●			70	ns
I^{2}C Interface Timing							
	Maximum Data Rate	(Note 7)	●	400			kHz
t_{PHL}, t_{PLH}	Propagation Delay	SCL to SCL2, C_L = 15pF (Figure 1) SDA to SDA2, R_L = Open, C_L = 15pF (Figure 3) SDA2 to SDA, R_L = 1.1kΩ, C_L = 15pF (Figure 3)	● ● ●		150 150 300	225 250 500	ns ns ns
	Low Period of SCL Clock	(Note 6)		1.3			µs

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	High Period of SCL Clock	(Note 6)		600			ns
	Hold Time (Repeated) Start	(Note 6)		600			ns
	Set-Up Time Repeated Start	(Note 6)		600			ns
$t_{HD(DAT)}$	Data Hold Time	(Note 6)			600		ns
$t_{SU(DAT)}$	Data Set-Up Time	(Note 6)		100			ns
	Set-Up Time for Stop	(Note 6)		600			ns
	Stop to Start Bus Free Time	(Note 6)		1.3			µs
t_R	Rise Time	SDA2, C_L = 200pF (Figure 3) SDA, R_L = 1.1kΩ, C_L = 200pF (Figure 3) SCL2, C_L = 200pF (Figure 1)	● ● ●	40 40		350 250 250	ns ns ns
t_F	Fall Time	SDA2, C_L = 200pF (Figure 3) SDA, R_L = 1.1kΩ, C_L = 200pF (Figure 3) SCL2, C_L = 200pF (Figure 1)	● ● ●	40 40		250 250 250	ns ns ns
t_{PZL}	ON Enable Time	ON↑ to SDA, R_L = 1kΩ, C_L = 15pF (Figure 2)	●			320	µs
t_{PLZ}	ON Disable Time	ON↓ to SDA, R_L = 1kΩ, C_L = 15pF (Figure 2)	●			70	ns
	Pulse Width of Spikes Suppressed by Input Filter	SDA, SDA2, SCL	●	0		50	ns
Power Supply							
	Power-Up Time	ON↑ to V_S (Min) ON↑ to V_{CC2} (Min)	● ●		0.2 0.2	1.5 2	ms ms

ISOLATION CHARACTERISTICS

Specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test 1 Second (Notes 8, 9)	5 6			kV_{RMS} kV_{RMS}
	Common Mode Transient Immunity	V_{CC} = V_L = ON = 5V, ΔV_{CM} = 1kV, Δt = 33ns (Note 6)	30	50		kV/µs
V_{IORM}	Maximum Continuous Working Voltage	(Notes 6,10)	1000 690			V_{PEAK} V_{RMS}
	Partial Discharge	V_{PD} = 1840V_{PEAK} (Note 8)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 6)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 6)		0.017		mm
DTI	Distance Through Insulation	(Note 6)		0.2		mm
	Input to Output Resistance	(Notes 6, 8)	1	5		TΩ
	Input to Output Capacitance	(Notes 6, 8)		5		pF
	Creepage Distance	(Note 6)		14.6		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to 0V unless otherwise noted.

Note 3: An internal shunt regulator limits the V_S pin to a minimum of 10.65V. Driving this pin to voltages beyond 10.65V may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current to less than 50mA.

Note 4: An internal clamp limits the DRAIN pin to a minimum of 3.5V. Driving this pin to voltages beyond the clamp may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current to less than 2mA.

Note 5: This µModule includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure. Thermal shutdown will result in the loss of the internally generated supply voltages (V_S and V_{CC2}) and subsequent shutdown of the GATE pin. Thermal shutdown is not internally latched, the part will automatically restart once the junction temperature decreases and start-up conditions are met. Note that any I^2C data configuration is lost on power failure.

Note 6: Guaranteed by design and not subject to production test.

Note 7: Maximum data rate is guaranteed by other measured parameters and is not tested directly.

Note 8: Device is considered a 2-terminal device. Pin group A1 through B7 shorted together and pin group P1 through T7 shorted together.

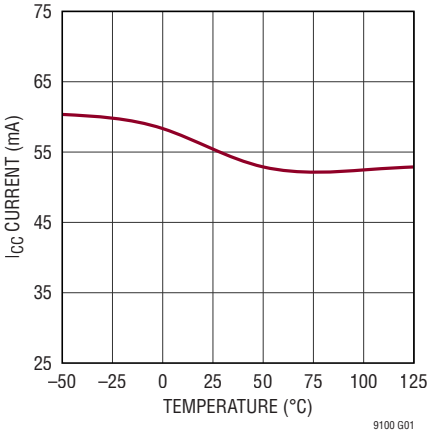
Note 9: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 10: The DC continuous working voltage is equivalent to the peak value.

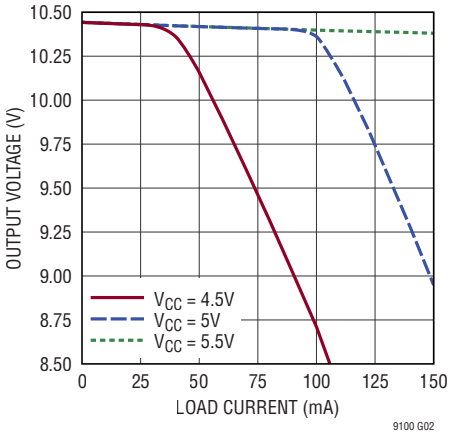
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

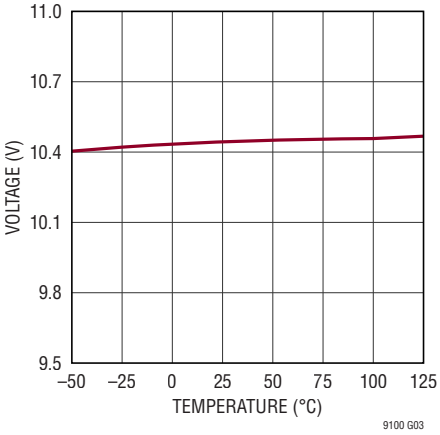
V_{CC} Supply Current vs Temperature



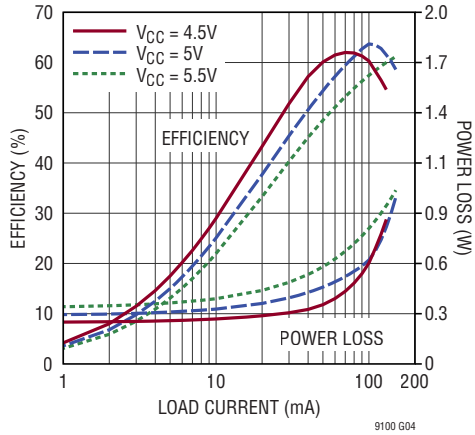
V_S Output Voltage vs Load Current



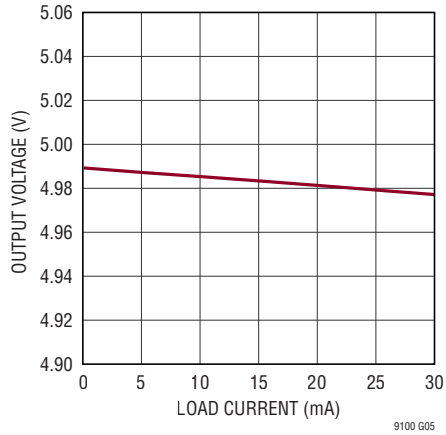
V_S Output Voltage vs Temperature



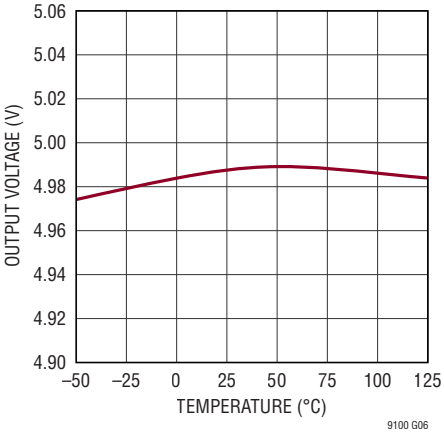
V_S Efficiency and Power Loss vs Load Current



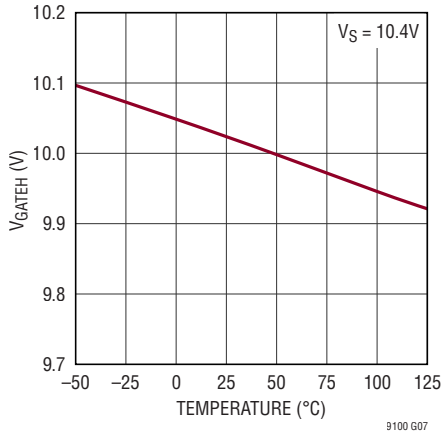
V_{CC2} Output Voltage vs Load Current



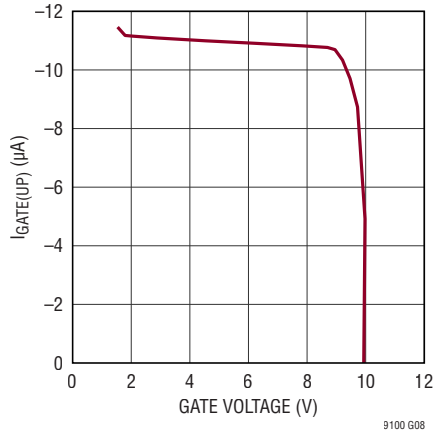
V_{CC2} Output Voltage vs Temperature



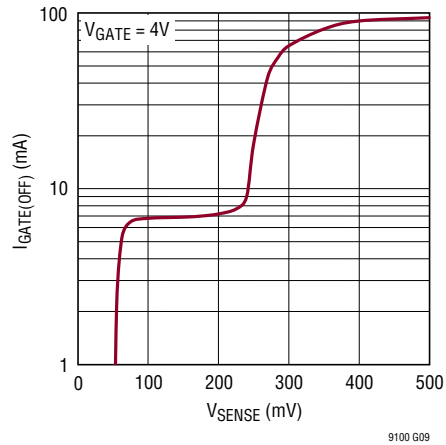
Gate Output High Voltage vs Temperature



Gate Pull-Up Current vs Gate Voltage



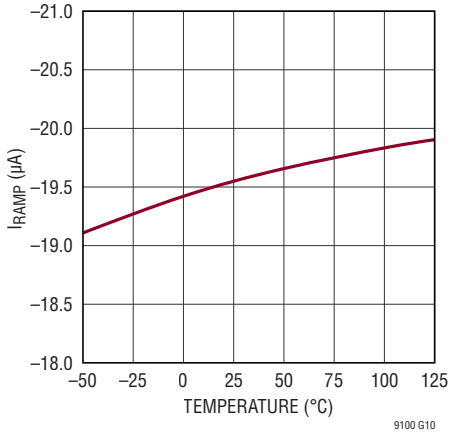
Gate Turn-Off Current vs SENSE Voltage



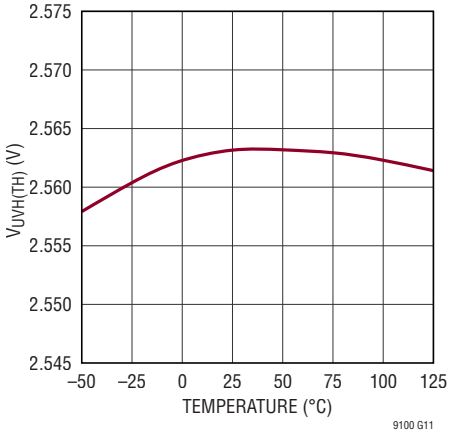
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

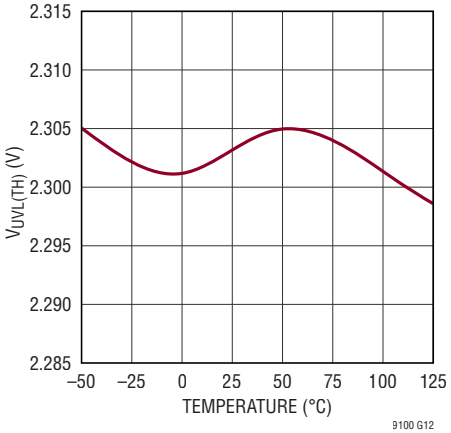
Ramp Pin Current vs Temperature



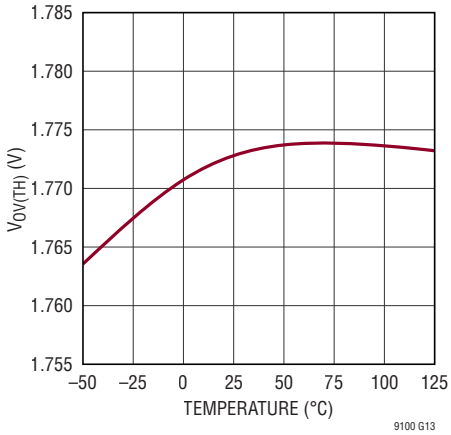
UVH Threshold vs Temperature



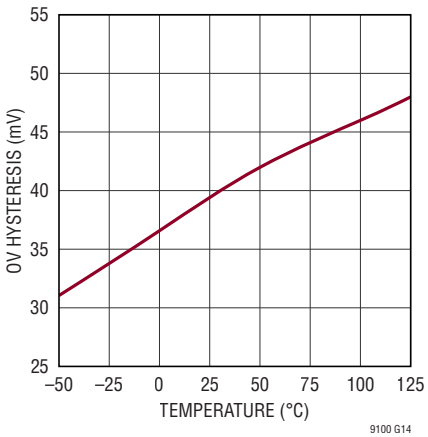
UVL Threshold vs Temperature



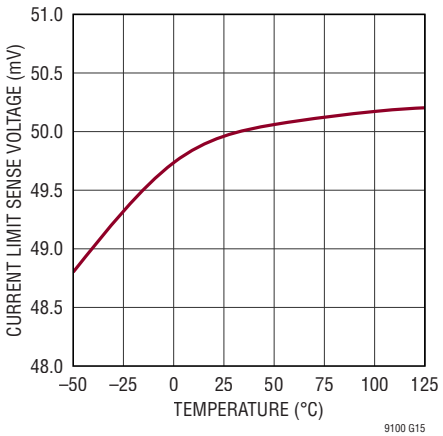
OV Threshold vs Temperature



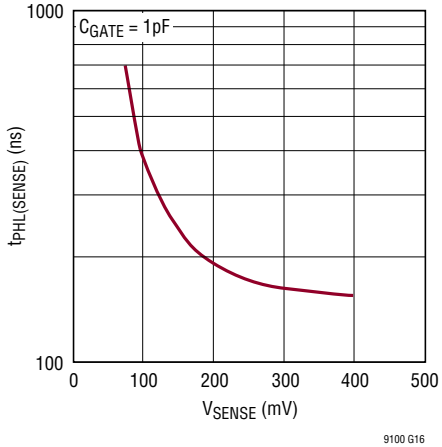
OV Hysteresis vs Temperature



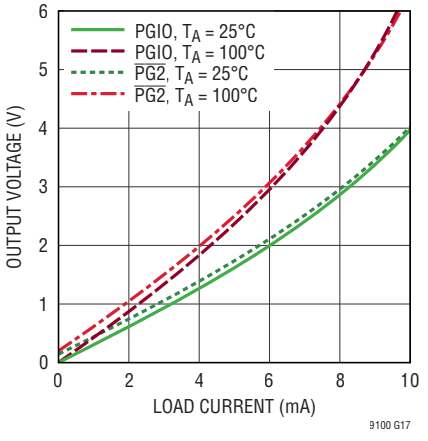
Current Limit Voltage vs Temperature



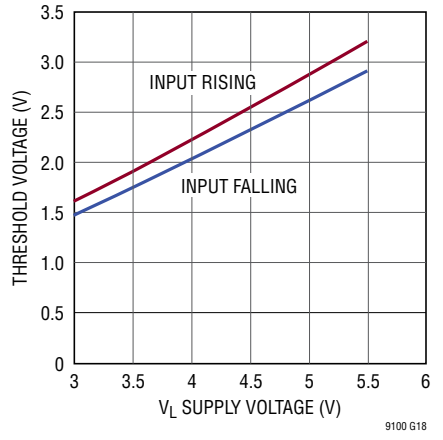
Current Limit Propagation Delay ($t_{PHL(SENSE)}$) vs V_{SENSE}



$\overline{PG2}$, PGIO Output Low Voltage vs Load Current



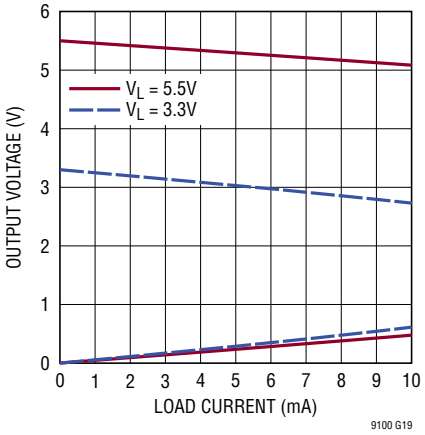
Logic Input Threshold vs V_L Supply Voltage



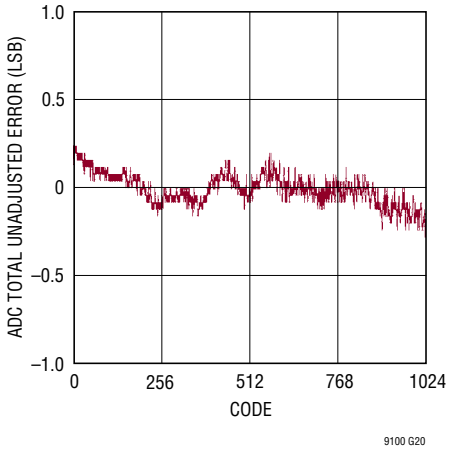
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

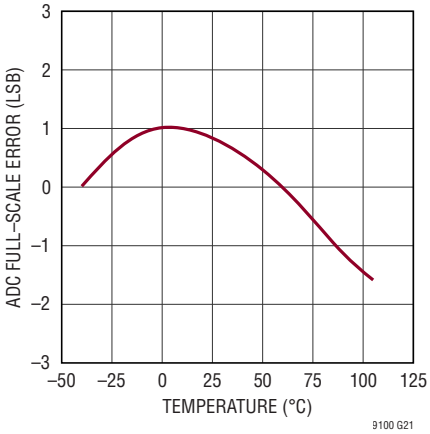
Logic Output Voltage vs Load Current



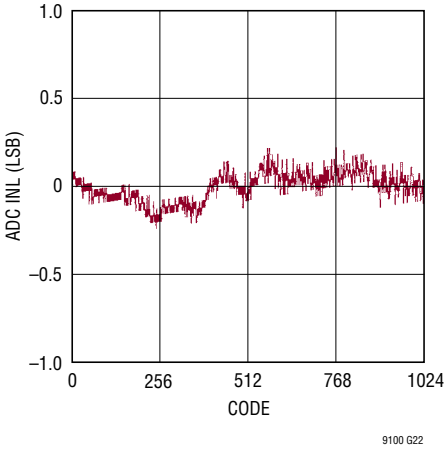
ADC Total Unadjusted Error vs Code (ADIN Pin)



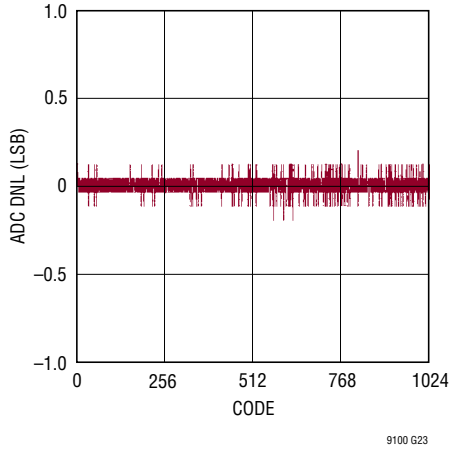
ADC Full-Scale Error vs Temperature (ADIN Pin)



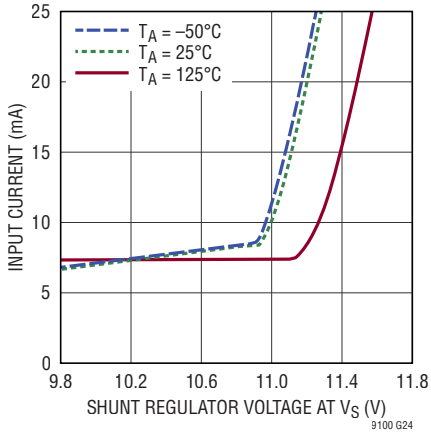
ADC INL vs Code (ADIN Pin)



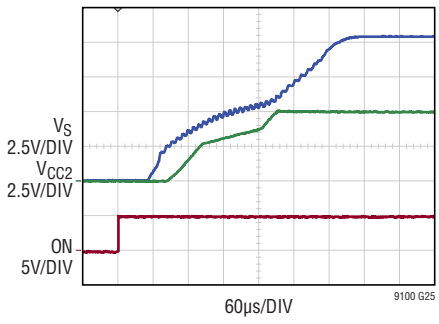
ADC DNL vs Code (ADIN Pin)



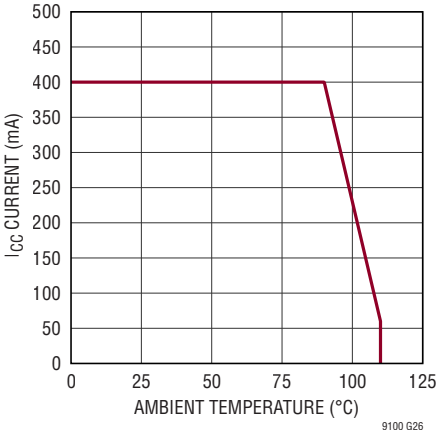
Input Current vs Shunt Regulator Voltage



Power-On Sequence



Derating for 125°C Maximum Internal Operating Temperature



PIN FUNCTIONS

Logic Side

$\overline{PG}$ (A1): Power Good Status Output, Referenced to V_L and GND. This logic pin pulls low and stays latched two timer delays after the isolated side power switch is on (when GATE reaches approximately 9.5V and DRAIN is within 1.77V of V_{EE}). The power good output is reset in all GATE pull-down events except an overvoltage fault. Under the condition of an isolation communication failure this output is in a high impedance state. A communication failure may occur due to extreme electromagnetic events including common mode transients or electrical overstress. Communication is automatically re-established if permanent damage has not occurred.

$\overline{ALERT}$ (A2): Fault Alert Output, Referenced to V_L and GND. This logic pin pulls low when an isolated side fault occurs as configured by the I²C ALERT register. See Applications Information. Under the condition of an isolation communication failure this output is in a high impedance state.

EN (A3): GATE Enable Input, Referenced to V_L and GND. A rising edge turns on the isolated side GATE pin while a falling edge turns it off. This pin is also used to configure the state of bit 3 (GATE_CTRL) in the I²C CONTROL (D) register (and hence the GATE pin) at power-up. For example if EN is tied high, then register bit D3 goes high one timer cycle after power-up. Likewise, if the EN pin is tied low, then the GATE pin remains low after power-up until the EN pin is transitioned high. The GATE pin may be controlled directly by I²C via register bit D3. A high to low transition clears any driver faults. Connect to V_L if not used.

SDA (A4): Serial I²C Data Pin, Referenced to V_L and GND. Bidirectional logic pin connected to isolated side SDA2 pin and configurable switch driver through isolation barrier. An external pull-up resistor or current source is required. Under the condition of an isolation communication failure this pin is in a high impedance state. Connect to V_L if not used.

SCL (A5): Serial I²C Clock Pin, Referenced to V_L and GND. Logic input connected to isolated side SCL2 pin and configurable switch driver through isolation barrier. An external pull-up resistor or current source is required. Connect to V_L if not used.

ON (A6): Module Enable Pin. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state, and the isolated side is unpowered. The ON pin may be used to enable the isolated side power switch driver by connecting EN to V_L. A low to high transition of ON would then enable the isolated side gate drive after the internal isolated side supply voltage exceeds approximately 9V followed by a timer delay. Connect to V_L if not used.

V_L (A7): Logic Supply. Interface supply voltage for pins $\overline{PG}$, $\overline{ALERT}$, EN, SDA, SCL, and ON. Operating voltage is 3V to 5.5V. Internally bypassed with 1µF.

GND (B1 TO B5): Circuit Ground.

V_{CC} (B6, B7): Isolated Power Converter Supply Voltage. Operating voltage is 4.5V to 5.5V. Internally bypassed with 1µF. This pin may be left unconnected or grounded if V_S is driven by an external voltage.

Isolated Side

$\overline{PG2}$ (P1): Power Good Status Output, Referenced to V_{CC2} and V_{EE}. This logic pin pulls low and stays latched two timer delays after the power switch is on (when GATE reaches approximately 9.5V and DRAIN is within 1.77V of V_{EE}). The power good output is reset in all GATE pull-down events except an overvoltage fault. Internally connected to V_{CC2} by a 10k resistor.

$\overline{ALERT2}$ (P2): Fault Alert Output, Referenced to V_{CC2} and V_{EE}. This logic pin pulls low when an isolated side fault occurs as configured by the I²C ALERT register. See Applications Information. Internally connected to V_{CC2} through a 10k resistor.

EN2 (P3): Enable Output, Referenced to V_{CC2} and V_{EE}. Logic output connected to logic side EN pin through isolation barrier and 4k resistor and to the switch driver. EN2 may be driven externally, see Applications Information. Internally connected to V_{EE} through 4k and 10k resistors.

SDA2 (P4): Serial I²C Data Pin, Referenced to V_{CC2} and V_{EE}. Bidirectional logic pin connected to logic side SDA pin through isolation barrier and to the switch driver. Allows for I²C bus expansion. Output is biased high by a

PIN FUNCTIONS

1.8mA current source. Under the condition of an isolation communication failure this output defaults to a high state.

SCL2 (P5): Serial I^2C Clock Output, Referenced to V_{CC2} and V_{EE}. Logic output connected to logic side SCL pin through isolation barrier and to the switch driver. Allows for I^2C bus expansion. Clock is unidirectional from logic to isolated side. Under the condition of an isolation communication failure this output defaults to a high state.

PGIO (P6): General Purpose Input/Output. Logic input and open-drain output. Default is output which pulls low two timer delays after the $\overline{PG}$ pin goes low to indicate a second power good output. Configure according to Table 4.

V_S (P7): 10.4V Nominal Isolated Supply Output Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 10.4V. V_S may be driven by an external supply if V_{CC} is not connected or grounded. If driven externally connect pin to a positive supply through a dropping resistor, see Applications Information. An internal shunt regulator clamps V_S (V_Z) at 11.2V. An undervoltage lockout (UVLO) circuit holds GATE low until V_S is above 9V. Internally bypassed with 1µF.

V_{EE} (R1 to R3, R5 to R7): Isolated Circuit Common.

ADR0, ADR1 (R4, S4): Serial Bus Address Inputs, Referenced to V_{CC2} and V_{EE}. Connecting these pins to V_{EE}, V_{CC2}, or floating configures one of nine possible addresses. See Table 1 in Applications Information.

$SENSE^-$ (S1): Negative Current Limit Sense Input. Kelvin connection for external current sense resistor (R_S). Internally filtered with 220pF.

SS (S2): Soft-Start Input. This pin is used to ramp inrush current during start-up, thereby effecting control over di/dt. Pin connected internally to a 220nF capacitor, additional external capacitance (C_{SS}) may be added. An internal 10µA current source charges the internal and external capacitance creating a voltage ramp. This voltage is converted to a current to charge the GATE pin up and to ramp the output voltage down. The SS pin is internally clamped to 2.56V limiting $I_{GATE(UP)}$ to 11.5µA and I_{RAMP} to 20µA.

TMR (S3): Delay Timer Input. This pin is used to create timing delays at power-up, when power good outputs pull down and when auto-retrying after faults (except overvoltage fault). Pin connected internally to a 47nF capacitor, additional external capacitance (C_{TMR}) may be added to extend the nominal delay beyond 12ms. Internal pull-up currents of 10µA and 5µA and pull-down currents of 5µA and 12mA configure the delay periods as multiples of a nominal delay t_D = 12ms + 256ms • C_{TMR}/µF. Delays for power-up and auto-retry following an undervoltage fault are the same as the nominal delay. Delays for sequenced power good outputs are twice the nominal delay. Delay for auto-retry following overcurrent fault are four times the nominal delay.

ADIN2, ADIN (S5, S6): ADC Inputs, Referenced to V_{EE}. A voltage between 0V and 2.56V applied to these pins is measured by the internal module ADC. Connect to V_{EE} if unused.

V_{CC2} (S7): 5V Nominal Isolated Supply Output Voltage. Linear regulated output generated from V_S with a UVLO threshold of 4.25V. This voltage powers up the isolated data converter and logic control circuitry. Internally bypassed with 1µF.

$SENSE^+$ (T1): Positive Current Limit Sense Input. Load current through an external current sense resistor (R_S) is monitored and controlled by an active current limit amplifier to 50mV/R_S. Once V_{SENSE} reaches 50mV, a circuit breaker timer starts and turns off the switch after 530µs. In the event of a catastrophic short-circuit, if V_{SENSE} crosses 250mV, a fast response comparator immediately pulls the GATE pin down to turn off the MOSFET. Internally filtered with 220pF.

GATE (T2): N-Channel MOSFET Switch (FET) Gate Drive Output. This pin is pulled up by an internal current source I_{GATE} (11.5µA when the SS pin reaches its clamping voltage). GATE stays low until V_S and V_{CC2} cross the UVLO thresholds, EN is high, UV and OV conditions are satisfied and the adjustable power-up timer delay expires. During turn-off, caused by faults or undervoltage lockout, a 110mA pull-down current between GATE and V_{EE} is activated. Internally filtered with 220pF. Under the condition of an isolation communication failure the switch is turned off.

DRAIN (T3): Drain Sense Input. Connect an external resistor between this pin and the drain terminal of the FET. Size the resistor for 50µA nominal current, do not exceed

PIN FUNCTIONS

2mA. The voltage at this pin is internally clamped to 4V. When the DRAIN pin voltage is less than 1.77V and the GATE pin voltage is approximately 9.5V the power good output is asserted after two timer delays. Internally filtered with 220pF.

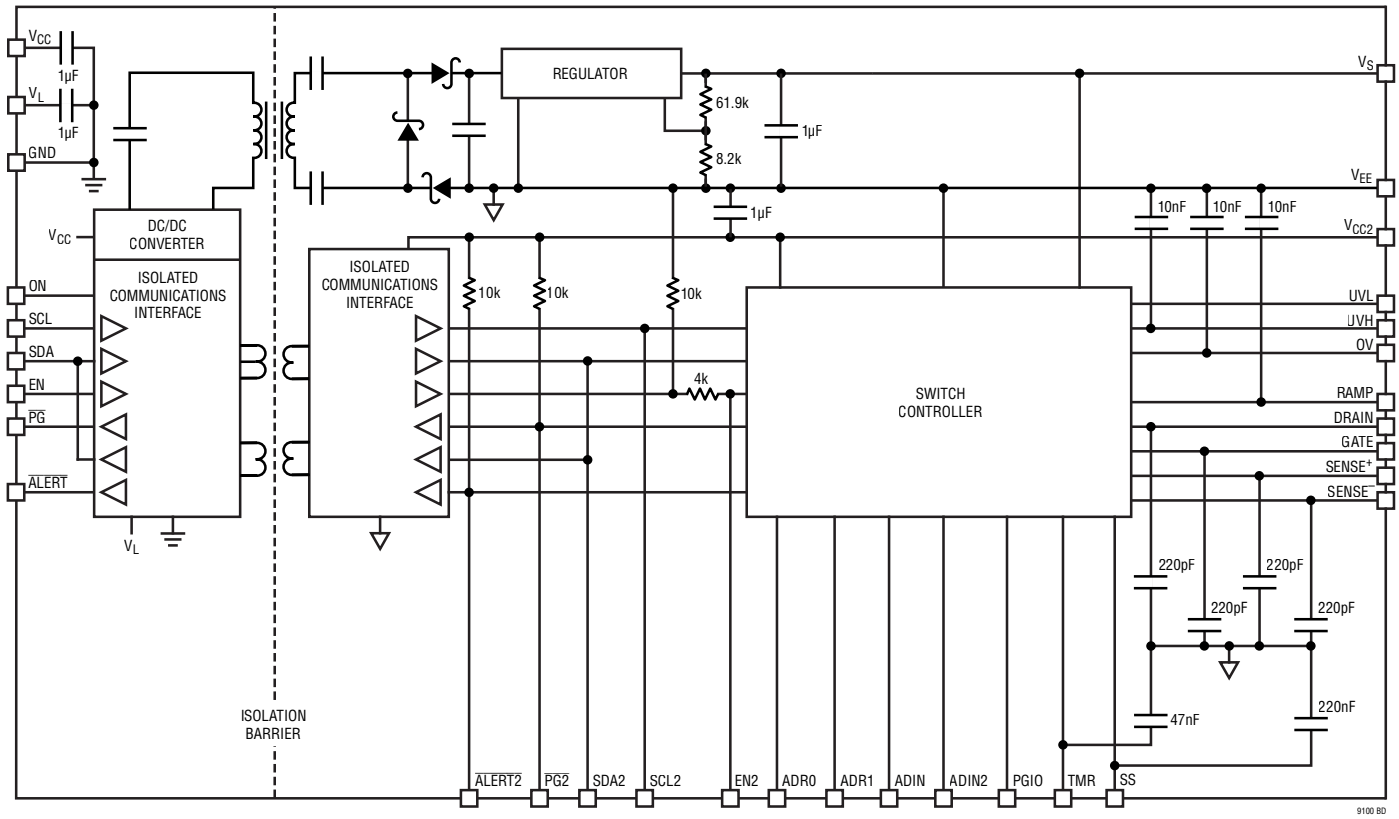
RAMP (T4): Inrush Current Ramp Control Pin. The inrush current is adjusted by placing a capacitor (C_R) between the RAMP pin and the drain terminal of the FET. At start-up, the GATE pin is pulled up by $I_{GATE(UP)}$ until the FET begins to turn on. A current, I_{RAMP}, then flows through C_R to ramp down the drain voltage. The value of I_{RAMP} is controlled by the SS pin voltage. When the SS pin reaches its clamp voltage (2.56V), I_{RAMP} = 20µA. For a capacitive load the RAMP rate of the FET drain voltage (V_{DRAIN}) and the load capacitor C_L set the inrush current: $I_{INRUSH} = (C_L/C_R) \bullet I_{RAMP}$. Internally filtered with 10nF; see Applications Information.

OV (T5): Overvoltage Detection Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at this pin rises above 1.77V, the FET is turned off. The overvoltage condition does not affect the status of the power good outputs. Internally filtered with 10nF. Connect to V_{EE} if not used.

UVH (T6): Undervoltage High Level Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the UVH pin rises above 2.56V and UVL is above 2.291V, the FET is allowed to turn on. Internally filtered with 10nF. Connect to V_{CC2} if not used.

UVL (T7): Undervoltage Low Level Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the UVL pin drops below 2.291V and UVH is below 2.56V, the FET is turned off and the power good outputs go high. Pulling this pin below 1.21V resets faults and allows the FET to turn back on. Connect to V_{CC2} if unused.

BLOCK DIAGRAM



TEST CIRCUITS

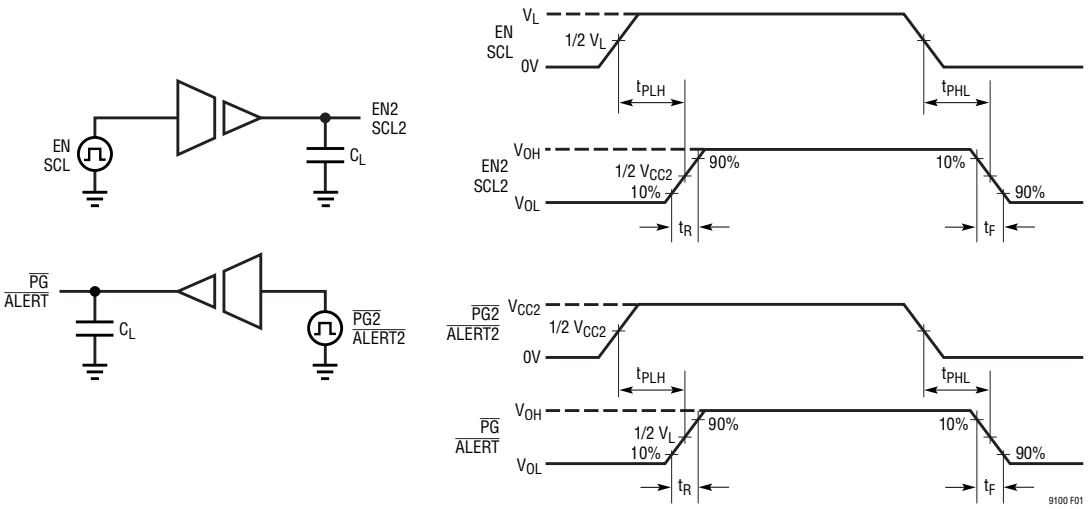


Figure 1. Logic Timing Measurements

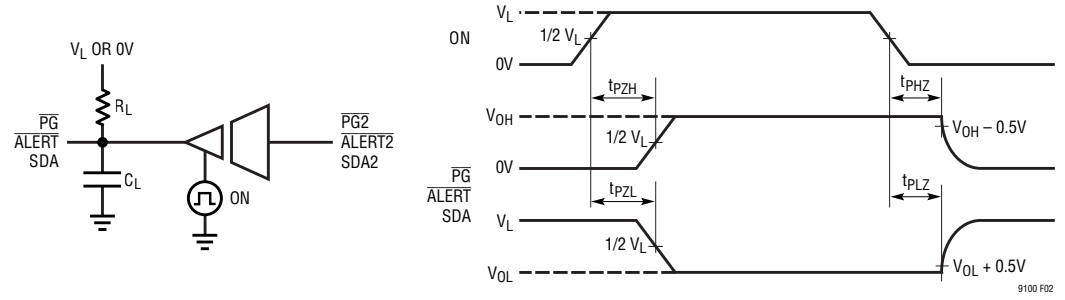


Figure 2. ON Enable/Disable Time

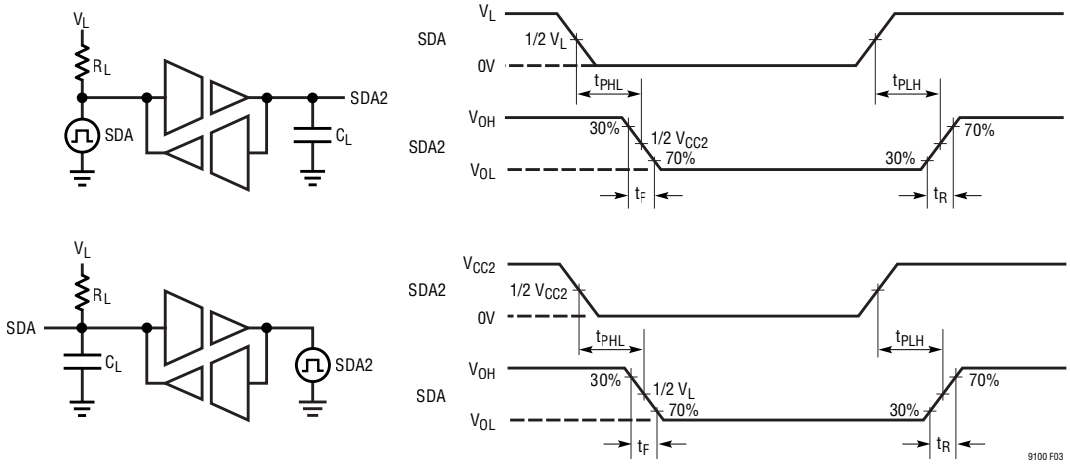


Figure 3. I²C Timing Measurements

APPLICATIONS INFORMATION

Overview

The LTM9100 µModule switch controller provides a galvanically-isolated robust driver interface, complete with decoupling capacitors. The LTM9100 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM9100 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common-mode events as fast as 70kV/µs providing excellent noise isolation.

The LTM9100 is designed to turn a supply voltage on and off in a controlled manner. In normal operation after initial power up and time delay (TMR), the GATE pin turns on a FET passing power to the load. The GATE pin is powered by an internal isolated DC/DC converter with output voltage (V_S) of approximately 10.4V.

An amplifier connected to the SENSE pins is used for overcurrent and short-circuit protection. It monitors the load current through an external sense resistor R_S. In an overcurrent condition, the current is limited to 50mV/R_S by regulating GATE. If the overcurrent condition remains for more than 530µs, GATE is turned off.

The DRAIN and GATE voltages are monitored to determine if the FET is fully enhanced. Upon successful turn on of the FET, two power good signals are presented on the $\overline{PG}$ and PGIO pins. They allow enabling and sequencing of loads. The PGIO pin can also be configured for a general purpose input or output.

The isolated side logic circuits are powered by an internally generated 5V supply (V_{CC2}). Prior to turning on the FET, both the internal gate drive supply voltage V_S and V_{CC2} voltages must exceed their undervoltage lockout thresholds. In addition, the control inputs UVH, UVL, OV and EN are monitored. The FET is held off until all start-up conditions are met.

A 10-bit analog-to-digital converter (ADC) is included in the LTM9100. The ADC measures the SENSE voltage as well as voltages at the ADIN2 and ADIN pins, for auxiliary functions such as sensing bus voltage or temperature, etc.

An I^2C interface is provided to read the ADC data registers. It also allows the host to poll the device and determine if a fault has occurred. If the ALERT line is used as an interrupt, the host can respond to a fault in real time. Two three-state pins, ADR0 and ADR1, are used to program eight possible device addresses.

The interface can also be pin configured for a single-wire broadcast mode, sending ADC data and fault status through the SDA pin to the host without clocking the SCL line. This single-wire, one-way communication can simplify system design.

The LTM9100 is ideally suited for distributed DC power systems and off-line power converter systems requiring an isolated communication and control interface. A basic 200W –48V distributed power application circuit using the LTM9100 is shown in Figure 4.

APPLICATIONS INFORMATION

µModule Technology

The LTM9100 utilizes isolator µModule technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the µModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with multiple regulators and powerful isolated DC/DC converter in one small package.

DC/DC Converter

The LTM9100 contains a fully integrated DC/DC converter, including the transformer, so that no external components are necessary for powering the isolated side. The logic side contains a full-bridge driver, running at 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a symmetric voltage doubler. This topology reduces common mode voltage perturbations on the isolated side ground, and eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated 10.4V output (V_S) for the GATE driver supply. V_S is decoupled internally by a 1µF capacitor.

The data converter and logic control circuits are powered by an internal linear regulator that derives 5V from the V_S supply. The 5V output is available at the V_{CC2} pin for driving external circuits (up to 15mA load current). V_{CC2} is decoupled internally by a 1µF capacitor.

Powering the LTM9100 from the Bus

The internal isolated power converter may be disabled by floating or grounding the V_{CC} pin. Isolated power may then be derived from the external bus voltage by using either a low or high side circuit depending upon the application's location of the LTM9100.

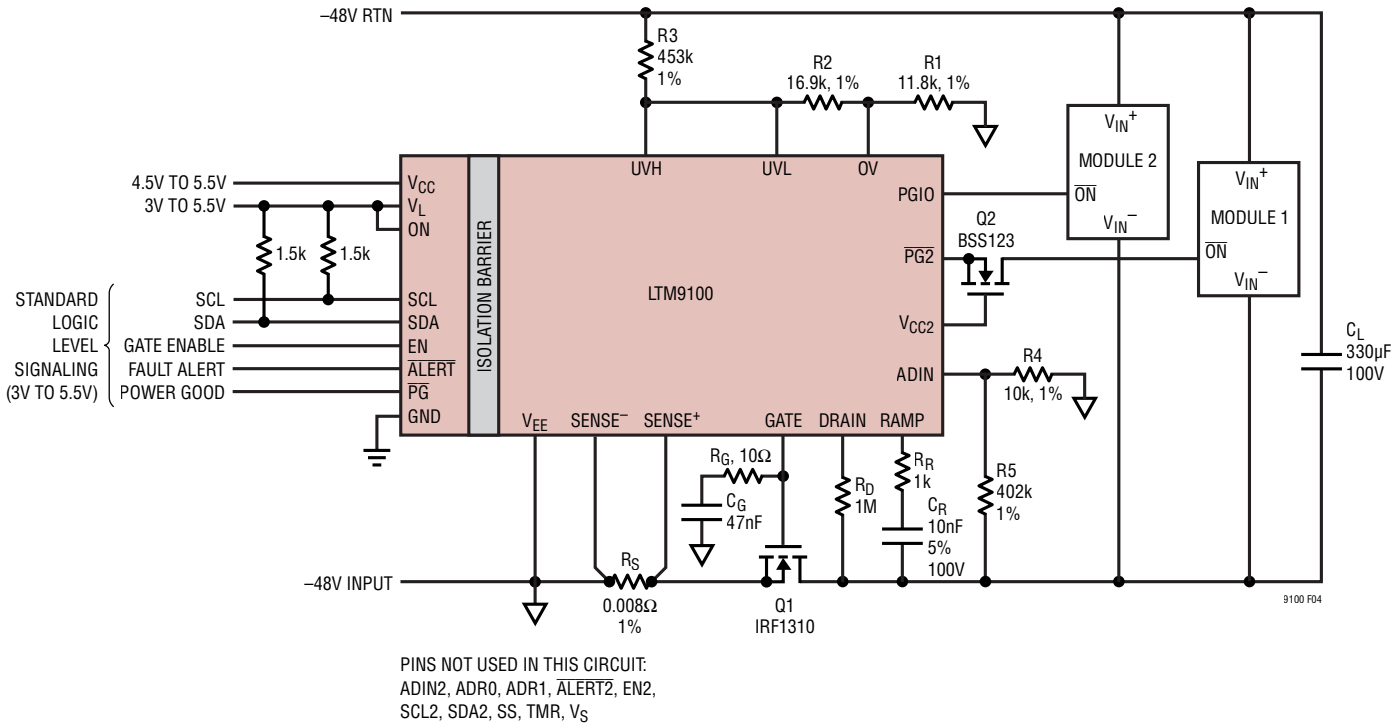


Figure 4. –48V/200W Low Side Hot Swap Controller Using LTM9100 with Current and Input Voltage Monitoring (5.6A Current Limit, 0.66A Inrush)

APPLICATIONS INFORMATION

Low Side Applications

Isolated power may be derived through a current limiting resistor (R_{LIM}) to the V_S pin (Figure 5) for low side configurations where V_{EE} is referenced to the negative side of the bus supply voltage. An internal shunt regulator clamps the voltage at V_S to 11.2V (V_Z) and provides power to the GATE driver. R_{LIM} should be chosen to accommodate the maximum isolated side supply current requirement of the LTM9100 (10mA), plus the supply current required by any external devices connected to V_S and V_{CC2}, at the minimum VBUS operation voltage. Alternative means of current limiting can also be used, e.g. an analog (active) current limiter (ACL).

$$R_{LIM} \leq \frac{VBUS_{(MIN)} - V_{Z(MAX)}}{I_{S(EXT)} + I_{CC2(EXT)} + 10mA}$$

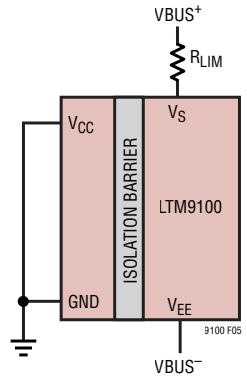


Figure 5. Isolated Side Power Derived From External Bus

$$P_{MAX} = \frac{[VBUS_{(MAX)} - V_{Z(MIN)}]^2}{R_{LIM}}$$

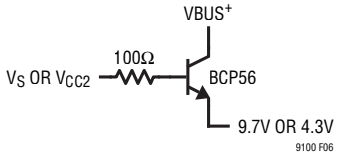


Figure 6. NPN Buffer Relieves R_{LIM} of Excessive Dissipation when Supplying External Loads

High Side Applications

For high side applications it is necessary to generate a voltage > V_Z volts above the bus voltage to power the LTM9100 once the FET is fully conducting; drain voltage near V_{EE}. Initially the LTM9100 can be powered directly from the bus until the FET drain drops below the minimum V_S voltage for operation. Note the V_S supply current flows through the load and will charge any load capacitance even when GATE is off. If the LTM9100 is configured to turn on the GATE upon application of bus voltage this is not an issue.

For bus voltages ≤100V the circuit of Figure 7 may be used. The step-up converter circuit provides an output voltage ~12V higher than the bus voltage, connecting to V_S through an ACL (depletion MOSFET Q1, R_{LIM}). For bus voltages >100V it is necessary to preregulate the input voltage to the step up converter, as shown in Figure 8. Any type of step up converter can be used to provide the boosted voltage: flyback, boost, charge pump, etc. Transistors Q1, Q3, and diode D1 must be selected based on the bus voltage and power dissipation.

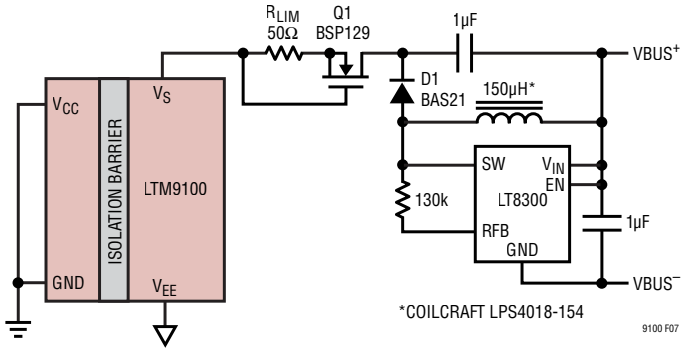


Figure 7. V_S Supply for VBUS ≤ 100V

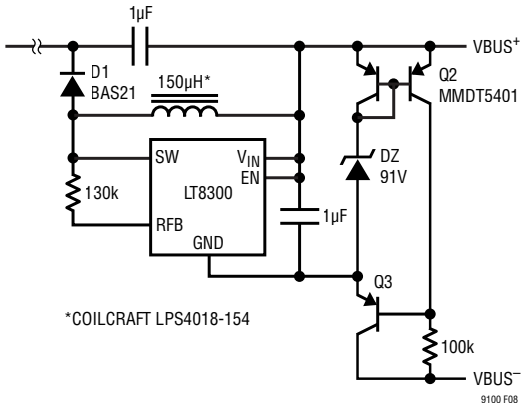


Figure 8. Preregulator for VBUS > 100V

APPLICATIONS INFORMATION

Switching the PowerPath™

For either low side or high side configuration, the internal DC/DC converter may be subsequently enabled and external isolated side converter disabled to minimize power dissipation. The circuit of Figure 9 uses the power good signals to automatically switch the power converter path once the main FET is on.

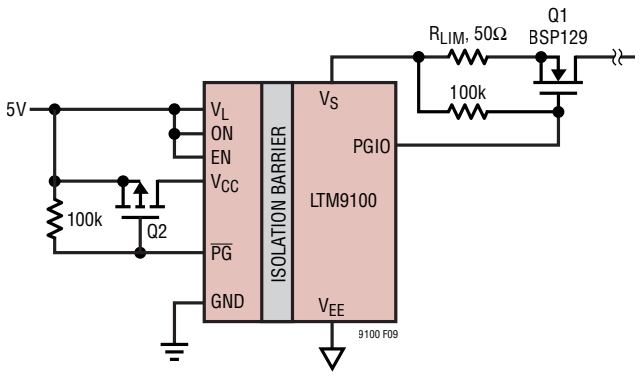


Figure 9. External-to-Internal PowerPath Switch-Over

V_L Logic Supply

A separate logic supply pin V_L allows the LTM9100 to interface with any logic signal from 3V to 5.5V as shown in Figure 10. Simply connect the desired logic supply to V_L.

There is no interdependency between V_{CC} and V_L; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order. V_{CC} and V_L are decoupled internally by 1µF capacitors.

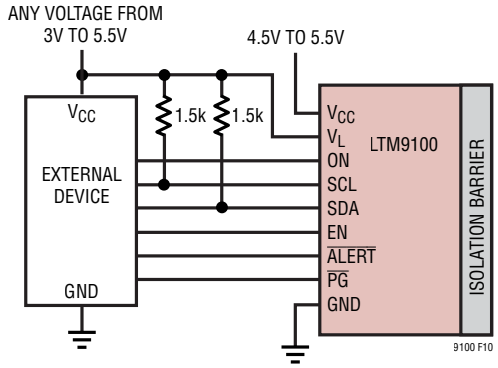


Figure 10. V_{CC} and V_L Are Independent

Hot Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM9100's power supplies, V_{CC} or V_L, due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high-Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM9100. Refer to Linear Technology Application Note AN88, entitled Ceramic Input Capacitors Can Cause Overvoltage Transients for a detailed discussion.

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals are assembled as a serial packet and transferred across the isolation barrier. The time required to transfer all three bits is 50ns typical, and sets the limit for how often a signal can change on the opposite side of the barrier. The technique used assigns SCL on the logic side and $\overline{PG2}$ on the isolated side the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically ±6ns, but may vary up to ±44ns if the low priority channels are not encoded within the same high priority serial packet.

Initial Start-Up and Inrush Control

Several conditions must be satisfied before the FET turn-on sequence is started. First the voltage at V_S must exceed its 9V undervoltage lockout level. Next the internal supply V_{CC2} must cross its 4.25V undervoltage lockout level. This generates a 100µs to 160µs power-on-reset pulse during which the FAULT register bits are cleared and the CONTROL register bits are set or cleared as described in the register section. After the power-on-reset pulse, the voltages at the UVH, UVL and OV pins must satisfy UVH > 2.56V, UVL > 2.291V and OV < 1.77V. All the above conditions must be satisfied throughout the duration of the start-up delay that is set by a combination of internal and external (C_{TMR}) capacitance connected to the TMR pin. C_{TMR} is charged with a pull-up current of 10µA until

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the voltage at TMR reaches 2.56V. C_{TMR} is then quickly discharged with a 12mA current. The initial delay expires when TMR is brought below 75mV. The duration of the start-up delay is given by:

$$t_D \cong 12ms + 256ms \bullet \frac{C_{TMR}}{1\mu F}$$

If any of the above conditions is violated before the start-up delay expires, C_{TMR} is quickly discharged and the turn-on sequence is restarted. After all the conditions are validated throughout the start-up delay, the EN pin is then checked. If it is high, the FET will be turned on. Otherwise, the FET will be turned on when the EN pin is raised or bit 3 (GATE_CTRL) in the CONTROL (D) register is set to 1 through the I^2C interface, when configured for I^2C only control.

The FET turn-on sequence follows by charging an internal and external (C_{SS}) capacitor at the SS pin with a 10µA pull-up current and the voltage at SS (V_{SS}) is converted to a current ($I_{GATE(UP)}$) of 11.5µA • V_{SS}/2.56V for GATE pull-up. When the GATE reaches the FET threshold voltage, current starts to flow through the FET and a current (I_{RAMP}) of 20µA • V_{SS}/2.56V flows out of the RAMP pin and through an external capacitor (C_R) connected between RAMP and the drain voltage. The SS voltage is clamped to 2.56V, which corresponds to $I_{GATE(UP)}$ = 11.5µA and I_{RAMP} = 20µA. The RAMP pin voltage is regulated at 1.1V and the ramp rate of V_{DRAIN} determines the inrush current for capacitive load:

$$I_{INRUSH} = 20\mu A \bullet \frac{C_L}{C_R}$$

The ramp rate of V_{SS} determines the di/dt of the inrush current:

$$\frac{dI_{INRUSH}}{dt} = 20\mu A \bullet \frac{C_L}{C_R} \bullet \frac{1\mu F}{256ms \bullet (C_{SS} + 220nF)}$$

If C_{SS} is absent externally, the SS ramps from 0V to 2.56V in approximately 56ms.

When V_{DRAIN} is ramped down to V_{EE}, I_{GATE} returns to the GATE pin and pulls the GATE up to V_{GATEH}. Figure 11 illustrates the start-up sequence of the LTM9100.

During live board insertion or input power step, an internal clamp turns on to hold the RAMP pin low. Resistor R_R and an internal 10nF capacitor to V_{EE} suppress noise at the RAMP pin. For proper operation, $R_R \bullet C_R$ should not exceed 50µs. Additional capacitance may be added from RAMP to V_{EE} for additional noise filtering.

Power Good Monitors

When the voltage across the FET falls below 1.77V and GATE pulls above approximately 9V, an internal power good signal is latched and a series of two delay cycles are started as shown in Figure 11. When the first delay cycle with a duration of $2t_D$ expires, the $\overline{PG2}$ and $\overline{PG}$ pins pull low as power good signals. When the second delay cycle ($2t_D$) expires, the PGIO pin pulls low as another power good signal. The $2t_D$ timer delay is obtained by charging the capacitance on TMR with a 5µA current and discharging with 12mA when TMR reaches 2.56V. The power good signals at $\overline{PG}$ and PGIO are reset in all FET turn-off conditions except the overvoltage fault.

Turn-Off Sequence and Auto-Retry

In any of the following conditions, the FET is turned off by pulling down GATE with a 110mA current, and the capacitances at SS and TMR are discharged with 12mA currents.

1. The EN (or EN2) pin is low or register bit D3 is set to 0.
2. The voltage at UVL is lower than 2.291V and the voltage at UVH is lower than 2.56V (undervoltage fault).
3. The voltage at OV is higher than 1.77V (overvoltage fault).
4. The voltage at V_S is lower than 8.5V (V_S undervoltage lockout).
5. The voltage at V_{CC2} is lower than 4.25V (V_{CC2} undervoltage lockout).
6. V_{SENSE} > 50mV and the condition lasts longer than 530µs (overcurrent fault).

For conditions 1, 4, 5, after the condition is cleared, the LTM9100 will automatically enter the FET turn-on sequence as previously described.

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For any of the fault conditions 2, 3, 6, the FET off mode is programmable by the corresponding auto-retry bit in the CONTROL register. If the auto-retry bit is set to 0, the FET is latched off upon the fault condition. If the auto-retry bit is set to 1, after the fault condition is cleared, the delay timer is started. After the timer expires, the FET enters the auto-retry mode and GATE is pulled up. The auto-retry delay following the undervoltage fault has a duration of t_D. The auto-retry delay following the overcurrent fault has a duration of $4t_D$ for extra cooling time. The auto-retry following the overvoltage fault does not have a delay. The auto-retry control bits and their defaults at power up are listed in Table 4. Note that the LTM9100 defaults to latch-off following the overcurrent fault.

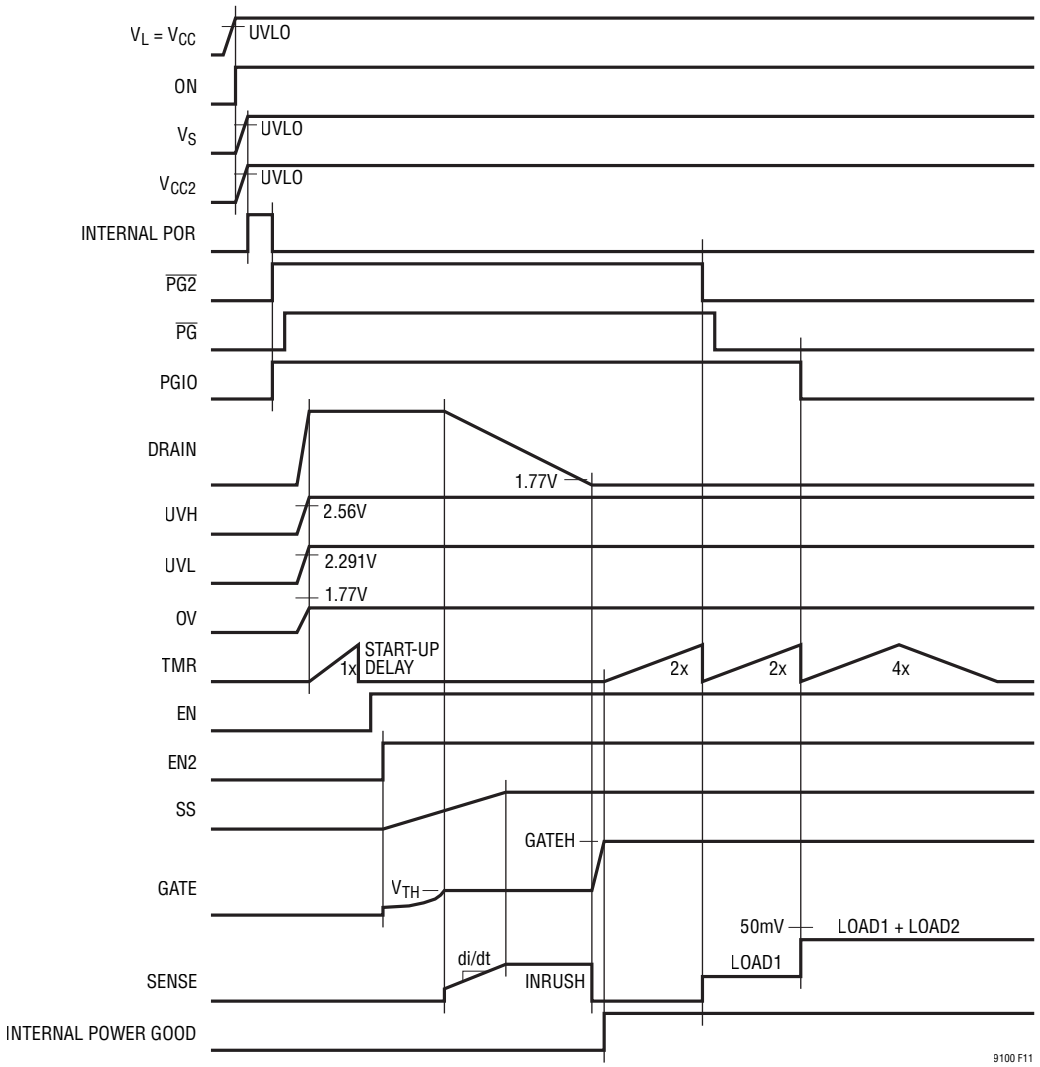

Figure 11. LTM9100 Turn-On Sequence

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Turning the GATE Pin (External FET) On

Many methods of on/off control are possible using the ON, EN, EN2, UV/OV or PGIO pins along with the I²C port. The EN pin works well with logic inputs or floating switch contacts; I²C control is intended for systems where the board operates only under command of a central control processor and the ON pin is useful with systems with low standby current requirements. The UV (UVH, UVL) and OV pins are useful with signals referenced to V_{EE}. PGIO controls nothing directly, but is useful for I²C monitoring of connection sense or other important signals.

On/off control is possible with or without I²C intervention. Even when operating autonomously, the I²C port can still exercise control over the GATE output, although depending on how they are connected, EN, EN2, and ON could subsequently override conditions set by I²C. UV, OV and other fault conditions seize control as needed to turn off the GATE output, regardless of the state of EN, EN2, ON or the I²C port. Figure 12 shows five configurations of on/off control of the LTM9100.

Logic Control with Isolation: Figure 12a shows an application using logic signal control. Rising and falling edges of either the ON pin or EN pin, with alternate pin tied high, turn the GATE output on and off. Rising edge control of ON results in a delay of the GATE signal by the power converter turn-on time and one t_D period, the falling edge will also be delayed by the converter discharge time (stored energy) and supply loading on V_S and V_{CC2}. The GATE will respond immediately to changes on the EN pin. The status of EN can be examined or overridden through the I²C port at register bit D3. Register bit D3 is set low whenever V_{CC2} drops below its UVLO threshold. The status of the GATE pin output is indicated by register bit A7 (GATE_STAT), which is equal to register bit D3 and the absence of UV, OV, and other faults.

Bootstrapped Power Connection: Figure 12b shows a low side application with control power derived on the isolated side. With EN2 tied high on the isolated side, GATE rises one t_D period after power is applied. The logic supply (V_L) or ON pin may be toggled either before or after the bus voltage is applied provided the EN pin is tied high, without interfering with the GATE signal.

Ejector Switch or Loop-Through Connection Sense: Floating switch contacts, or a connection sense loop work well with the EN or EN2 pins. Figure 12c illustrates this configuration using the EN2 pin and includes a debounce delay.

Short Pin to RTN: Figure 12d uses the UV divider string to detect board insertion. The short pin connection could also be wired to work in conjunction with either the ON or EN pins.

I²C Only Control: To lock out EN and ON, use the configuration shown in Figure 12e and control the GATE pin with register bit D3. The circuit defaults off at power up with EN2 tied to V_{EE}. To default on, do not connect EN2. The PGIO pin can be used as an input to monitor a connection sense or other control signal. PGIO is configured as an input by setting register bits D6 and D7 high; its input state is stored at register bit A6.

Overcurrent Protection and Overcurrent Fault

The LTM9100 features two levels of protection from short-circuit and overcurrent conditions. Load current is monitored by the SENSE pins and resistor R_S. There are two distinct thresholds for the voltage at SENSE: 50mV for engaging the active current limit loop and starting a 530µs circuit breaker timer and 250mV for a fast GATE pull-down to limit peak current in the event of a catastrophic short-circuit or an input step.

In an overcurrent condition, when the voltage drop across R_S exceeds 50mV, the current limit loop is engaged and an internal 530µs circuit breaker timer is started. The current limit loop servos the GATE to maintain a constant output current of 50mV/R_S. When the circuit breaker timer expires, the FET is turned off by pulling GATE down with a 110mA current, the capacitors at SS and TMR are discharged and the power good signals are reset. At this time, the overcurrent present bit A2 and the overcurrent fault bit B2 are set, and the circuit breaker timer is reset.

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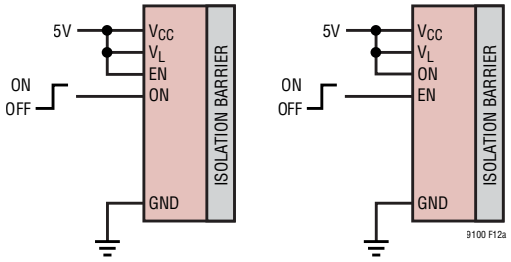
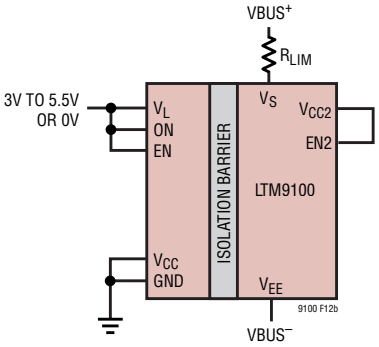
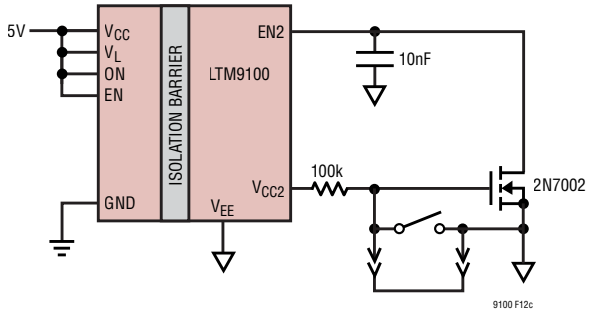


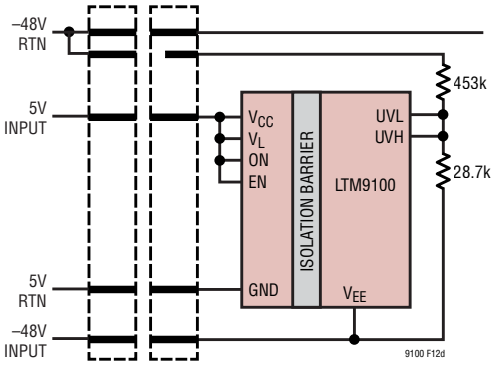
12(a) Logic Input Control



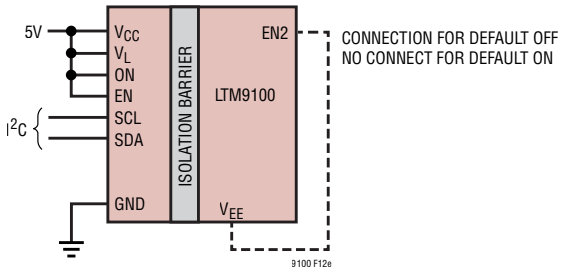
12(b) Bootstrapped Power Connection



12(c) Contact Debounce Delay Upon Insertion for Use with an Ejector Switch or Loop-Through Style Connection Sense



12(d) Short Pin Connection Sense to RTN



12(e) I²C Only Control

Figure 12. On/Off Control of the LTM9100

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After the FET is turned off, the overcurrent condition register bit A2 is cleared. If the overcurrent auto-retry register bit D2 has been set, the switch will turn on again automatically after a cooling time of $4t_D$. Otherwise, the FET will remain off until the overcurrent fault register bit B2 is reset. When the overcurrent fault bit is reset (see Resetting Faults), the FET is allowed to turn on again after a delay of $4t_D$. The $4t_D$ cooling time associated with the overcurrent fault will not be interrupted by any other fault condition. See Figure 13 for operation of LTM9100 under overcurrent condition followed by auto-retry.

In the case of a low impedance short-circuit on the load side or an input step during battery replacement, current overshoot is inevitable. A fast SENSE comparator with a threshold of 250mV detects the overshoot and immediately pulls GATE low. Once the SENSE voltage drops to 50mV, the current limit loop takes over and servos the current as previously described. If the short-circuit condition lasts longer than 530µs, the FET is shut down and the overcurrent fault is registered.

In the case of an input step, after an internal clamp pulls the RAMP pin down to 1.1V, the inrush control circuit takes over and the current limit loop is disengaged before the circuit breaker timer expires. From this point on, the device works as in the initial start-up: V_{DRAIN} is ramped down at the rate set by I_{RAMP} and C_R followed by GATE pull-up. The power good signals on the $\overline{PG}$ and PGIO pins, the TMR pin, and the SS pin are not interrupted through the input step sequence. The waveform in Figure 14 shows how the LTM9100 responds to an input step.

Note that the current limit threshold should be set sufficiently high to accommodate the sum of the load current and the inrush current to avoid engagement of the current limit loop in the event of an input step. The maximum value of the inrush current is given by:

$$I_{INRUSH} \le 0.8 \bullet \frac{45mV}{R_S} - I_{LOAD}$$

where the 0.8 factor is used as a worst-case margin combined with the minimum SENSE threshold (45mV).

The active current limit circuit is compensated using the capacitor C_G with a series resistor R_G (10Ω) connected between GATE and V_{EE}, as shown in Figure 4. The suggested value for C_G is 47nF. This value should work for most FETs (Q1).

Overvoltage Fault

An overvoltage fault occurs when the OV pin rises above its 1.77V threshold. This shuts off the FET immediately, sets the overvoltage present register bit A0 and the overvoltage fault register bit B0, and pulls the SS pin down. Note that the power good signals are not affected by the overvoltage fault. If the OV pin subsequently falls back below the threshold, the FET will be allowed to turn on again immediately (without delay) unless the overvoltage auto-retry has been disabled by clearing register bit D0.

Undervoltage Comparator and Undervoltage Fault

The LTM9100 provides two undervoltage pins, UVH and UVL, for adjustable UV threshold and hysteresis. The UVH and UVL pin have the following accurate thresholds:

for UVH rising, $V_{UVH(TH)}$ = 2.56V, turn-on

for UVL falling, $V_{UVL(TH)}$ = 2.291V, turn-off

The UVH and UVL pins have a hysteresis of δV_{UV} (15mV typical). In either a rising or a falling input supply, the undervoltage comparator works in such a way that both the UVH and the UVL pins have to cross their thresholds for the comparator output to change state.

The UVH, UVL, and OV threshold ratio is designed to match the standard telecom operating range of 43V to 71V and UV hysteresis of 4.5V when UVH and UVL are tied together as in Figure 4, where the built-in UV hysteresis referred to the UVL pin is:

$$\Delta V_{UV(HYST)} = V_{UVH(TH)} - V_{UVL(TH)} = 0.269V$$

Using R1 = 11.8k, R2 = 16.9k and R3 = 453k as in Figure 4 gives a typical operating range of 43.0V to 70.7V, with an undervoltage shutdown threshold of 38.5V and an overvoltage shutdown threshold of 72.3V.

The UV hysteresis can be adjusted by separating the UVH and UVL pins with a resistor R_H (Figure 15). To increase the UV hysteresis, the UVL tap should be placed above the UVH tap as in Figure 15a. To reduce the UV hysteresis,

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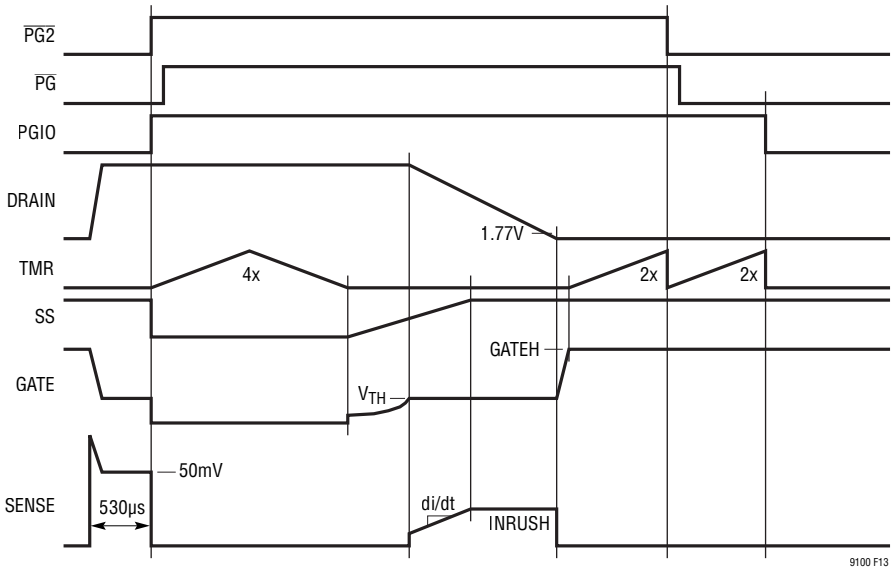

Figure 13. Overcurrent Fault and Auto-Retry

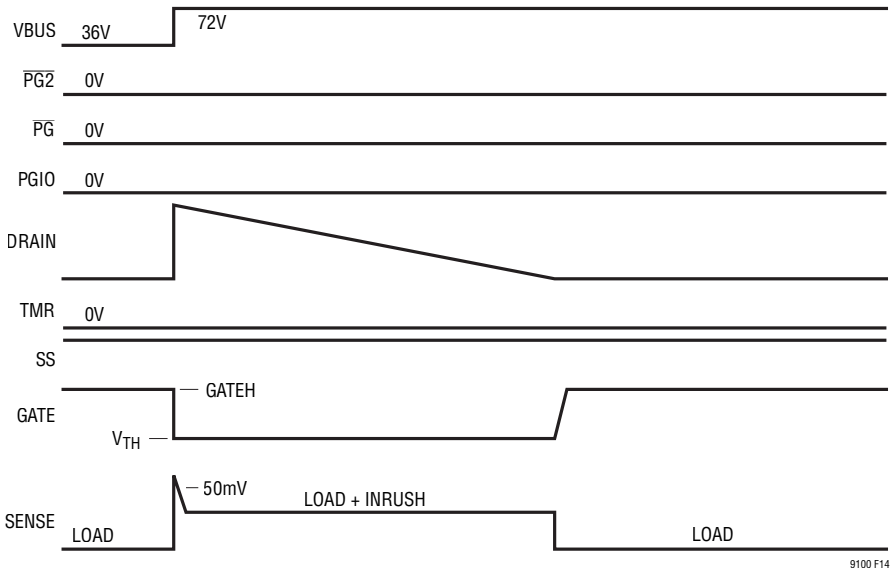

Figure 14. 36V to 72V Step Response

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place the UVL tap under the UVH tap as in Figure 15b. UV hysteresis referred to the UVL pin is given by:

for $V_{UVL} \geq V_{UVH}$

$$V_{UVL(HYST)} = V_{UV(HYST)} + 2.56V \bullet \frac{R_H}{R1+R2}$$

or for $V_{UVL} < V_{UVH}$

$$V_{UVL(HYST)} = V_{UV(HYST)} - 2.56V \bullet \frac{R_H}{R1+R2+R_H}$$

For $V_{UVL} < V_{UVH}$, the minimum UV hysteresis allowed is the minimum hysteresis at UVH and UVL: δV_{UV} = 15mV when $R_{H(MAX)} = 0.11 \bullet (R1 + R2)$.

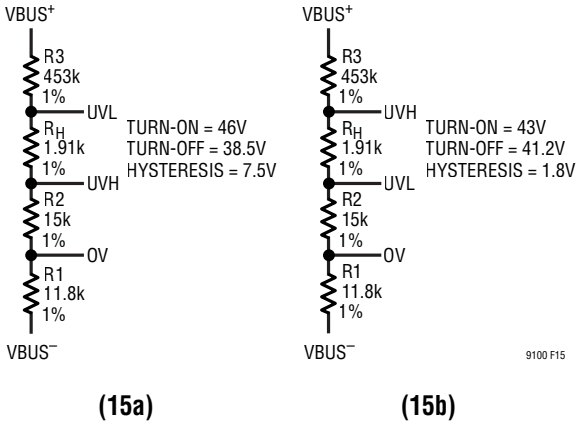

Figure 15. Adjustment of Undervoltage Thresholds for Larger (15a) or Smaller (15b) Hysteresis

The design of the LTM9100 protects the UV comparator from chattering even when R_H is larger than $R_{H(MAX)}$.

An undervoltage fault occurs when the UVL pin falls below 2.291V and the UVH pin falls below 2.56V – δV_{UV}. This activates the FET turn-off and sets the undervoltage present register bit A1 and the undervoltage fault register bit B1. The power good signals at $\overline{PG}$ and PGIO are also reset.

The undervoltage present register bit A1 is cleared when the UVH pin rises above 2.56V and the UVL pin rises above 2.291V + δV_{UV}. After a delay of t_D, the FET will turn on again unless the undervoltage auto-retry has been disabled by clearing register bit D1.

When power is applied to the device, if UVL is below the 2.291V threshold and UVH is below 2.56V – δV_{UV} after V_{CC2} crosses its undervoltage lock out threshold (4.25V), an undervoltage fault will be logged in the fault register.

Because of the compromises of selecting from a table of discrete resistor values (1% resistors in 2% increments, 0.1% resistors in 1% increments), best possible OV and UV accuracy is achieved using separate dividers for each pin. This increases the total number of resistors from three or four to as many as six, but maximizes accuracy, greatly simplifies calculations and facilitates running changes to accommodate multiple standards or customization without any board changes.

FET Short Fault

A FET short fault will be reported if the data converter measures a current sense voltage greater than or equal to 2mV while the FET is turned off. This condition sets the FET_STAT register bit A5 and the FET_FAULT register bit B5.

External Fault Monitor

The PGIO pin, when configured as a general purpose input, allows the monitoring of external fault conditions such as broken fuses. In this case, if the voltage at PGIO is above 1.25V, both register bit A6 and register bit B6 are set, though there is no alert bit associated with this fault. An external fault condition on PGIO does not directly affect the GATE control functions.

Fault Alerts

When any of the fault bits in the FAULT (B) register are set, an optional bus alert can be generated by setting the appropriate bit in the ALERT (C) register. This allows only selected faults to generate alerts. At power-up the default state is not to alert on faults. If an alert is enabled, the corresponding fault will cause the $\overline{ALERT2}$ and $\overline{ALERT}$ pins to pull low. After the bus master controller broadcasts the alert response address, the LTM9100 will respond with its address on the SDA line and release $\overline{ALERT}$ as shown in Figure 30. If there is a collision between two LTM9100's responding with their addresses simultaneously, then

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the device with the lower address wins arbitration and responds first. The $\overline{\text{ALERT}}$ line will also be released if the device is addressed by the bus master.

Once the $\overline{\text{ALERT}}$ signal has been released for one fault, it will not be pulled low again until the FAULT register indicates a different fault has occurred, or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated FAULT register bit has been cleared.

Resetting Faults

Faults are reset with any of the following conditions. First, writing zeros to the FAULT register will clear the associated fault bits. Second, the entire FAULT register is cleared when either the EN2 pin or register bit D3 goes from high to low, or if V_{CC2} falls below its 4.25V undervoltage lockout. Pulling the UVL pin below its 1.21V reset threshold also clears the entire FAULT register. When the UVL pin is brought back above 1.21V but below 2.291V, the undervoltage fault register bit B1 is set if the UVH pin is below 2.56V. This can be avoided by holding the UVH pin above 2.56V while toggling the UVL pin to reset faults.

Fault bits with associated conditions that are still present (as indicated in the STATUS (A) Register) cannot be cleared. The FAULT register will not be cleared when auto-retrying. When auto-retry is disabled, the existence of register bits B0 (overvoltage), B1 (undervoltage) or B2 (overcurrent) keeps the FET off. After the fault bit is cleared and a delay of t_D expires, the FET will turn on again. Note that if the overvoltage fault register bit B0 is cleared by writing a zero through I^2C, the FET is allowed to turn on without a delay. If auto-retry is enabled, then a high value in register bits A0, A1 or A2 will hold the FET off and the FAULT register is ignored. Subsequently, when register bits A0, A1 and A2 are cleared, the FET is allowed to turn on again.

Data Converter

The LTM9100 incorporates a 10-bit ΔΣ analog-to-digital converter (ADC) that continuously monitors three different voltages at (in the sequence of) SENSE, ADIN2 and ADIN. The ΔΣ architecture inherently averages signal noise during the measurement period. The voltage between the $SENSE^+$ and $SENSE^-$ pins is monitored with a 64mV full-scale and 62.5μV resolution, and the data is stored in registers E and F. The ADIN and ADIN2 pins are monitored with a 2.56V full-scale and 2.5mV resolution. The data for the ADIN2 pin is stored in registers G and H. The data for the ADIN pin is stored in registers I and J.

The results in registers E, F, G, H, I and J are updated at a frequency of 7.3Hz. Setting register bit D5 invokes a test mode that halts updating these registers so that they can be written to and read from for software testing. By invoking the test mode right before reading the ADC data registers, the 10-bit data separated in two registers are synchronized.

The ADIN and ADIN2 pins can be used to monitor input and output voltages or temperature of the controller as shown in Figures 33 to 35, 39, 40, 43, and 45.

Configuring the PGIO Pin

Table 4 describes the possible states of the PGIO pin using register bits D6 and D7. At power-up the default state is for the PGIO pin to pull low when the second power good signal is ready. Other uses for the PGIO pin are to go high impedance when the second power good is ready, a general purpose output and a general purpose input. When the PGIO pin is configured as a general purpose output, the status of register bit C6 is sent out to the pin. When it is configured as a general purpose input, if the input voltage at PGIO is higher than 1.25V, both register bits A6 and B6 are set. If the input voltage at PGIO subsequently drops below 1.25V, register bit A6 is cleared. Register bit B6 can be cleared by resetting the FAULT register as described previously.

Design Procedure

1. Using the load current (I_{LOAD}) requirement of the application, calculate the sense resistor (R_S) value using the minimum SENSE threshold voltage of 45mV.

$$R_S = \frac{45mV}{I_{LOAD}}$$

$$I_{MAX} = \frac{55mV}{R_S}$$

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2. For a capacitive load (C_L) set the inrush (I_{INRUSH}) current by calculating the ramp capacitor (C_R) value.

$$C_R = C_L \bullet \frac{I_{RAMP}}{I_{INRUSH}} = C_L \bullet \frac{20\mu A}{I_{INRUSH}}$$

The inrush current and ramp capacitor may need to be iterated based upon the selected switch safe operating area (SOA).

For resistive or inductive loads the turn-on voltage rate of change is calculated by:

$$\frac{dV}{dt} = \frac{I_{RAMP}}{C_R} = \frac{20\mu A}{C_R}$$

3. Select an N-channel switch (Q1); MOSFET, SiC MOSFET, IGBT, etc. Switch selection is based upon maximum operating voltage (with margin), ON state power dissipation ($I_{MAX}^2 \bullet R_{DSON}$ or $I_{MAX} \bullet V_{CESAT}$), and SOA. The maximum ON state power dissipation (P_{ON}) is calculated using the maximum load current and maximum expected switch R_{DSON}. The maximum switch resistance at 125°C is generally 2× the data sheet electrical table maximum ON resistance at 25°C junction temperature.

$$P_{ON} = I_{MAX}^2 \bullet R_{DSON(125°C)}$$

Multiple cases must be considered for the switch SOA including; normal inrush turn-on, turn-on into a short circuit, input voltage steps, and short-circuit while conducting. To evaluate the switch SOA between multiple manufacturers and operating cases the calculated data, and constant power (diagonally decreasing) portion of the data sheet SOA curves, can be normalized by calculating P^2t or $P\sqrt{t}$ and comparing. Switches designed and characterized for linear or DC operation are most suitable. These are generally switches fabricated using a planar process, as opposed to a high density vertical process (e.g. trench).

a. Normal switch turn-on power dissipation (P_{TON}) consists of a voltage ramp from VBUS to ≈ 0V with constant charging current of I_{INRUSH}. Assuming no load current and ignoring slow start:

$$P_{TON} = \frac{VBUS \bullet I_{INRUSH}}{2}$$

$$t_{INRUSH} = \frac{C_R \bullet VBUS}{I_{RAMP(min)}} = \frac{C_L \bullet VBUS}{I_{INRUSH}}$$

$$P\sqrt{t} = P_{TON}\sqrt{t_{INRUSH}}$$

b. Load short-circuit turn-on power dissipation (P_{SCTON}) consists of a current ramp to I_{MAX}, this is the MOSFET transconductance period (t_{fs}), followed by the circuit breaker period (t_{CB}) at I_{MAX}, each at constant bus voltage. Ignoring slow start:

$$P_{fs} = \frac{VBUS \bullet I_{MAX}}{2}$$

$$P_{CB} = VBUS \bullet I_{MAX}$$

$$t_{fs} = \frac{(C_G + C_{iss(max)}) \bullet 2 \bullet I_{MAX}}{I_{GATE(min)} \bullet g_{fs(min)}}$$

where $I_{GATE(min)}$ = 7.5µA, C_{iss} is the MOSFET gate input capacitance, and g_{fs} is the MOSFET forward transconductance.

t_{CB} = 620µs (Maximum)

Calculate the total power dissipation over the event:

$$P_{SCTON} = \frac{P_{fs} \bullet t_{fs} + P_{CB} \bullet t_{CB}}{t_{fs} + t_{CB}}$$

$$P\sqrt{t} = P_{SCTON}\sqrt{t_{fs} + t_{CB}}$$

c. Power dissipation for an input voltage step (P_{STEP}) consists of a voltage ramp from V_{STEP} to ≈ 0V with constant current of $I_{MAX} = I_{INRUSH} + I_{LOAD}$. Assuming load current is constant with operating voltage:

$$P_{STEP} = \frac{V_{STEP} \bullet I_{MAX}}{2}$$

$$t_{STEP} = \frac{C_R \bullet V_{STEP}}{I_{RAMP(min)}} = \frac{C_L \bullet V_{STEP}}{I_{INRUSH}}$$

$$P\sqrt{t} = P_{STEP}\sqrt{t_{STEP}}$$

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d. Load short-circuit while conducting power dissipation (P_{SCON}) consists of a constant bus voltage at maximum current for the circuit breaker period.

$$P_{SCON} = VBUS \bullet I_{MAX}$$

$$t_{CB} = 620\mu s$$

$$P\sqrt{t} = P_{SCON}\sqrt{t_{CB}}$$

On inspection case d will always result in a lower value than case b and will not need to be calculated.

4. Select the GATE compensation capacitance (C_G). The total capacitance on the GATE pin should be ≈ 47nF to compensate the active current limit circuit. The total capacitance is equal to:

$$C_{G(TOTAL)} = C_G + C_{iss} \approx 47nF$$

5. Size divider resistors for undervoltage and overvoltage trip points, assuming UVL and UVH pins tied together, and one divider for both functions (Figure 4). These functions may be disabled by tying UVL and UVH to V_{CC2}, and OV to V_{EE}.

a. Choose a nominal current to run in the divider ($I_{DIV(NOM)}$). Typically this is 100µA.

b. The current in the divider during an overvoltage condition is:

$$I_{DIV(OV)} = I_{DIV(NOM)} \bullet \frac{VBUS_{OV}}{VBUS_{NOM}}$$

where $VBUS_{NOM}$ is the nominal bus voltage and $VBUS_{OV}$ is the bus voltage in the overvoltage condition.

c. Calculate R1:

$$R_1 = \frac{V_{OV(TH)}}{I_{DIV(OV)}} = \frac{1.77V}{I_{DIV(OV)}}$$

d. Choose the undervoltage bus voltage ($VBUS_{UV}$). Undervoltage may be set using the rising threshold (UVH) of 2.56V, the bus voltage where the system starts to operate, or falling threshold (UVL) of 2.291V, the bus voltage where the system ceases to operate, depending on the system requirements.

e. The current in the divider at threshold of undervoltage event is:

$$I_{DIV(UV)} = I_{DIV(NOM)} \bullet \frac{VBUS_{UV}}{VBUS_{NOM}}$$

f. Calculate R2:

$$R2 = \frac{V_{UV(TH)}}{I_{DIV(UV)}} - R1$$

g. Calculate R3:

$$R3 = \frac{VBUS_{NOM}}{I_{DIV(NOM)}} - R1 - R2$$

6. Size resistor to the DRAIN pin, the suggested bias current is 50µA, limit the value to < 2mA.

$$R_D = \frac{VBUS_{NOM}}{50\mu A}$$

Design Example #1

For this design example, consider the 200W application with C_L = 330µF as shown in Figure 4. The operating voltage range is from 43V to 71V with a UV turn-off threshold of 38.5V. For the purposes of calculation the minimum operating voltage is 36V and maximum is 72V. The design must tolerate short circuits and an input voltage step of 36V.

1. The sense resistor is calculated using the minimum sense threshold, minimum operating voltage, and application power:

$$R_S = \frac{45mV \bullet 36V}{200W} = 0.008\Omega$$

$$I_{MAX} = \frac{55mV}{0.008} = 6.875A$$

2. Set the inrush current to 0.66A.

$$C_R = C_L \bullet \frac{20\mu A}{0.66A} = 10nF$$

R_R is chosen to be 1k as discussed previously.

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3. Select a MOSFET and compare the calculated power dissipation under all conditions. The IRF1310 is selected, worst case conduction loss is:

   $P_{ON} = I_{MAX}^2 \bullet R_{DSON(125°C)} = 6.875^2 \bullet 72m\Omega = 3.4W$

   From the data sheet SOA curve the $P\sqrt{t}$ for 10ms operation is $\approx 25W\sqrt{s}$ (V_{DS} = 50V, I_D = 5A).

   Case 3a:

   $$P\sqrt{t} = \frac{72 \bullet 0.66}{2}\sqrt{\frac{330\mu \bullet 72}{0.66}} = 4.5W\sqrt{s}$$

   Case 3b:

   $$P_{fs} = \frac{72 \bullet 6.875}{2} = 248W, P_{CB} = 72 \bullet 6.875 = 495W$$

   $$t_{fs} = \frac{(47n + 1.9n) \bullet 2 \bullet 6.875}{7.5\mu A \bullet 14} = 6.4ms$$

   $$P_{SCTON} = \frac{248 \bullet 6.4m + 495 \bullet 620\mu}{6.4m + 620\mu} = 270W$$

   $$P\sqrt{t} = 270\sqrt{6.4m + 620\mu} = 22.6W\sqrt{s}$$

   Case 3c:

   $$P\sqrt{t} = \frac{36 \bullet 6.875}{2}\sqrt{\frac{330\mu \bullet 36}{0.66}} = 16.6W\sqrt{s}$$

   All cases are satisfied with $P\sqrt{t}$ values < $25W\sqrt{s}$.

4. The FET selected in step 3 has an input capacitance of 1.9nF, so the C_G value of 47nF is appropriate.

5. Set the nominal UV/OV divider string to 100µA, resistors are rounded to the nearest 1% value.

   $$I_{DIV(OV)} = 100\mu A \bullet \frac{72}{48} = 150\mu A$$

   $$I_{DIV(UV)} = 100\mu A \bullet \frac{43}{48} = 89.6\mu A$$

   $$R1 = \frac{1.77}{150\mu A} = 11.8k\Omega$$

   $$R2 = \frac{2.56}{89.6\mu A} - 11.8k\Omega = 16.9k\Omega$$

   $$R3 = \frac{48}{100\mu A} - 11.8k\Omega - 16.9k\Omega = 453k\Omega$$

6. The DRAIN pin resistor is set to 1MΩ.

Design Example #2

For this design example, consider the 380V application with C_L = 330µF as shown on the back page. The operating voltage range is from 260V to 420V with a UV turn-off threshold of 235V, and OV threshold of 435V. The design must tolerate short circuits, and be designed to maximize the available load current with an off-the-shelf MOSFET.

With a 435V maximum operating voltage a MOSFET with 600V drain to source voltage is desired. In order to maximize load current, minimum R_{DSON} and excellent SOA are needed. A device survey shows than an IXYS, IXTH30N60L2, is a good candidate. A reasonable, heat-sinkable, board level conduction loss (P_{ON}) is 5W. The maximum operating current can now be calculated:

$$I_{MAX} = \sqrt{\frac{P_{ON}}{R_{DSON(125°C)}}} = \sqrt{\frac{5}{0.48}} = 3.25A$$

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1. Calculate the sense resistor:

$$R_S = \frac{55mV}{3.25A} = 0.017\Omega$$

2. Set the inrush current, by choosing an operating current below the DC SOA operating curve at 400V.

$$I_{INRUSH} = 0.3A, C_R = 330\mu \bullet \frac{20\mu A}{0.3A} = 22nF$$

3. The $P\sqrt{t}$ of the device is ≈ $80W\sqrt{s}$ at a case temperature of 75°C.

   Case 3a:

$$P\sqrt{t} = \frac{430 \bullet 0.3}{2}\sqrt{\frac{330\mu \bullet 430}{0.3}} = 44W\sqrt{s}$$

   Case 3b:

$$P_{fs} = \frac{430 \bullet 3.25}{2} = 700W, P_{CB} = 430 \bullet 3.25 = 1.4kW$$

$$t_{fs} = \frac{(39n + 10.7n) \bullet 2 \bullet 3.25}{7.5\mu A \bullet 10} = 4.3ms$$

$$P_{SCTON} = \frac{700 \bullet 4.3m + 1400 \bullet 620\mu}{4.3m + 620\mu} = 788W$$

$$P\sqrt{t} = 788\sqrt{4.3m + 620\mu} = 55W\sqrt{s}$$

   Case 3c is not calculated since an input step was not specified.

4. The FET selected has an input capacitance of 10.7nF, so the C_G value of 39nF is appropriate.

5. In this example the bus voltage must be level shifted and referenced to V_{EE} to utilize the UV, OV, and analog inputs. This is accomplished by the differential amplifier stage using the LTC®2054. Since the output of the amplifier connects to the UV pins, the amplifier divide ratio is set for an output voltage of 2.291V at the UV turn-off threshold of 235V; 235/2.291=102.3. Choose the input resistors to minimize current and power dissipation; 3.3MΩ is chosen, the divider resistors are then 3.3MΩ/102.3 = 32.4kΩ. As noted on the schematic the ADIN voltage should be 2.56V at 435V, and the OV voltage should be 1.77V at 435V. Set the maximum divider string current to 200µA.

$$R1 = \frac{1.77}{200\mu A} = 8.87k\Omega$$

$$R2 = \frac{2.56}{200\mu A} - 8.87k\Omega = 3.92k\Omega$$

$$R3 = \frac{\frac{VBUS_{OV}}{102.3}}{200\mu A} - 8.87k\Omega - 3.92k\Omega = 8.45k\Omega$$

6. The DRAIN pin resistor is set to 3.3MΩ.

External Switch

While the primary application of the LTM9100 is the control of an external N-Channel MOSFET switch, insulated gate bipolar transistors (IGBTs) may be used. This is of particular interest in voltage applications greater than 250V where traditional FETs with sufficient SOA and low R_{DSON} are not available.

IGBTs are readily available with voltage ratings of 600V, 1200V, and higher. Not all IGBTs are suitable, only those specified for DC or near DC operation as indicated in the data sheet SOA operating curves. Two additional areas of concern are the collector to emitter saturation voltage and gate to emitter threshold voltage.

The LTM9100 monitors the collector voltage of the IGBT, via the DRAIN pin and series resistor, to insure the IGBT is turned on before the power good signals are transitioned. The DRAIN pin threshold is 1.77V. The saturation voltage, $V_{CE(SAT)}$, of the IGBT may be higher than this necessitating a voltage divider on the DRAIN monitor input pin as shown in Figure 16.

Resistor R1 is sized based on the bus voltage and maximum DRAIN current of 2mA. Resistor R2 is then chosen to provide a voltage less than 1.77V on the DRAIN pin with

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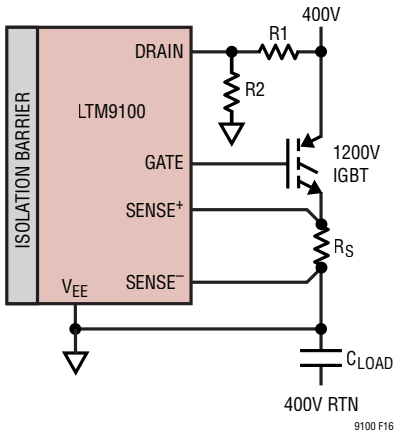

Figure 16. LTM9100 DRAIN Monitor Resistive Divider for IGBT Collector Sense

margin for the worst-case load current and V_{CE} voltage of the IGBT at the minimum GATE voltage.

The IGBT gate to emitter threshold voltage must also be considered. The IGBT should be selected with a maximum gate to emitter threshold voltage, $V_{GE(th)}$, corresponding to the minimum LTM9100 GATE power good condition or V_S minimum UVLO voltage of 8.5V. The threshold voltage presented in the device data sheet electrical table is often at very low collector currents. Plots are typically provided for collector current vs gate-emitter voltage, and gate-emitter voltage vs gate charge. The IGBT characteristics must be carefully evaluated to ensure compatibility with the LTM9100.

Boosting Gate Voltage

Higher gate voltage may be desired for two primary reasons. First, to reduce the sensitivity of dV/dt coupling from the drain or collector to gate via the Miller capacitance, providing additional noise margin. Secondly to optimize the R_{DSON} or V_{CE} which in turn reduces power dissipation.

Figure 17 shows a simple method to increase the gate voltage. Q2 remains on until the LTM9100 GATE pin voltage, relative to V_S, reaches the V_{GS} threshold of Q2. When Q2 turns off, the gate of Q1 continues to charge through R1 to an external supply voltage (V_{BOOST}). The value of R1 should be selected to insure that the Q1 gate is near full voltage before $\overline{PG2}$ transitions, one timer delay after the LTM9100 GATE pin reaches ~9V. The value of R1 also impacts Q1's gate charging current. This additional current must be accounted for in the load current inrush calculation and sizing of C_R.

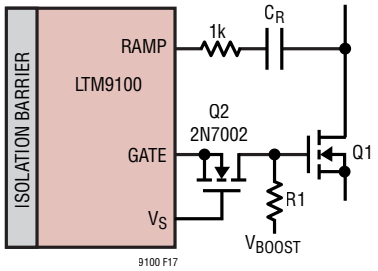

Figure 17. Simple Gate Voltage Booster

$$I_{RAMP} \approx 20\mu A + 2 \bullet \frac{V_{BOOST} - V_{Q1(threshold)}}{R1}$$

$$C_R = C_L \bullet \frac{I_{RAMP}}{I_{INRUSH}}$$

Negative Gate Bias

While the GATE signal is strongly pulled to V_{EE} in the off state, additional voltage margin may still be desired to further reduce the risk of capacitance coupled switch turn on. In this situation, a negative gate off bias may also be incorporated as shown in Figure 18. Q4 enables the negative bias when EN transitions low, Q3 blocks current from the V_{EE} based GATE pin, and Q2 connects an external negative voltage ($-V_{BIAS}$) to the switch.

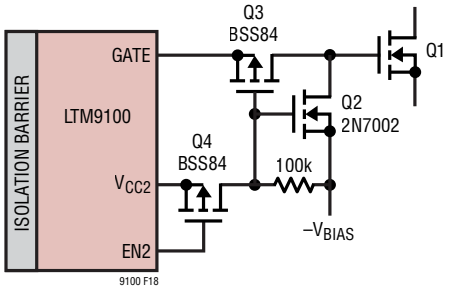

Figure 18. Negative Gate Bias Controlled by EN

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The application circuit of Figure 36, shows a method to generate both the boosted voltage supply and negative bias supply from V_S.

Paralleling Switches

It is not recommended to connect switches in parallel to increase the SOA during turn-on. The LTM9100 does not include any provisions to insure current sharing between multiple switches. Differences in switch turn-on characteristics will inevitably result in one switch conducting most of the turn-on current until fully enhanced.

This also holds for FET modules which are composed of multiple die to achieve higher current ratings. The modules do not employ any dynamic current sharing methods. Switch threshold matching is insufficient to guarantee current sharing.

DC Bus with AC Ripple (Rectified AC)

The LTM9100 is primarily intended to control the charging of a capacitor by linearly ramping the drain voltage of an external FET which produces a constant charging current. If the DC bus voltage includes an AC component, then the capacitor is only charged when the rectified input voltage exceeds the capacitor voltage, producing high peak currents in short intervals.

Typically a series inductor is added to reduce the AC ripple and smooth the capacitor charging current. The input LC filter must be carefully designed based on the source impedance, load requirements, etc., and it's design is beyond the scope of this discussion.

If an inductive input filter is not desired, and the load requirements are such that the peak capacitor charging currents after initial turn-on are tolerable, then the LTM9100 may be configured to charge the load capacitance, see Figure 19. The RAMP pin is not used due to coupling of the AC voltage onto the GATE, instead transistor Q2 is added with the ramp capacitor placed in series to control GATE as the load capacitor is charged. Diode D5 resets the ramp capacitor at turn-off and transistor Q3 isolates GATE after the turn-on sequence completes to prevent further GATE modulation during normal operation.

The sense resistor is sized for the peak capacitor charging current during normal operation to avoid engaging the internal current limit and circuit breaker functions, otherwise excessive power dissipation and FET destruction may result. This is particularly true during the inrush charging period where the FET has up to the full input bus voltage across it.

The internal circuit breaker time of 530µs results in excessive power dissipation during turn-on with a short-circuit

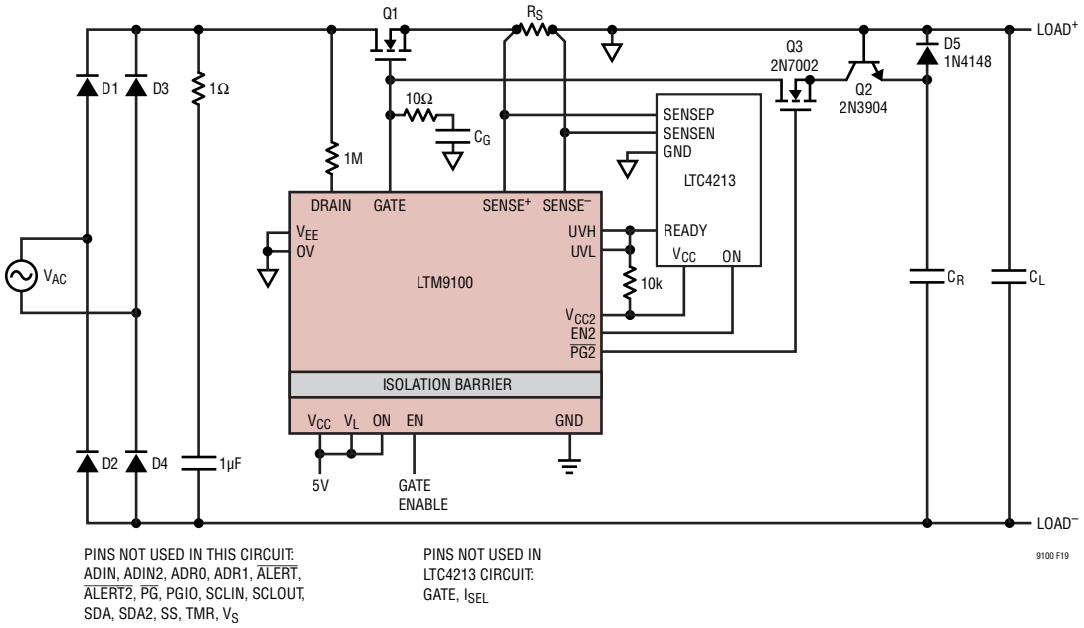

Figure 19. Rectified AC High Side Charging Circuit

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Table 1. Component Values for 13.4% Ripple Single Phase and 3.4% Ripple Three Phase

V_{AC}	Q1			C_G	I_{LOAD}	C_L	C_R	R_S	
	PART #	VOLTAGE	$R_{DSON(25°C)}$					1ϕ	3ϕ
48	FQA90N15	150V	0.018	39nF	8	5600µF	56nF	0.0008	0.0016
120	FQA55N25	250V	0.04	47nF	6	1500µF	39nF	0.001	0.002
240	FDL100N50F	500V	0.055	33nF	5	680µF	6.8nF	0.001	0.002

condition. If short-circuit protection during turn-on is required then an external electronic circuit breaker is required, LTC4213 of Figure 19.

The load charging current (I_{INRUSH}) is chosen based on the FET SOA. The ramp capacitor (C_R), and ramp time (t_{INRUSH}) are calculated as before using the GATE current instead of the RAMP current:

$$C_R = C_L \bullet \frac{I_{GATE}}{I_{INRUSH}} = C_L \bullet \frac{11.5\mu A}{I_{INRUSH}}$$

$$t_{INRUSH} = C_R \bullet \frac{V_{PEAK}}{I_{GATE}} = C_L \bullet \frac{V_{PEAK}}{I_{INRUSH}}$$

The charging time may need to be extended to reduce transient thermal excursions during turn-on. Circuit simulation software, such as LTspice®, can be useful in predicting the maximum junction temperature, provided an accurate FET transient thermal impedance model is available. Table 1 shows the component values for both single and three phase voltage inputs at three different input voltage levels. The load charging voltage, current, and junction temperature of Q1 are shown in Figure 20 for the 120V_{AC} case of Table 1.

The sense resistors specified for the examples in Table 1 are based on a source impedance of 0Ω and therefore represent the minimum value, in practice the peak capacitor charging currents will be lower and the sense resistor should be sized appropriately. In addition, the load capacitor must be selected to handle the high RMS charging current, and will typically be composed of multiple parallel capacitors for this reason.

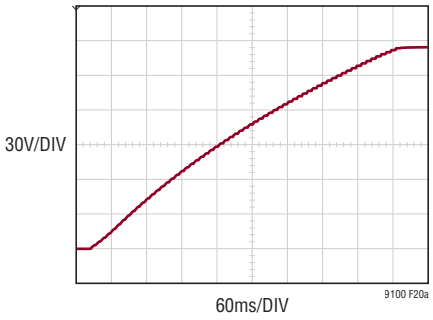

Figure 20(a). Load Capacitor Voltage

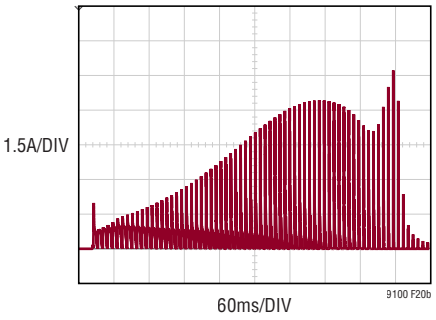

Figure 20(b). Load Capacitor Current

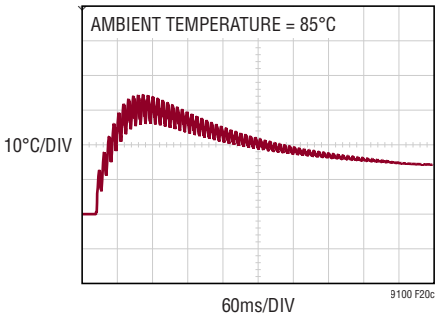

Figure 20(c). Q1 Junction Temperature

Figure 20. Load Capacitor Charging Voltage, Current, and Junction Temperature

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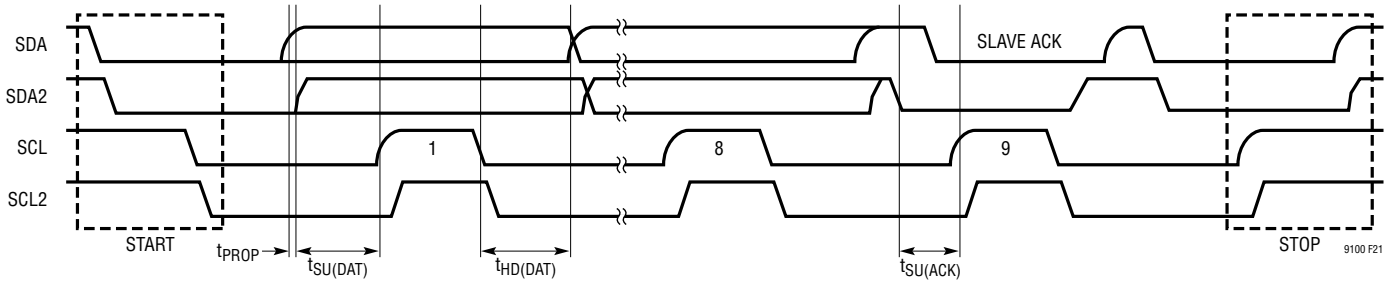

Figure 21. I²C Timing Diagram

Inter-IC Communication Bus (I²C)

The LTM9100 provides an I²C compatible isolated interface; clock (SCL→SCL2) is unidirectional, supporting master mode only, and data (SDA↔SDA2) is bidirectional. The I²C interface provides access to the ADC data registers and four other registers for the monitoring and control of the FET. In addition, the isolated side I²C pins are accessible, allowing additional serial device expansion.

The maximum I²C data rate is 400kHz, fast-mode capable, limited by the slave acknowledge setup time ($t_{SU(ACK)}$), consisting of the system propagation delay, glitch filter, and fixed isolated data delay of approximately 500ns. Timing is detailed in Figure 21. The total setup time reduces the I²C data hold time ($t_{HD(DAT)}$) to a maximum of 175ns, guaranteeing sufficient data setup time ($t_{SU(DAT)}$).

The isolated side bidirectional serial data pin, SDA2, simplified schematic is shown in Figure 22. An internal 1.8mA current source provides a pull-up for SDA2. Do not connect any other pull-up device to SDA2. This current source is sufficient to satisfy the system requirements for bus capacitances greater than 200pF in FAST mode and greater than 400pF in STANDARD mode.

Additional proprietary circuitry monitors the slew rate on the SDA and SDA2 signals to manage directional control across the isolation barrier. Slew rates on both pins must be greater than 1V/µs for proper operation.

The logic side bidirectional serial data pin, SDA, requires a pull-up resistor or current source connected to V_L. Follow the requirements in Figures 23 and 24 for the appropriate pull-up resistor on SDA that satisfies the desired rise time specifications and V_{OL} maximum limits for FAST and

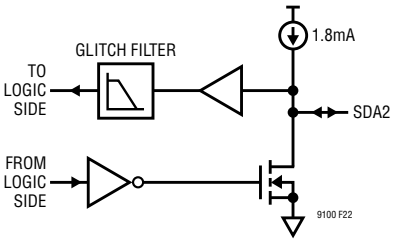

Figure 22. Isolated SDA2 Pin Schematic

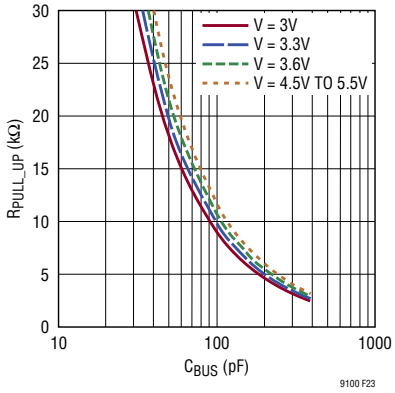

Figure 23. Maximum Standard Speed Pull-Up Resistance on SDA

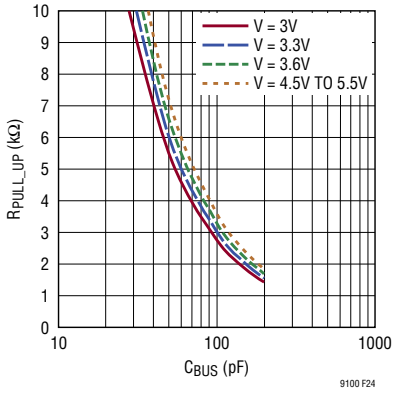

Figure 24. Maximum Fast Speed Pull-Up Resistance on SDA

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STANDARD modes. The resistance curves represent the maximum resistance boundary; any value may be used to the left of the appropriate curve.

The isolated side clock pin, SCL2 has a weak push-pull output driver; do not connect an external pull-up device. SCL2 is compatible with I^2C devices without clock stretching. On lightly loaded connections, a 100pF capacitor from SCL2 to V_{EE} or RC low pass filter (R = 500Ω, C = 100pF) can be used to increase the rise and fall times and minimize noise.

The LTM9100 is a read-write slave device and supports SMBus bus read byte, write byte, read word and write word commands. The second word in a read word command will be identical to the first word. The second word in a write word command is ignored. The data formats for these commands are shown in Figures 25 to 28.

START and STOP Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transiting SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Stuck-Bus Reset

The LTM9100 I^2C interface features a stuck-bus reset timer. The low conditions of the SCL2 and SDA2 pins are ORed to start the timer. The timer is reset when both SCL2 and SDA2 are pulled high. If the SCL2 pin or the SDA2 pin is held low for over 66ms, the stuck-bus timer will expire and the internal I^2C state machine will be reset to allow

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	P
	001a3:a0	0	0	XXXXb3:b0	0	b7:b0	0	

9100 F25

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 25. LTM9100 Serial Bus SDA Write Byte Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	DATA	A	P
	001a3:a0	0	0	XXXXb3:b0	0	b7:b0	0	XXXXXXXX	0	

9100 F26

Figure 26. LTM9100 Serial Bus SDA Write Word Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	$\overline{A}$	P
	001a3:a0	0	0	XXXXb3:b0	0		001a3:a0	1	0	b7:b0	1	

9100 F27

Figure 27. LTM9100 Serial Bus SDA Read Byte Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	001a3:a0	0	0	XXXXb3:b0	0		001a3:a0	1	0	b7:b0	0	b7:b0	1	

9100 F28

Figure 28. LTM9100 Serial Bus SDA Read Word Protocol

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normal communication after the stuck-low condition is cleared. When the SCL2 pin and the SDA2 pin are held low alternately, if the ORed low period of SCL2 and SDA2 exceeds 66ms before the timer reset condition (both SCL2 and SDA2 are high) occurs, the stuck-bus timer will expire and the I²C state machine is reset.

I²C Device Addressing

Any of eight distinct I²C bus addresses are selectable using the three-state pins ADR0 and ADR1, as shown in Table 2. Note that the configuration of ADR0 = L and ADR1 = H is used to enable the single-wire broadcasting mode. For the eight I²C bus addresses, address bits b7, b6 and b5 are configured to (001) and the least significant bit b0 is the R/W bit. In addition, the LTM9100 will respond to two special addresses. Address (0011 111) is a mass write used to write to all LTM9100s, regardless of their individual address settings. Address (0001 100) is the SMBus alert response address. If the LTM9100 is pulling low on the $\overline{\text{ALERT}}$ pin, it will acknowledge this address using the SMBus alert response protocol. Note, if multiple LTM9100's are configured to share a single ALERT bus then the addition of an open drain buffer is necessary, see Figure 29.

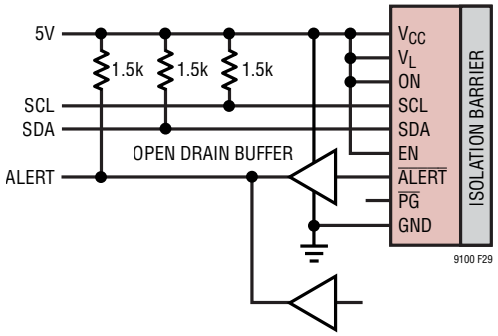

Figure 29. Open Drain Buffer for Shared ALERT Bus

Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it must pull down the SDA2 line so that it remains low during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA2 high, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must pull down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master will leave the SDA line high (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the R/W bit set to zero. The addressed LTM9100 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTM9100 acknowledges this and then latches the lower four bits of the command byte into its internal register address pointer. The master then delivers the data byte and the LTM9100 acknowledges once more and latches the data into its internal register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a write word command, the second data byte will be acknowledged by the LTM9100 but ignored.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the R/W bit set to zero. The addressed LTM9100 acknowledges this and then the master sends a command byte that indicates which internal register the master wishes to read. The LTM9100 acknowledges this and then latches the lower four bits of the command byte into its internal register address pointer. The master then sends a repeated START

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condition followed by the same seven bit address with the R/W bit now set to one. The LTM9100 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a read word command, the LTM9100 will repeat the requested register as the second data byte. Note that the register address pointer is not cleared at the end of the transaction. Thus the receive byte protocol can be used to repeatedly read a specific register.

Alert Response Protocol

The LTM9100 implements the SMBus alert response protocol as shown in Figure 30. If enabled to do so through the ALERT (C) register, the LTM9100 will respond to faults by pulling the $\overline{\text{ALERT}}$ pins low. Multiple LTM9100s can share a common $\overline{\text{ALERT2}}$ line on the isolated side, or a common $\overline{\text{ALERT}}$ line on the logic side with the addition of open drain buffers. The protocol allows a master to determine which LTM9100 is pulling the line low. The master begins by sending a START bit followed by the special alert response address (0001 100) with the R/W bit set to one. Any LTM9100 that is pulling its $\overline{\text{ALERT}}$ pins low will acknowledge and begin sending back its individual slave address.

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{\text{A}}$	P
	0001100	1	0	001a3:a00	1	

9100 F30

Figure 30. LTM9100 Serial Bus SDA Alert Response Protocol

An arbitration scheme ensures that the LTM9100 with the lowest address will have priority; all others will abort their response. The successful responder will then release its $\overline{\text{ALERT}}$ pins while any others will continue to hold their $\overline{\text{ALERT}}$ pins low. Polling may also be used to search for any LTM9100 that have detected faults. Any LTM9100 pulling its $\overline{\text{ALERT}}$ pins low will also release them if it is individually addressed during a read or write transaction.

The $\overline{\text{ALERT}}$ signals will not be pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated FAULT register bit has been cleared.

Single-Wire Broadcast Mode

The LTM9100 provides a single-wire broadcast mode in which selected register data are sent out to the SDA pin without clocking the SCL line (Figure 31). The single-wire broadcast mode is enabled by setting the ADR1 pin high and the ADR0 pin low (the I^2C interface is disabled). At the end of each conversion of the three ADC channels, a stream of eighteen bits are broadcasted to SDA with a serial data rate of 15.3kHz ±20% in a format as illustrated in Figure 32. The data bits are encoded with an internal clock in a way similar to Manchester encoding that can be easily decoded by a microcontroller or FPGA. Each data bit consists of a noninverting phase and an inverting phase. During the conversion of each ADC channel, SDA will idle high. At the end of the conversion, the SDA pin pulls low. The START bit indicates the beginning of data broadcasting and is used along with the dummy bit (DMY) to measure the internal clock cycle (i.e., the serial data rate). Following the DMY bit are two channel code bits CH1 and CH0 labeling the ADC channel (see Table 3). Ten data bits of the ADC channel (ADC9 to ADC0) and three FAULT register bits (B2, B1 and B0) are then sent out. A parity bit (PRTY) ends each data stream. After that the SDA line enters the idle mode with SDA pulled high.

The following data reception procedure is recommended:

1. Wait for SDA falling edge.
2. The first falling edge could be a glitch, so check again after a delay of 10µs. If back to high, wait again. If still low, it is the START bit.
3. Use the following low-to-high and high-to-low transitions to measure 1/2 of the internal clock cycle.
4. Wait for the second low-to-high transition (middle of DMY bit).

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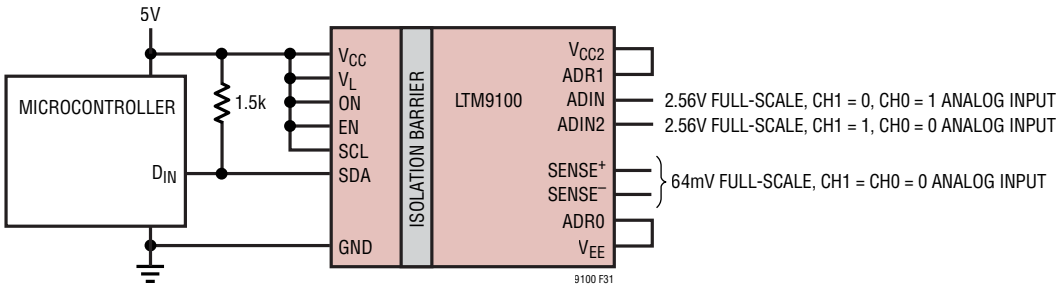
5. Wait 3/4 of a clock cycle.
6. Sample bit CH1, wait for transition.
7. Wait 3/4 of a clock cycle.
8. Sample bit CH0, wait for transition.
9. Wait 3/4 of a clock cycle.
10. Sample ADC9, wait for transition.
11. Continue until all bits are read.

The above procedure can be ported to a microcontroller or used to design a state machine in an FPGA. Code should have timeouts in case an edge is missed. Abort the read if it takes more than double the typical time (1.2ms) for all 18 bits to be clocked out.

A typical application circuit with the LTM9100 in the broadcast mode is illustrated in Figure 35, where input voltage, V_{DS} of the FET and V_{SENSE} are monitored.

Register Addresses and Contents

The device addresses and register contents are detailed in Table 2 and Table 4. The function of each register bit is described in Table 4.



PINS NOT USED IN THIS CIRCUIT:
$\overline{ALERT}$, $\overline{ALERT2}$, DRAIN, EN2, GATE, OV, $\overline{PG}$, $\overline{PG2}$, PGIO, RAMP, SCL2, SDA2, SS, TMR, UVL, UVH, V_S

Figure 31. Single-Wire Broadcast Mode

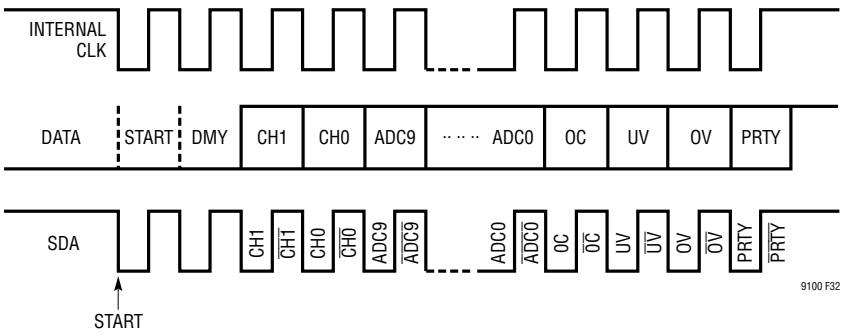


Figure 32. Single-Wire Broadcast Data Format

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Table 2. LTM9100 Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTM9100 ADDRESS PINS	
	h	b7	b6	b5	b4	b3	b2	b1	b0 (R/W)	ADR1	ADR0
Mass Write	3E	0	0	1	1	1	1	1	0	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X
0	20	0	0	1	0	0	0	0	X	L	L
1	22	0	0	1	0	0	0	1	X	L	NC
2	24	0	0	1	0	0	1	0	X	H	NC
3	26	0	0	1	0	0	1	1	X	L	H
4	28	0	0	1	0	1	0	0	X	NC	L
5	2A	0	0	1	0	1	0	1	X	NC	NC
6	2C	0	0	1	0	1	1	0	X	H	H
7	2E	0	0	1	0	1	1	1	X	NC	H
8	Single-Wire Broadcast Mode								X	H	L

H = Tie to V_{CC2}; L = Tie to V_{EE}; NC = No connect, open; X = Don't care

Table 3. ADC Channel Labeling for Single-Wire Broadcast Mode

CH1	CH2	ADC CHANNEL
0	0	SENSE Voltage
0	1	ADIN2 Voltage
1	0	ADIN Voltage

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Table 4. Register Map

REG*	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT
0x00 (Read Only)	**STATUS (A)** System Status Information	**GATE_STAT** State of GATE Pin 1=On 0=Off	**PGIO_IN** State of PGIO Pin as Input 1=High 0=Low	**FET_STAT** V_{SENSE} > 2mV with GATE Off 1=Short 0=No Short	Reserved	Reserved	**OC_STAT** Overcurrent Condition 1=OC 0=No OC	**UV_STAT** Undervoltage Condition 1=UV 0=No UV	**OV_STAT** Overvoltage Condition 1=OV 0=No OV	0000,0000
0x01	**FAULT (B)** Fault Log and PGIO Input	Reserved	**PGIO_HIGH** PGIO as Input High Transition Detected 1=High 0=Low	**FET_FAULT** FET Short Detected 1=Fault 0=No Fault	Reserved	Reserved	**OC_FAULT** Overcurrent Fault Occurred 1=Fault 0=No Fault	**UV_FAULT** Undervoltage Fault Occurred 1=Fault 0=No Fault	**OV_FAULT** Overvoltage Fault Occurred 1=Fault 0=No Fault	0000,0000
0x02	**ALERT (C)** Controls if ALERT Pin is Pulled Low After a Fault is Logged in the Fault Register and PGIO Output	Reserved	**PGIO_OUT** Controls PGIO Pin State as Output 1=High 0=Low	**FET_ALERT** Enable Alert for FET Short Fault 1=Enable 0=Disable	Reserved	Reserved	**OC_ALERT** Enables Alert for Overcurrent Fault 1=Enable 0=Disable	**UV_ALERT** Enables Alert for Undervoltage Fault 1=Enable 0=Disable	**OV_ALERT** Enables Alert for Overvoltage Fault 1=Enable 0=Disable	0000,0000
0x03	**CONTROL (D)** Controls for Auto-Retry after Faults and GATE Switch State	**PGIO_CONFIG** Configures Behavior of PGIO Pin 00=Power Good Low, Open Drain 10=Power Good High, Open Drain 01=General Purpose Output, PGIO=C6 11=General Purpose Input, PGIO=Hi-Z		**ADC_WRITE** Halts ADC Operation and Enables Writes to ADC Registers 1=Enable 0=Disable	Reserved	**GATE_CTRL** Turns Gate On and Off 1=ON 0=OFF	**OC_AUTO** Enables Auto-Retry After an Overcurrent Fault 1=Enable 0=Disable	**UV_AUTO** Enables Auto-Retry After an Undervoltage Fault 1=Enable 0=Disable	**OV_AUTO** Enables Auto-Retry After an Overvoltage Fault 1=Enable 0=Disable	0000,y011 y=EN2 Pin State After Start-Up Delay
0x04	**SENSE (E)**	**SENSE_MSBS** 10-Bit ADC Current Sense Voltage Data (8 MSBs) with 62.5µV LSB and 64mV Full-Scale								xxxx,xxxx
0x05	**SENSE (F)**	**SENSE_LSBS** 10-Bit ADC Current Sense Voltage Data (2 LSBs)	Reserved Always Returns 0, Not Writable							xx00,0000
0x06	**ADIN2 (G)**	**ADIN2_MSBS** 10-Bit ADC ADIN2 Voltage Data (8 MSBs) with 2.5mV LSB and 2.56V Full-Scale								xxxx,xxxx
0x07	**ADIN2 (H)**	**ADIN2_LSBS** 10-Bit ADC ADIN2 Voltage Data (2 LSBs)	Reserved Always Returns 0, Not Writable							xx00,0000
0x08	**ADIN (I)**	**ADIN_MSBS** 10-Bit ADC ADIN Voltage Data (8 MSBs) with 2.5mV LSB and 2.56V Full-Scale								xxxx,xxxx
0x09	**ADIN (J)**	**ADIN_LSBS** 10-Bit ADC ADIN Voltage Data (2 LSBs)	Reserved Always Returns 0, Not Writable							xx00,0000

*Register address MSBs b7-b4 are ignored. Register 0x00 read only. Registers 0x04 through 0x09 writable if bit D5 set in Register 0x03.
NOTE: Underlined text denotes the default condition.

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RF, Magnetic Field Immunity

The isolator µModule technology used within the LTM9100 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 5.

Table 5. Test Frequency Field Strength

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

*non IEC method

PCB Layout

The high integration of the LTM9100 simplifies PCB layout. However, to optimize its electrical performance and isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- To achieve accurate current sensing, a Kelvin connection is recommended. The minimum trace width for 1oz copper foil is 0.02" per amp to minimize temperature rise. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µV/square. Small resistances add up quickly in high current applications.
- To improve noise immunity, put the resistive divider to the UV and OV pins close to the module and keep traces to V_{EE} short. Internal 10nF capacitors from the UVH pin and OV pin to V_{EE} help reject supply noise.
- Under heavily loaded conditions, V_{CC} and GND current can exceed 300mA. Use sufficient copper on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level.
- Input supply decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8µF to 22µF and ESR of 1Ω to 3Ω is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and V_{EE} is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure, which can radiate differential voltages formed between GND and V_{EE}. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can increase RF emissions.

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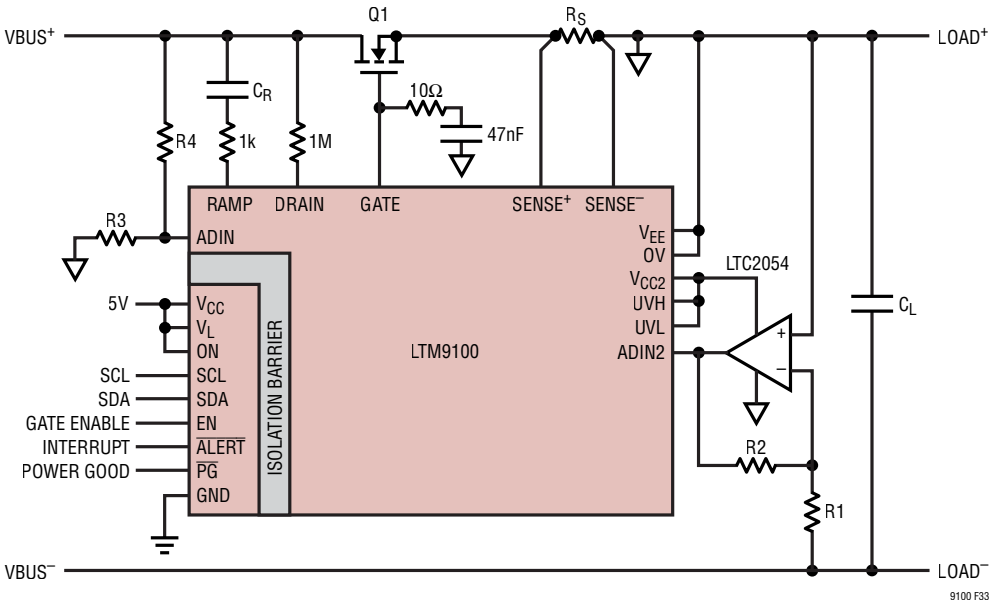
- For large ground planes a small capacitance (≤ 330pF) from GND to V_{EE}, either discrete or embedded within the substrate, provides a low impedance current return path for common mode current conducted through the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates the other component selection issues; however, the PCB must be four or more layers. Care must be exercised in applying either technique to ensure the voltage rating of the barrier is not compromised.
- In applications without an embedded PCB substrate capacitance, a slot may be added between the logic side and isolated side device pins. The slot extends the creepage path between terminals on the PCB side, and may reduce leakage caused by PCB contamination. The slot should be placed in the middle of the device terminals and extend beyond the package perimeter.

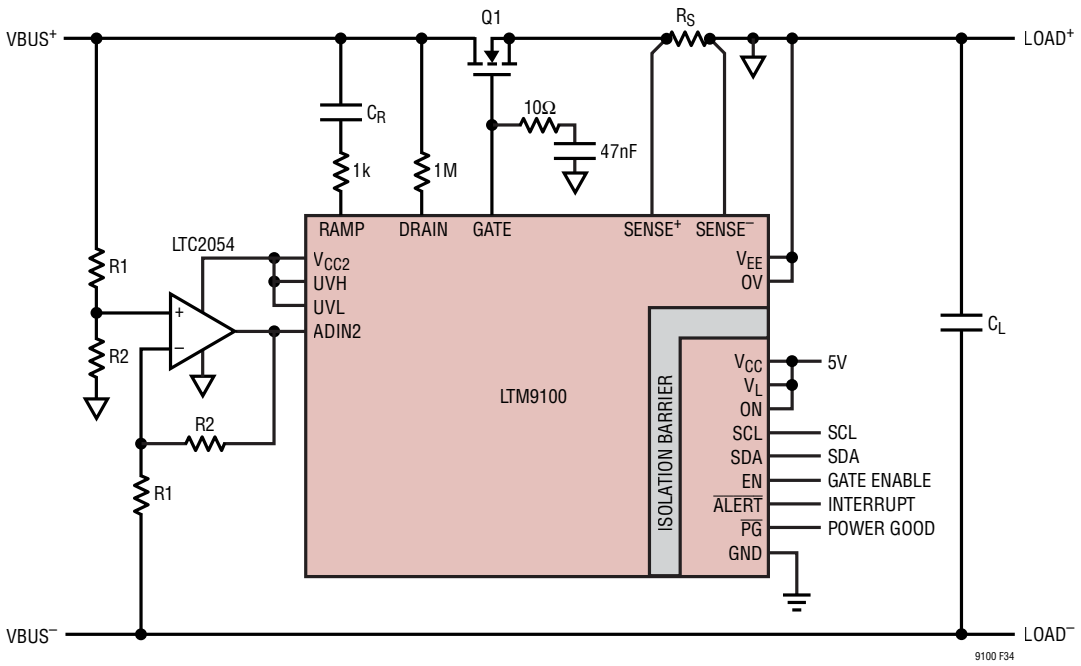
TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT:
ADR0, ADR1, $\overline{\text{ALERT2}}$, EN2, $\overline{\text{PG2}}$, PGIO, SCL2, SDA2, SS, TMR, V_S

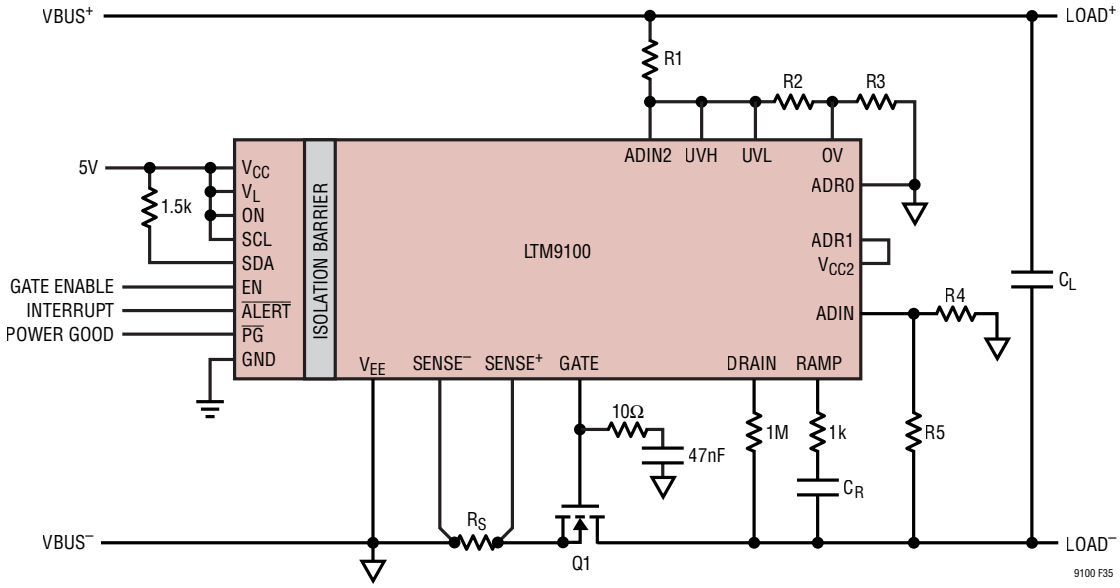
Figure 33. High Side Inrush Current Control with Switch Voltage Sense (R3, R4 to ADIN) and Load Voltage Sense (R1, R2 Buffered/Inverted to ADIN2)

TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT:
ADIN, ADR0, ADR1, $\overline{ALERT2}$, EN2, $\overline{PG2}$, PGIO, SCL2, SDA2, SS, TMR, V_S

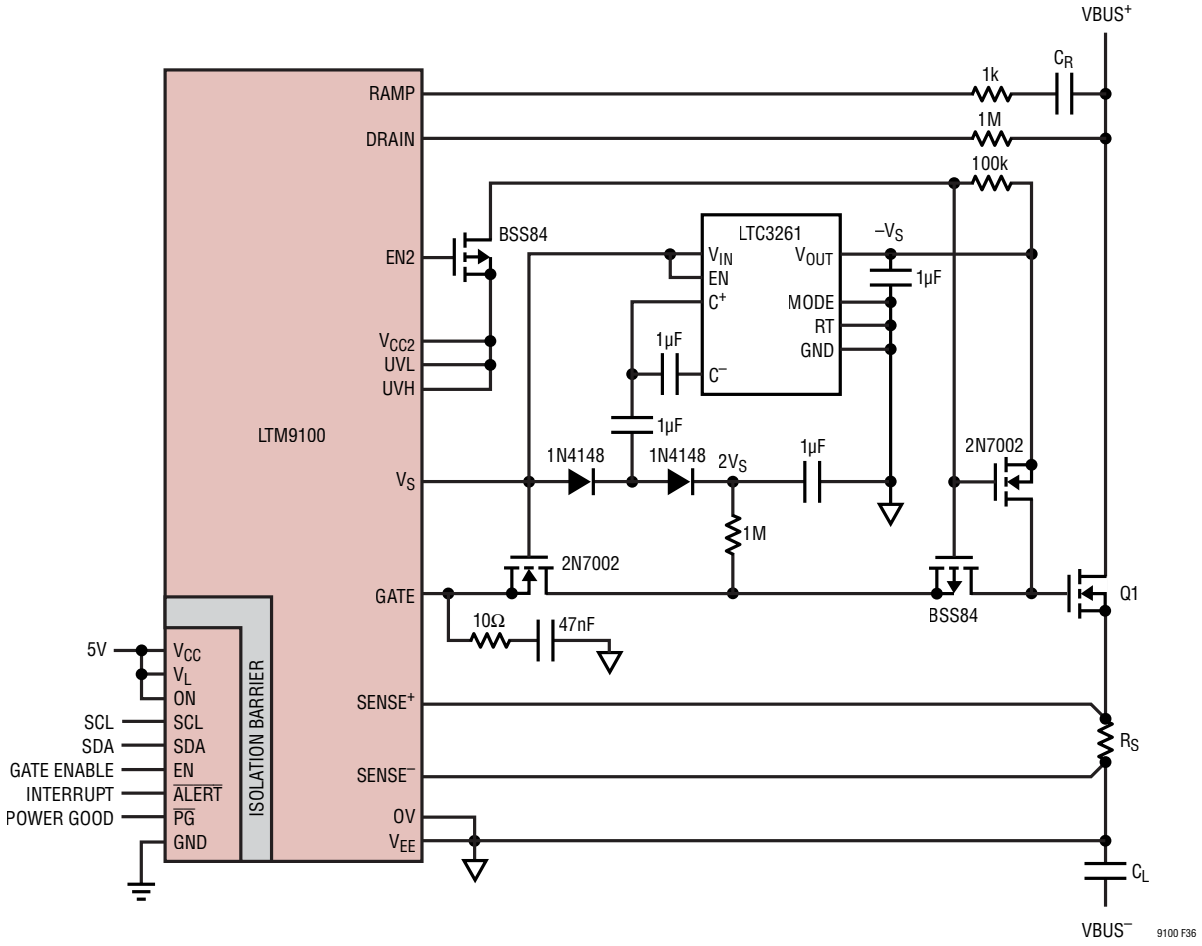
Figure 34. High Side Inrush Current Control with Line/Load Voltage Sense



PINS NOT USED IN THIS CIRCUIT:
$\overline{ALERT2}$, EN2, $\overline{PG2}$, PGIO, SCL2, SDA2, SS, TMR, V_S

Figure 35. Low Side Inrush Current Control with Line/Load Voltage Sense (R1, R2, R3 to ADIN2) and Switch Voltage Sense (R4, R5 to ADIN), Configured for 1 Wire Broadcast Mode

TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT:
ADIN, ADIN2, ADR0, ADR1, $\overline{\text{ALERT2}}$, $\overline{\text{PG2}}$, PGIO, SCL2, SDA2, SS, TMR

Figure 36. Boosted Gate Drive with Negative Off Bias

TYPICAL APPLICATIONS

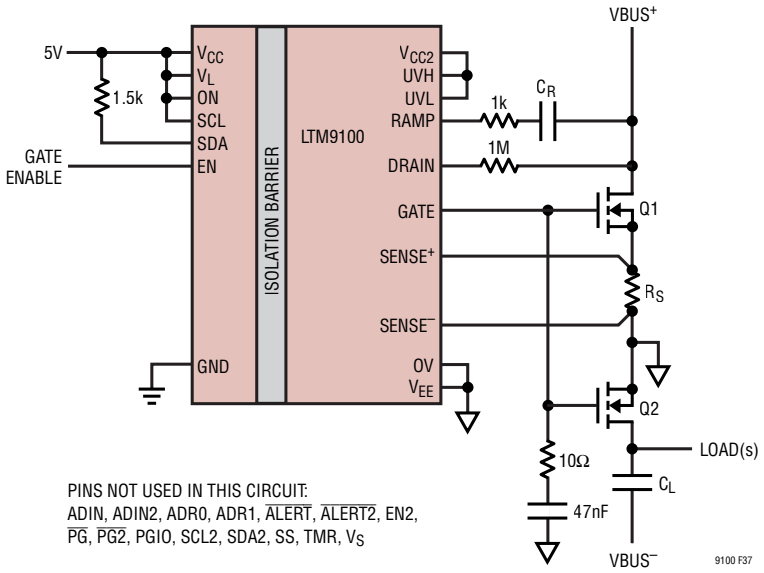


Figure 37. Switch Control with Reverse Conduction Blocking

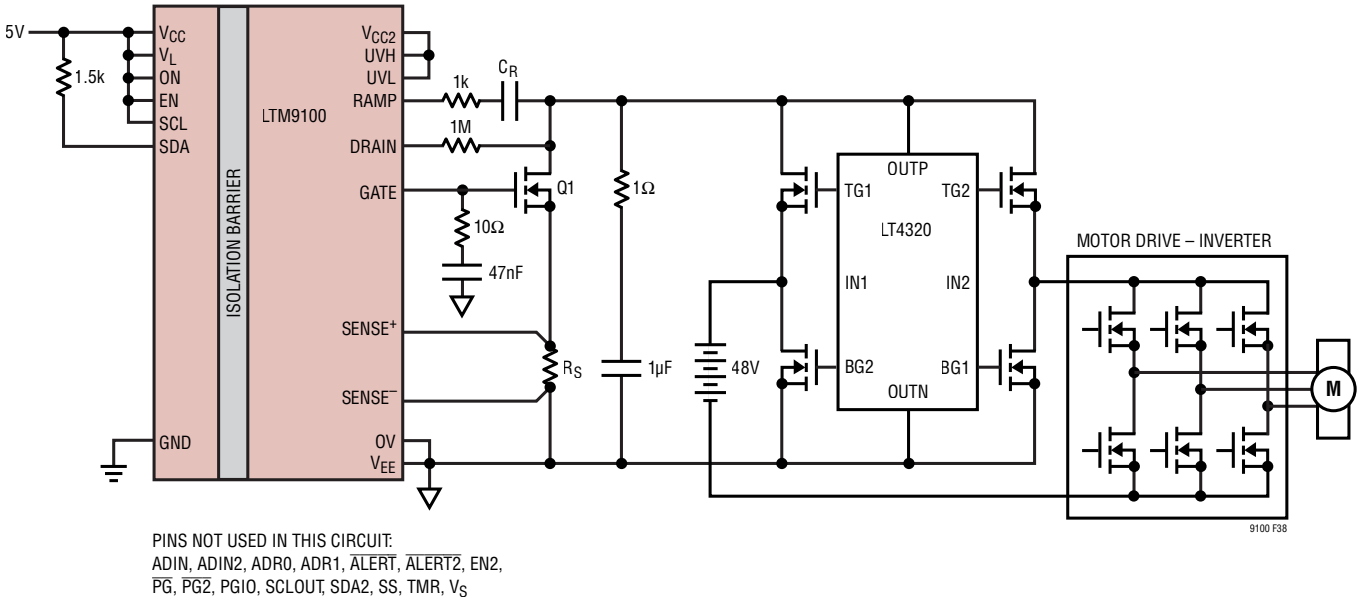
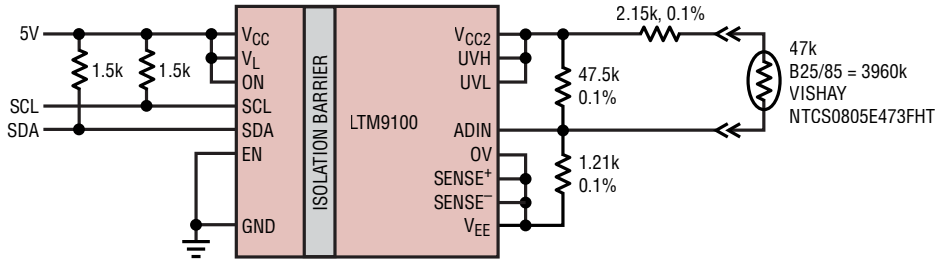


Figure 38. Bi-Directional Battery — Inverter Inrush Current Limiter

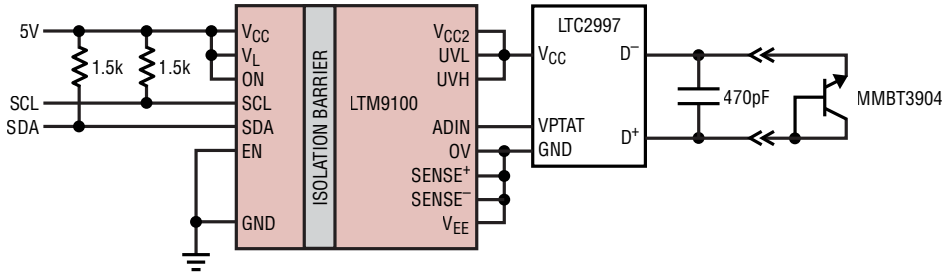
TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT:
ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, DRAIN, EN2, GATE,
$\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, RAMP, SCL2, SDA2, SS, TMR, V_S

$$V_{ADIN} = \frac{10mV}{°C}$$, RANGE = 0°C TO 150°C, RESOLUTION = 0.25°C, ACCURACY = ±2.5°C 9100 F39

Figure 39. Linear 10-Bit Remote (or Local) Thermistor Temperature Sense



PINS NOT USED IN THIS CIRCUIT:
ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, DRAIN, EN2, GATE,
$\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, RAMP, SCL2, SDA2, SS, TMR, V_S, V_{REF}

$$V_{ADIN} = \frac{4mV}{K}$$, RANGE = –55°C TO 150°C, RESOLUTION = 0.625°C, ACCURACY = ±1°C 9100 F40

Figure 40. Precision 10-Bit Remote Temperature Sense

TYPICAL APPLICATIONS

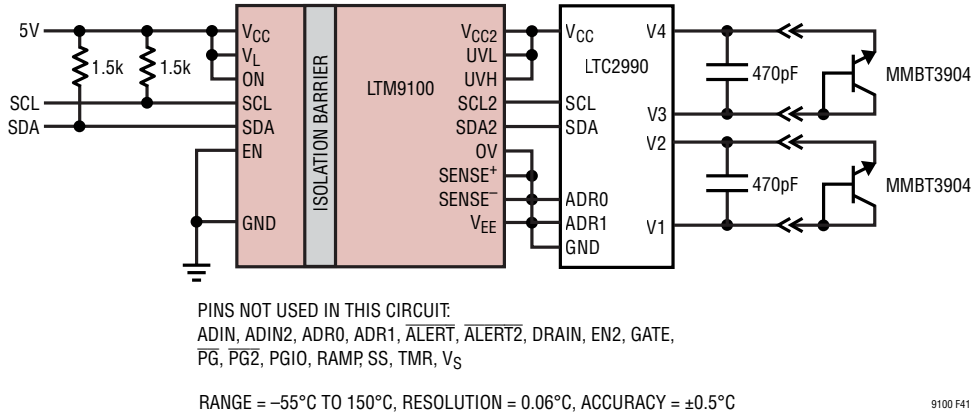


Figure 41. I²C Precision 14-Bit Remote (or Local) Dual Temperature Sense

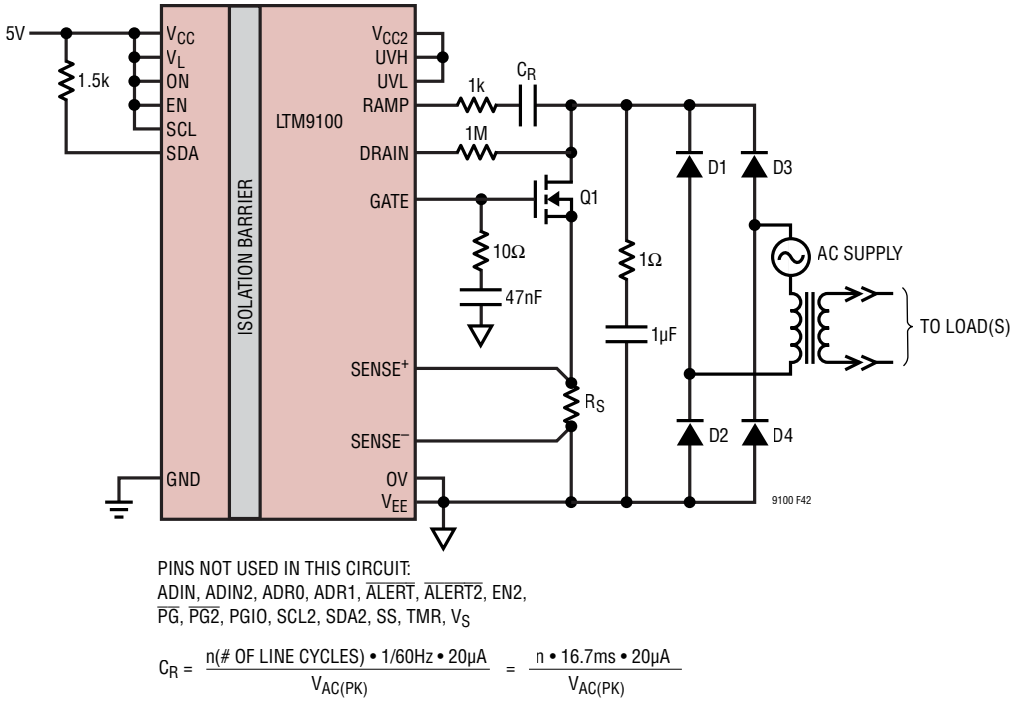
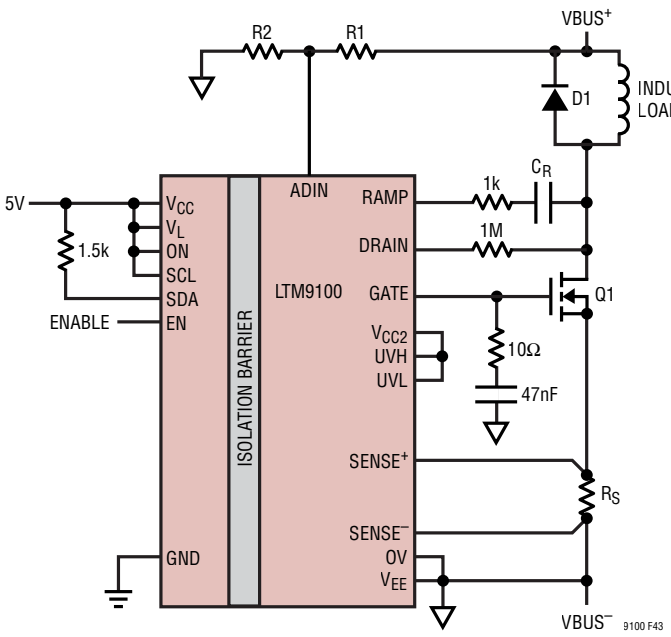


Figure 42. Transformer Inrush Current Limiter, n Line Cycle Ramp

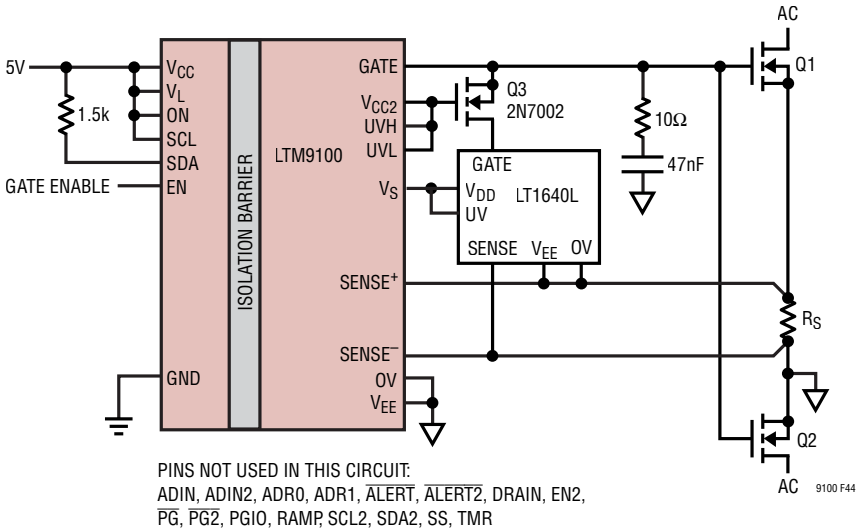
TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT:
ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, EN2,
$\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, SCL2, SDA2, SS, TMR, V_S

$$C_R = \frac{\Delta t \bullet 20\mu A}{V_{BUS}}$$

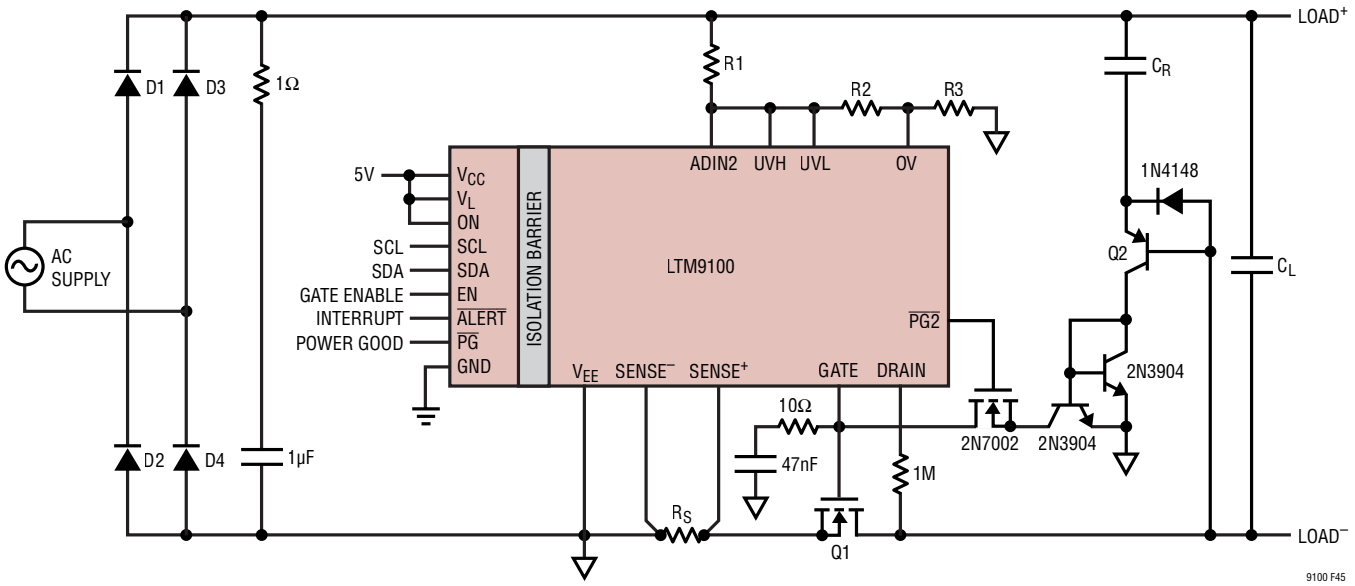
Figure 43. Inductive Load Current Limiter – Controlled Turn-On



PINS NOT USED IN THIS CIRCUIT:
ADIN, ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, DRAIN, EN2,
$\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, RAMP, SCL2, SDA2, SS, TMR

Figure 44. AC Circuit Breaker

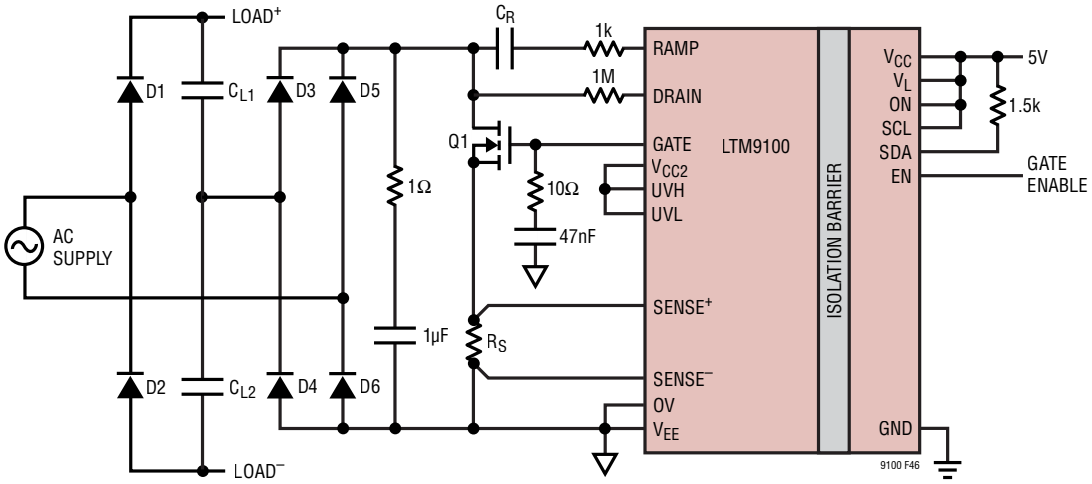
TYPICAL APPLICATIONS



PINS NOT USED IN THIS CIRCUIT:
ADIN, ADR0, ADR1, $\overline{\text{ALERT2}}$, EN2, PGIO,
RAMP, SCL2, SDA2, SS, TMR, V_{CC2}, V_S

$I_{INRUSH} \approx 10\mu A \bullet \frac{C_L}{C_R}$, Q2 VOLTAGE RATING > $V_{AC(PK)}$

Figure 45. Low Side Switch Controller with Rectified AC-DC Link (DC Bus with Ripple)



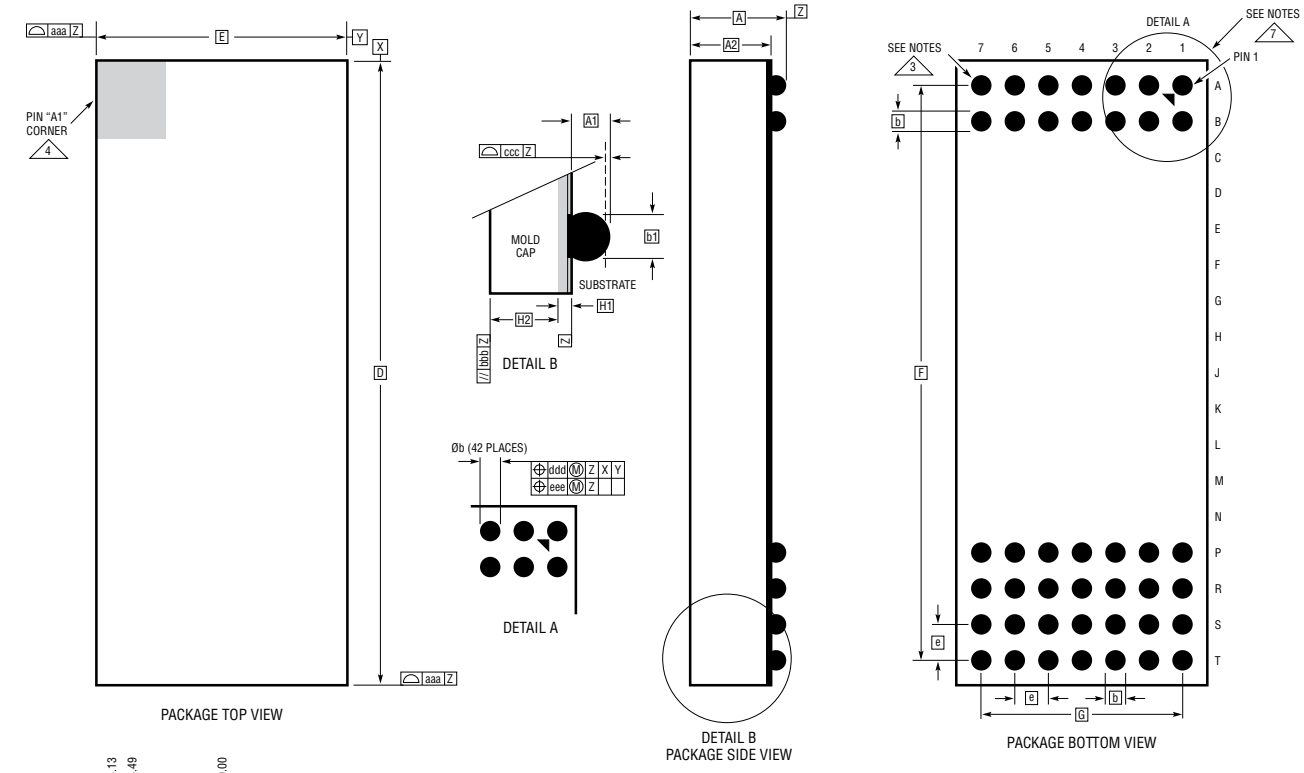
PINS NOT USED IN THIS CIRCUIT:
ADIN, ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, EN2,
$\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, SCL2, SDA2, SS, TMR, V_S

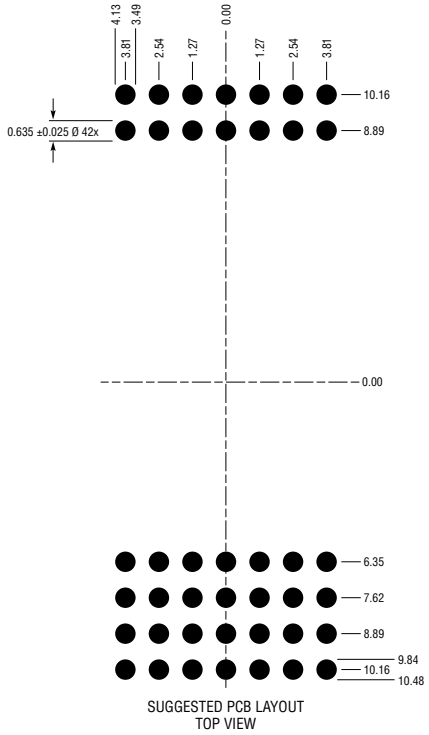
Figure 46. Inrush Current Limiting for AC Voltage Doubler

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM9100#packaging for the most recent package drawings.

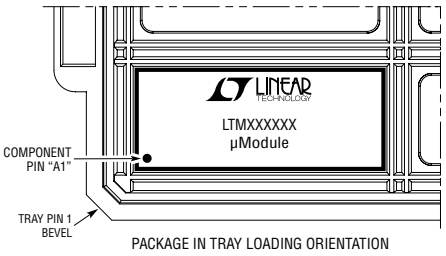
BGA Package
42-Lead (22mm × 9mm × 5.16mm)
(Reference LTC DWG# 05-08-1973 Rev Ø)





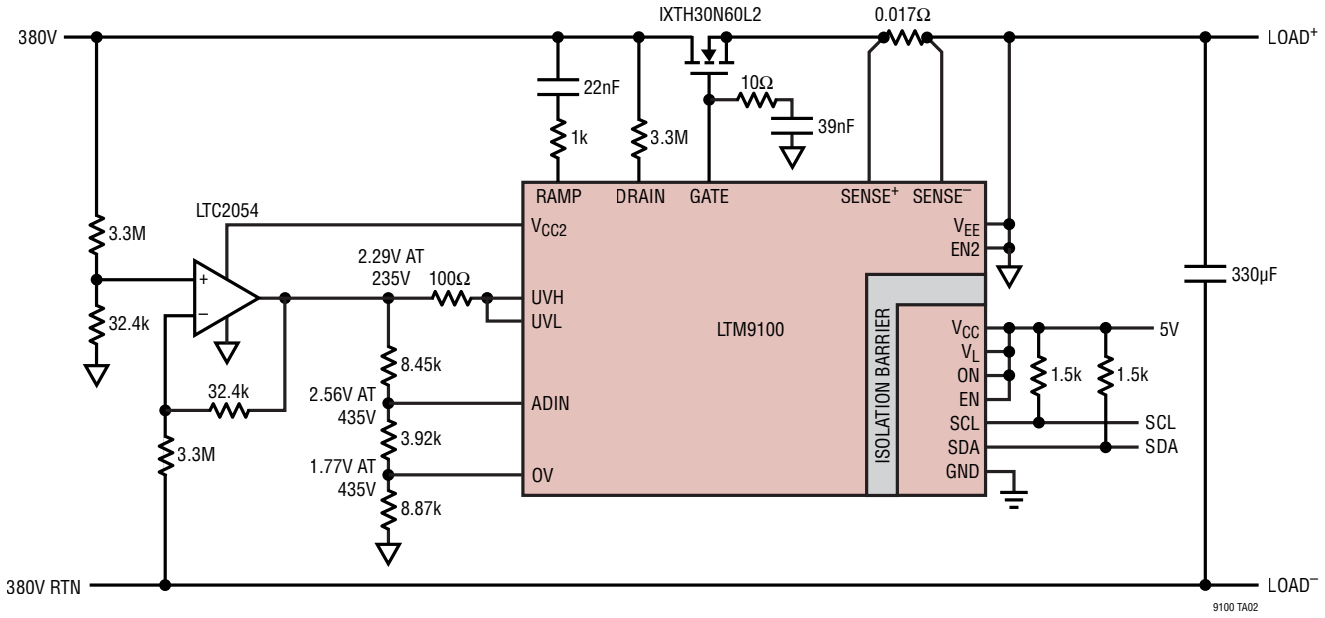
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.91	5.16	5.41	
A1	0.50	0.60	0.70	
A2	4.41	4.56	4.71	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		22.0		
E		9.0		
e		1.27		
F		20.32		
G		7.62		
H1	0.46	0.56	0.66	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.15	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 42				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



TYPICAL APPLICATION

High Side 380V Bus Inrush Current Limiter with Line Voltage Monitor and I²C Only Control



PINS NOT USED IN THIS CIRCUIT:
ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, $\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, SCL2, SDA2, SS, TMR, V_S

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2881	Isolated RS485/RS422 µModule Transceiver with Integrated DC/DC Converter	20Mbps 2500V_{RMS} Isolation with Power in LGA/BGA Package
LTM2882	Dual Isolated RS232 µModule Transceiver with Integrated DC/DC Converter	2500V_{RMS} Isolation with Power in LGA/BGA Package
LTM2883	SPI/Digital or I²C Isolated µModule with Adjustable 5V, and ±12.5V Nominal Voltage Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2884	Isolated High Speed USB µModule with Integrated DC/DC Converter	2500V_{RMS} Isolation with Power in BGA Package
LTM2885	Isolated RS485/RS422 µModule Transceiver with integrated DC/DC converter	20Mbps 6500V_{RMS} Isolation with Power in BGA Package
LTM2886	SPI/Digital or I²C Isolated µModule with Adjustable 5V, and Fixed ±5V Power Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2887	SPI/Digital or I²C Isolated µModule with Two Adjustable 5V Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2889	Isolated CAN µModule Transceiver with Integrated DC/DC Converter	4Mbps 2500V_{RMS} Isolation with Power in BGA Package
LTM2892	SPI/Digital or I²C Isolated µModule	3500V_{RMS} Isolation in BGA Package
LTM2893	Complete 100MHz SPI ADC µModule Isolator	6000V_{RMS} Isolation in Surface Mount BGA
LTM2894	Complete Isolated USB µModule Transceiver	7500V_{RMS} Isolation in Surface Mount Package
LTC1535	Isolated RS485 Transceiver	2500V_{RMS} Isolation with External Transformer Drive
LTC4260	Positive High Voltage Hot Swap Controller	With I²C and ADC, Supplies from 8.5V to 80V
LTC4261	Negative High Voltage Hot Swap Controller	With I²C and ADC, Supplies from –12V to –100V

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