

## Absolute Maximum Ratings (Note 1)

Input Supply Voltage (+V <sub>IN</sub> ) .....	40V
Sense Inputs .....	+V <sub>IN</sub>
SCR Trigger Current (Note 2) .....	300mA
Indicator Output Voltage .....	40V

Indicator Output Sink Current .....	50mA
Operating Junction Temperature	
Hermetic (J Package) .....	150°C
Plastic (N, DW Packages) .....	150°C
Storage Temperature Range .....	-65°C to 150°C
RoHS Peak Package Solder Reflow (40 sec. max. exp.)...260°C (+0, -5)	

Note 1. Values beyond which damage may occur.

Note 2. At higher input voltages, a dissipation limiting resistor, R<sub>G</sub> is required. See Figure 2.

## Thermal Data

J Package:

Thermal Resistance-Junction to Case, θ <sub>JC</sub> .....	25°C/W
Thermal Resistance-Junction to Ambient, θ <sub>JA</sub> .....	70°C/W

N Package:

Thermal Resistance-Junction to Case, θ <sub>JC</sub> .....	30°C/W
Thermal Resistance-Junction to Ambient, θ <sub>JA</sub> .....	60°C/W

DW Package:

Thermal Resistance-Junction to Case, θ <sub>JC</sub> .....	35°C/W
Thermal Resistance-Junction to Ambient, θ <sub>JA</sub> .....	90°C/W

Note A. Junction Temperature Calculation: T<sub>J</sub> = T<sub>A</sub> + (P<sub>D</sub> × J<sub>A</sub>).

Note B. The above numbers for θ<sub>JC</sub> are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ<sub>JA</sub> numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

## Recommended Operating Conditions (Note 3)

Input Supply Voltage (+V <sub>IN</sub> ) .....	4.7V to 40V
Current Limit Common Mode	
Input Voltage Range .....	0V to +V <sub>IN</sub> -3V
Reference Load Current .....	0 to 10mA
Indicator Output Voltage .....	4.7V to 40V
Indicator Output Current .....	0 to 10mA

Delay Timing Capacitor (Note 4) .....	0 to 1μF
Operating Ambient Temperature Range	
SG1544 .....	-55°C to 125°C
SG2544 .....	-25°C to 85°C
SG3544 .....	0°C to 70°C

Note 3: Range over which the device is functional.

Note 4. Larger value capacitor may be used with peak current limiting. See Figure 2.

## Electrical Characteristics

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1544 with -55°C ≤ T<sub>A</sub> ≤ 125°C, SG2544 with -25°C ≤ T<sub>A</sub> ≤ 85°C, SG3544 with 0°C ≤ T<sub>A</sub> ≤ 70°C, and +V<sub>IN</sub> = 10V. Indicator outputs have 2kΩ pull-up resistors. All electrical ratings and specifications are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

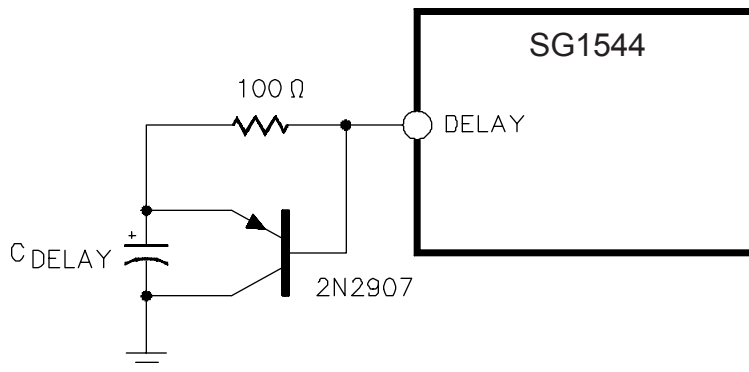
Parameter	Test Conditions	SG1544/SG2544			SG3544			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>Supply Section</b>								
Input Voltage Range	T <sub>J</sub> = 25°C to T <sub>MAX</sub>	4.5		40	4.5		40	V
		4.7		40	4.7		40	V
Supply Current	+V <sub>IN</sub> = 40V, Outputs open		7	10		7	10	mA
<b>Reference Section</b>								
Output Voltage	T <sub>J</sub> = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
		2.45		2.55	2.40		2.60	V
Line Regulation	+V <sub>IN</sub> = 5 to 30V		1	5		1	5	mV
Load Regulation	I <sub>REF</sub> = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V <sub>REF</sub> = 0V	12	25	40	12	25	40	mA
Temperature Stability			.005			.005		%/°C

## Electrical Characteristics (Continued)

Parameter	Test Conditions	SG1544/SG2544			SG3544			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>Comparator Section</b>								
Input Threshold (Note 5)	$T_J = 25^\circ\text{C}$	2.45	2.50	2.55	2.40	2.50	2.60	V
		2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense input = 0V		0.3	1.0		0.3	1.0	$\mu\text{A}$
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	8		6	8	V
Delay Charging Current	$V_D = 0\text{V}$	200	250	300	200	250	300	$\mu\text{A}$
Indicate Saturation	$I_L = 10\text{mA}$		0.2	0.5		0.2	0.5	V
Indicate Leakage	$V_{IND} = 40\text{V}$		.01	1.0		0.1	1.0	$\mu\text{A}$
Propagation Delay	$V_{O.V. N.I. IN} = 2.7\text{V}$ , $V_{U.V. INV. IN} = 2.3\text{V}$ , $T_J = 25^\circ\text{C}$							
	$C_D = 0$		400			400		ns
	$C_D = 1\mu\text{F}$		10			10		ms
<b>SCR Trigger Section</b>								
Peak Output Current	$+V_{IN} = 5\text{V}$ , $R_G = 0$ , $V_O = 0$	100	200	400	100	200	400	mA
Peak Output Voltage	$+V_{IN} = 15\text{V}$ , $I_O = 100\text{mA}$	12	13		12	13		V
Output Off Voltage	$+V_{IN} = 40\text{V}$ , $R_L = 1\text{k}\Omega$		0	0.1		0	0.1	V
Remote Activate Current	REM. ACT. pin = Gnd		0.4	0.8		0.4	0.8	mA
Remote Activate Voltage	REM. ACT pin open		2	6		2	6	V
Reset Current	RESET pin = Gnd, REM. ACT. = Gnd		0.4	0.8		0.4	0.8	mA
Reset Voltage	RESET pin open, REM. ACT. = Gnd		2	6		2	6	V
Output Current Rise Time	$R_L = 50\Omega$ , $T_J = 25^\circ\text{C}$ , $C_D = 0$		400			400		mA/ $\mu\text{s}$
Prop. Delay from REM. ACT. Pin	$V_{REM. ACT.} = 0.4\text{V}$		300			300		ns
Prop. Delay fom O.V. N.I. IN Pin	$V_{O.V. N.I. INPUT} = 2.7\text{V}$		500			500		ns
<b>Current Limit Section</b>								
Input Voltage Range		0		$V_{IN} -3\text{V}$	0		$V_{IN} -3\text{V}$	V
Input Bias Current	OFFSET/COMP pin open, $V_{CM} = 0\text{V}$		0.3	1.0		0.3	1.0	$\mu\text{A}$
Input Offset Voltage	OFFSET/COMP pin open, $V_{CM} = 0\text{V}$		0	10		0	15	mV
	$10\Omega$ from OFFSET/COMP pin to Gnd, $T_J = 25^\circ\text{C}$	80	100	120	70	100	130	mV
CMRR	$0 \leq V_{CM} \leq 12\text{V}$ , $V_{IN} = 15\text{V}$	60	70		60	70		dB
AVOL	OFFSET/COMP pin open, $V_{CM} = 0\text{V}$	72	80		72	80		dB
Output Saturation	$I_L = 10\text{mA}$		0.2	0.5		0.2	0.5	V
Output Leakage	$V_{IND} = 40\text{V}$		.01	1.0		.01	1.0	$\mu\text{A}$
Small Signal Bandwidth	$A_V = 0\text{dB}$ , $T_J = 25^\circ\text{C}$		5			5		MHz
Propagation Delay	$V_{OVERDRIVE} = 100\text{mV}$ , $T_J = 25^\circ\text{C}$		200			200		ns

Note 5. Input voltage rising on O.V. N.I. INPUT and falling on U.V. INV. INPUT.

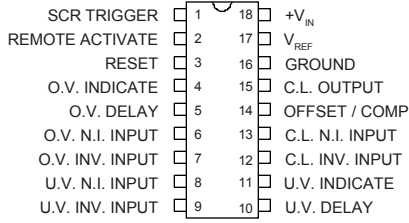
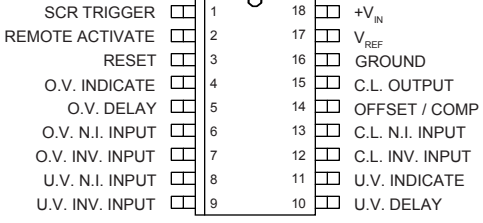
## Application Information



**Figure 2** - Surge Limit Circuit for Large Delay Capacitors

The 100 ohm resistor ( $R_G$ ) limits the peak discharge current into the SG1544 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

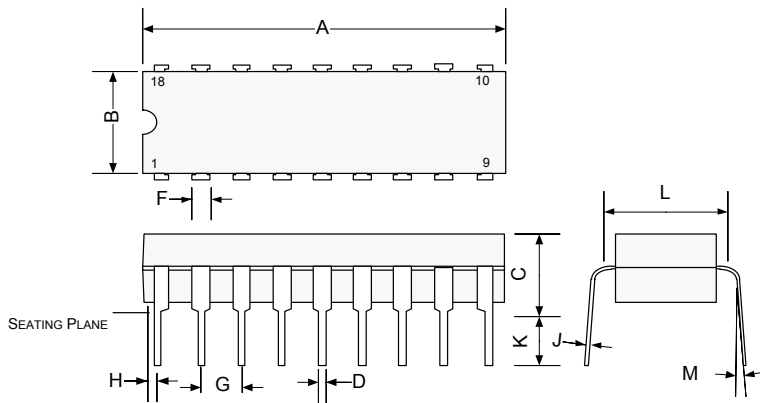
## Connection Diagrams and Ordering Information (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1544J-883B SG1544J-DESC SG1544J SG2544J SG3544J	-55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	 <p>N Package: RoHS Compliant / Pb-free Transition DC: 0503 N Package: RoHS / Pb-free 100% Matte Tin lead Finish</p>
18-PIN PLASTIC DIP N - PACKAGE	SG2544N SG3544N	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC SOIC DW - PACKAGE	SG2544DW SG3544DW	-25°C to 85°C 0°C to 70°C	 <p>DW Package: RoHS Compliant / Pb-free Transition DC: 0516 DW Package: RoHS / Pb-free 100% Matte Tin lead Finish</p>

- Note
1. Contact factory for DESC product availability.
  2. All packages are viewed from the top.
  3. J package uses Sn63/Pb37 hot solder lead finish, contact factory for availability of a RoHS version.

# Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.

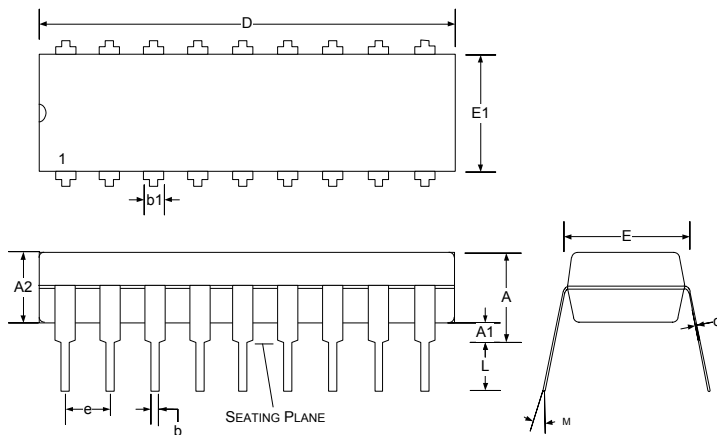


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	24.38	-	0.960
B	5.59	7.11	0.220	0.280
C	-	5.08	-	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	-	2.03	-	0.080
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.37	7.87	0.290	0.310
M	-	15°	-	15°

**Note:**

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

**Figure 3 - J 18-Pin CERDIP Package Dimensions**



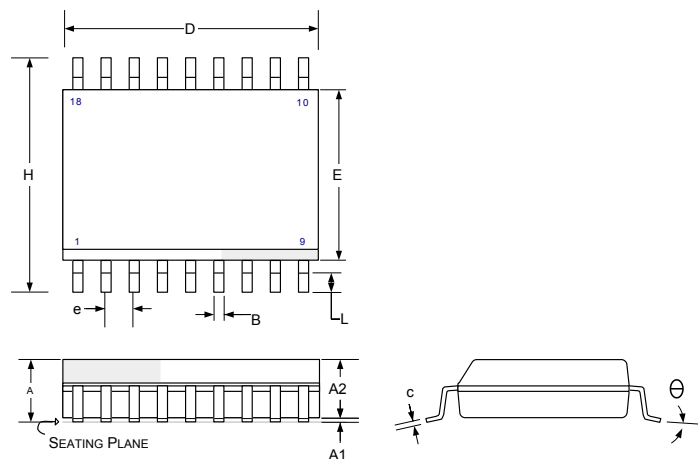
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.33	-	0.210
A1	0.38	-	0.015	-
A2	3.30 Typ		0.130 Typ	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	22.35	23.34	0.880	0.920
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	3.81	0.115	0.150
M	-	15°	-	15°

**Note:**

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

**Figure 4 - N 18-Pin Plastic Dual Inline Package Dimensions**

## Package Outline Dimensions (continued)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
A2	2.20	2.55	0.086	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	11.40	11.70	0.449	0.461
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
$\theta$	0°	8°	0°	8°
*LC	–	0.10	–	0.004

Lead co planarity

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

**Figure 5 • DW 18-Pin Plastic Wide-body SOIC (SOWB) Package Dimensions**



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