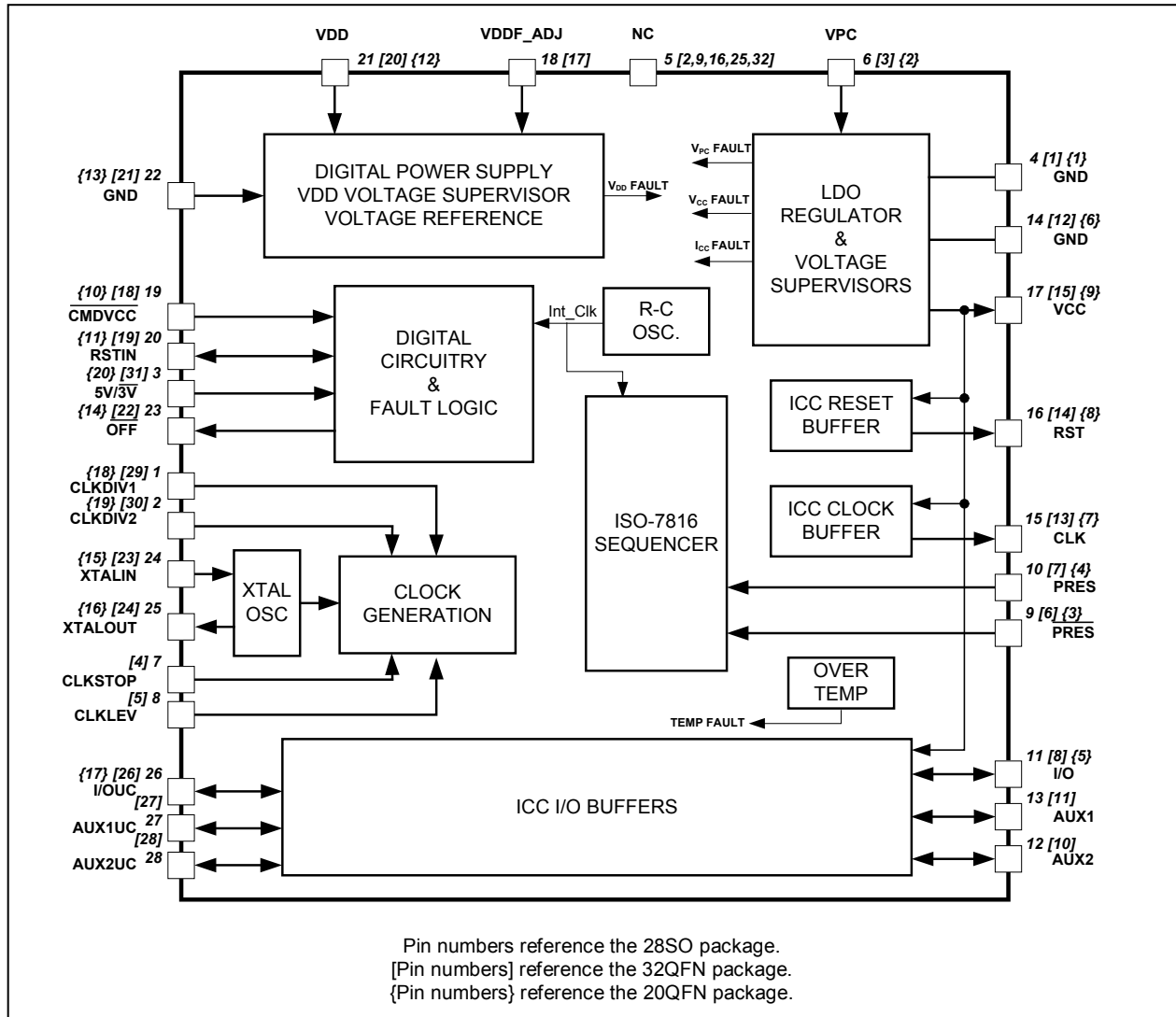


**FUNCTIONAL DIAGRAM**



**Figure 1: 73S8024RN Block Diagram**

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## 1 Pin Description

### CARD INTERFACE

Name	Pin 28SO	Pin 20QFN	Pin 32QFN	Description
I/O	11	5	8	Card I/O: Data signal to/from card. Includes a pull-up resistor to $V_{CC}$ .
AUX1	13	–	11	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC}$ .
AUX2	12	–	10	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC}$ .
RST	16	8	14	Card reset: provides reset (RST) signal to card.
CLK	15	7	13	Card clock: provides clock signal (CLK) to card. The rate of this clock is determined by the external crystal frequency or frequency of the external clock signal applied on XTALIN and CLKDIV selections.
PRES	10	4	7	Card Presence switch: active high indicates card is present. Should be tied to GND when not used, but it includes a high-impedance pull-down current source.
$\overline{PRES}$	9	3	6	Card Presence switch: active low indicates card is present. Should be tied to $V_{DD}$ when not used, but it includes a high-impedance pull-up current source.
VCC	17	9	15	Card power supply – logically controlled by sequencer, output of LDO regulator. Requires an external filter capacitor to the card GND.
GND	14	6	12	Card ground.

### MISCELLANEOUS INPUTS AND OUTPUTS

Name	Pin 28SO	Pin 20QFN	Pin 32QFN	Description
XTALIN	24	15	23	Crystal oscillator input: can either be connected to crystal or driven as a source for the card clock.
XTALOUT	25	16	24	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as external clock input.
VDDF_ADJ	18	–	17	$V_{DD}$ fault threshold adjustment input: this pin can be used to adjust the $V_{DDF}$ values (that controls deactivation of the card). Must be left open if unused.
NC	5	–	2, 9, 16, 25, 32	Non-connected pin.

### POWER SUPPLY AND GROUND

Name	Pin 28SO	Pin 20QFN	Pin 32QFN	Description
VDD	21	12	20	System interface supply voltage and supply voltage for internal circuitry.
VPC	6	2	3	LDO regulator power supply source.
GND	4	1	1	LDO Regulator ground.
GND	22	13	21	Digital ground.

## MICROCONTROLLER INTERFACE

Name	Pin 28SO	Pin 20QFN	Pin 32QFN	Description															
$\overline{\text{CMDVCC}}$	19	10	18	Command VCC (negative assertion): Logic low on this pin causes the LDO regulator to ramp the $V_{CC}$ supply to the card and initiates a card activation sequence, if a card is present.															
5V/3V	3	20	31	5 volt / 3 volt card selection: Logic one selects 5 volts for $V_{CC}$ and card interface, logic low selects 3 volt operation. When the part is to be used with a single card voltage, this pin should be tied to either GND or $V_{DD}$ . However, it includes a high impedance pull-up resistor to default this pin high (selection of 5V card) when not connected.															
CLKSTOP	7	–	4	Stops the card clock signal during a card session when set high (card clock STOP mode). Internal pull-down resistor allows this pin to be left as an open circuit if the clock STOP mode is not used.															
CLKLVL	8	–	5	Sets the logic level of the card clock STOP mode when the clock is de-activated by setting pin 7 high. Logic low selects card STOP low. Logic high selects card STOP high. Internal pull-down resistor allows this pin to be left as an open circuit if the clock STOP mode is not used.															
CLKDIV1 CLKDIV2	1 2	18 19	29 30	Sets the divide ratio from the XTAL oscillator (or external clock input) to the card clock. These pins include pull-down resistors.  <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CLKDIV1</th> <th>CLKDIV2</th> <th>CLOCK RATE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>XTALIN/8</td> </tr> <tr> <td>0</td> <td>1</td> <td>XTALIN/4</td> </tr> <tr> <td>1</td> <td>1</td> <td>XTALIN/2</td> </tr> <tr> <td>1</td> <td>0</td> <td>XTALIN</td> </tr> </tbody> </table>	CLKDIV1	CLKDIV2	CLOCK RATE	0	0	XTALIN/8	0	1	XTALIN/4	1	1	XTALIN/2	1	0	XTALIN
CLKDIV1	CLKDIV2	CLOCK RATE																	
0	0	XTALIN/8																	
0	1	XTALIN/4																	
1	1	XTALIN/2																	
1	0	XTALIN																	
$\overline{\text{OFF}}$	23	14	22	Interrupt signal to the processor. Active Low - Multi-function indicating fault conditions and card presence. Open drain output configuration. It includes an internal 21k $\Omega$ pull-up to $V_{DD}$ .															
RSTIN	20	11	19	Reset Input: This signal is the reset command to the card.															
I/OUC	26	17	26	System controller data I/O to/from the card. Includes a pull-up resistor to $V_{DD}$ .															
AUX1UC	27	–	27	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to $V_{DD}$ .															
AUX2UC	28	–	28	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to $V_{DD}$ .															

## 2 System Controller Interface

Three separated digital inputs allow direct control of the card interface from the host as follows:

- Pin  $\overline{\text{CMDVCC}}$ : When low, starts an activation sequence.
- Pin RSTIN: controls the card Reset signal (when enabled by the sequencer).
- Pin  $5V/\overline{3V}$ : Defines the card voltage.

Card clock is controlled by four digital inputs:

- CLKDIV1 and CLKDIV2 define the division rate for the clock frequency, from the input clock frequency (crystal or external clock).
- CLKSTOP (active high) allows card power down mode by stopping the card clock.
- CLKLEV defines the card clock level of the card power down mode.

Interrupt output to the host: As long as the card is not activated, the  $\overline{\text{OFF}}$  pin informs the host about the card presence only (Low = No card in the reader). When  $\overline{\text{CMDVCC}}$  is set low (Card activation sequence requested from the host), low level on  $\overline{\text{OFF}}$  means a fault has been detected (e.g. card removal during card session, or voltage fault, or thermal / over-current fault) that automatically initiates a deactivation sequence.

### 3 Power Supply and Voltage Supervision

The 73S8024RN smart card interface IC incorporates a LDO voltage regulator. The voltage output is controlled by the digital input  $5V/3V$ . This regulator is able to provide either 3V or 5V card voltage from the power supply applied on the VPC pin.

Digital circuitry is powered by the power supply applied on the VDD pin.  $V_{DD}$  also defines the voltage range to interface with the system controller.

Three voltage supervisors constantly check the presence of the voltages  $V_{DD}$ ,  $V_{PC}$  and  $V_{CC}$ . A card deactivation sequence is forced upon fault of any of these voltage supervisors. The two voltage supervisors for  $V_{PC}$  and  $V_{CC}$  are linked so that a fault is generated to activate a deactivation sequence when the voltage  $V_{PC}$  becomes lower than  $V_{CC}$ . It allows the 73S8024RN to operate at lower  $V_{PC}$  voltage when using 3V cards only. The voltage regulator can provide a current of at least 90mA on  $V_{CC}$  that comply easily with EMV 4.0 and NDS specifications. The  $V_{PC}$  voltage supervisor threshold values are defined from applicable standards (EMV and NDS). A third voltage supervisor monitors the  $V_{DD}$  voltage. It is used to initialize the ISO 7816-3 sequencer at power-on, and to deactivate the card at power-off or upon fault. The voltage threshold of the  $V_{DD}$  voltage supervisor is internally set by default to 2.3V nominal. However, it may be desirable, in some applications, to modify this threshold value. The pin  $VDDF\_ADJ$  (pin 18 in the SO package, pin 17 in the 32QFN package, not supported in the 20QFN package) is used to connect an external resistor  $R_{EXT}$  to ground to raise the  $V_{DD}$  fault voltage to another value  $V_{DDF}$ . The resistor value is defined as follows:

$$R_{EXT} = 56k\Omega / (V_{DDF} - 2.33)$$

An alternative method (more accurate) of adjusting the  $V_{DD}$  fault voltage is to use a resistive network of R3 from the pin to supply and R1 from the pin to ground (see applications diagram). In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated Kx. Kx is defined as  $R1/(R1+R3)$ . Kx is calculated as:

$$Kx = (2.789 / V_{TH}) - 0.6125 \text{ where } V_{TH} \text{ is the desired new threshold voltage.}$$

To determine the values of R1 and R3, use the following formulas.

$$R3 = 24000 / Kx \quad R1 = R3 * (Kx / (1 - Kx))$$

Taking the example above, where a  $V_{DD}$  fault threshold voltage of 2.7V is desired, solving for Kx gives:

$$\rightarrow Kx = (2.789 / 2.7) - 0.6125 = 0.42046.$$

$$\text{Solving for R3 gives: } \rightarrow R3 = 24000 / 0.42046 = 57080.$$

$$\text{Solving for R1 gives: } \rightarrow R1 = 57080 * (0.42046 / (1 - 0.42046)) = 41412.$$

Using standard 1 % resistor values gives  $R3 = 57.6K\Omega$  and  $R1 = 42.4K\Omega$ .

These values give an equivalent resistance of  $Kx = 0.4228$ , a 0.6% error.

If the 2.3V default threshold is used, this pin must be left unconnected. The 20QFN package has the  $V_{DD}$  fault threshold fixed at this default value.

## 4 Card Power Supply

The card power supply is internally provided by the LDO regulator, and controlled by the digital ISO 7816-3 sequencer. Card voltage selection is carried out by the digital input 5V/3V.

### Choice of the V<sub>CC</sub> Capacitor:

Depending on the applications, the requirements in terms of both V<sub>CC</sub> minimum voltage and transient currents that the interface must be able to provide to the card are different. An external capacitor must be connected between the VCC pin and to the card ground in order to guarantee stability of the LDO regulator, and to handle the transient requirements. The type and value of this capacitor can be optimized to meet the desired specification. Table 1 shows the recommended capacitors for each V<sub>PC</sub> power supply configuration and applicable specification.

**Table 1: Choice of V<sub>CC</sub> Pin Capacitor**

Specification Requirements			System Requirements		
Specification	Min V <sub>CC</sub> Voltage Allowed During Transient Current	Max Transient Current Charge	Min V <sub>PC</sub> Power Supply Required	Capacitor Type	Capacitor Value
EMV 4.0	4.6V	30nA.s	4.75V	X5R/X7R w/ ESR < 100mΩ	3.3 μF
ISO 7816-3	4.5V	20nA.s	4.75V		1 μF
NDS	4.6V	40nA.s	4.85V		1 μF

Note: Capacitor value for NDS implementation is also defined by the deactivation time requirement.

## 5 Over-Temperature Monitor

A built-in detector monitors die temperature. Upon an over-temperature condition, a card deactivation sequence is initiated, and an error or fault condition is reported to the system controller.

## 6 On-Chip Oscillator and Card Clock

The 73S8024RN device has an on-chip oscillator that can generate the smart card clock using an external crystal (connected between the pins XTALIN and XTALOUT) to set the oscillator frequency. When the clock signal is available from another source, it can be connected to the pin XTALIN, and the pin XTALOUT should be left unconnected.

The card clock frequency may be chosen between four different division rates, defined by digital inputs CLKDIV 1 and CLKDIV 2, as per Table 2.

**Table 2: Card Clock Frequency**

CLKDIV1	CLKDIV2	CLK
0	0	1/8 XTALIN
0	1	1/4 XTALIN
1	0	XTALIN
1	1	1/2 XTALIN

Card power down mode (card clock STOP) is supported and is controllable through the dedicated digital inputs CLKSTOP and CLKLEV (not supported in the 20QFN package).

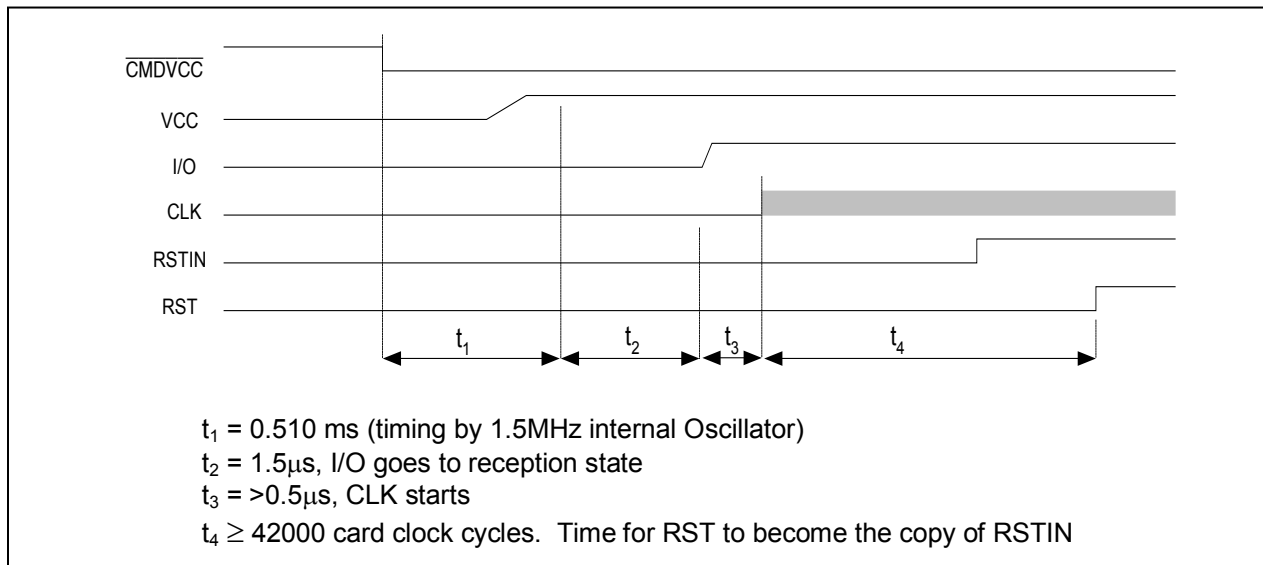


## 7 Activation Sequence

The 73S8024RN smart card interface IC has an internal 10ms delay at power on reset or on the application of  $V_{DD} > V_{DDF}$ . No activation is allowed at this time. The  $\overline{CMDVCC}$  (edge triggered) must then be set low to activate the card. In order to initiate activation, the card must be present; there can be no over-temperature fault or no  $V_{DD}$  fault.

The following steps show the activation sequence and the timing of the card control signals when the system controller sets  $\overline{CMDVCC}$  low while the  $RSTIN$  is low:

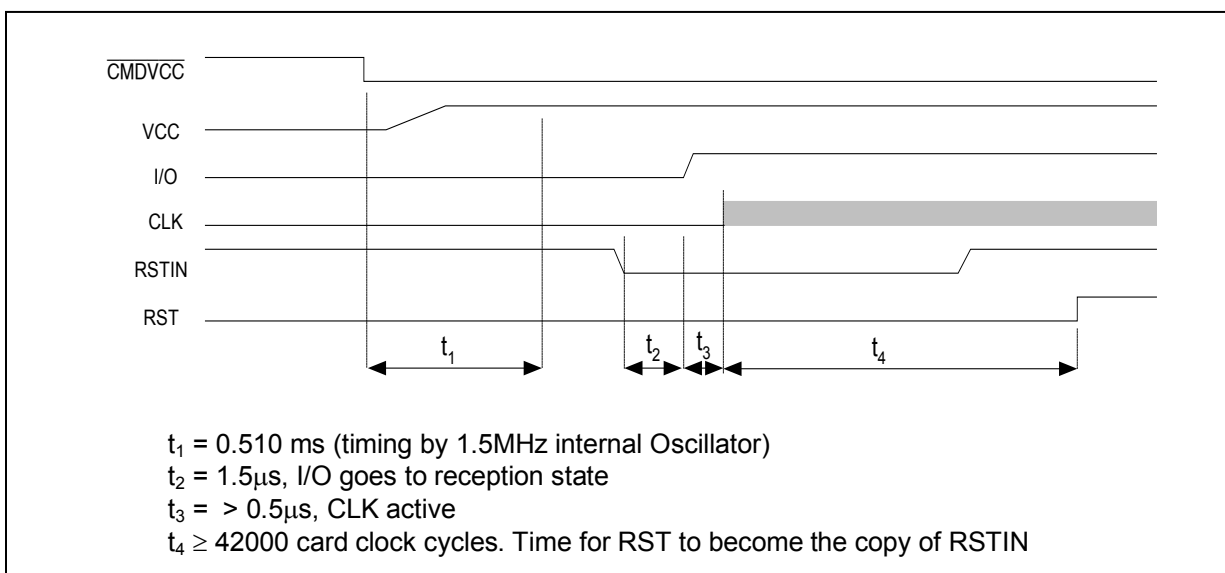
- $\overline{CMDVCC}$  is set low.
- Next, the internal  $V_{CC}$  control circuit checks the presence of  $V_{CC}$  at the end of  $t_1$ . In normal operation, the voltage  $V_{CC}$  to the card becomes valid during  $t_1$ . If  $V_{CC}$  does not become valid, the OFF goes low to report a fault to the system controller, and the power  $V_{CC}$  to the card is shut off.
- Turn I/O (AUX1, AUX2) to reception mode at the end of ( $t_2$ ).
- CLK is applied to the card at the end of ( $t_3$ ).
- RST is a copy of  $RSTIN$  after ( $t_4$ ).  $RSTIN$  may be set high before  $t_4$ , however the sequencer will not set RST high until 42000 clock cycles after the start of CLK.



**Figure 2: Activation Sequence – RSTIN Low When  $\overline{CMDVCC}$  Goes Low**

The following steps show the activation sequence and the timing of the card control signals when the system controller pulls the  $\overline{\text{CMDVCC}}$  low while the RSTIN is high:

- $\overline{\text{CMDVCC}}$  is set low.
- Next, the internal  $V_{\text{CC}}$  control circuit checks the presence of  $V_{\text{CC}}$  at the end of  $t_1$ . In normal operation, the voltage  $V_{\text{CC}}$  to the card becomes valid during this time. If not,  $\overline{\text{OFF}}$  goes low to report a fault to the system controller, and the power  $V_{\text{CC}}$  to the card is shut down.
- Due to the fall of RSTIN at ( $t_2$ ), turn I/O (AUX1, AUX2) to reception mode.
- CLK is applied to the card at the end of ( $t_3$ ), after I/O is in reception mode.
- RST is to be a copy of RSTIN after ( $t_4$ ). RSTIN may be set high before  $t_4$ , however the sequencer will not set RST high until 42000 clock cycles after the start of CLK.



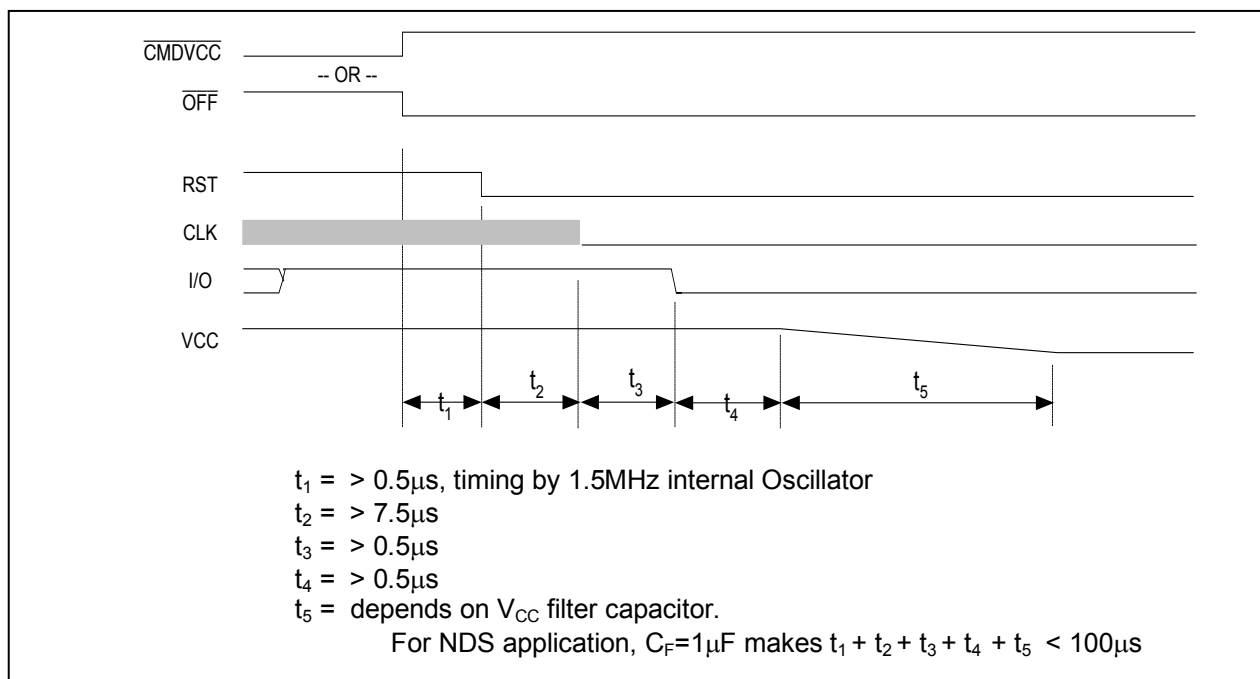
**Figure 3: Activation Sequence – RSTIN High When  $\overline{\text{CMDVCC}}$  Goes Low**

## 8 Deactivation Sequence

Deactivation is initiated either by the system controller by setting the  $\overline{\text{CMDVCC}}$  high, or automatically in the event of hardware faults. Hardware faults are over-current, overheating,  $V_{\text{DD}}$  fault,  $V_{\text{PC}}$  fault,  $V_{\text{CC}}$  fault, and card extraction during the session. To be noted that  $V_{\text{PC}}$  and  $V_{\text{CC}}$  faults are linked together so that a fault is generated when  $V_{\text{PC}}$  goes lower than  $V_{\text{CC}}$ .

The following steps show the deactivation sequence and the timing of the card control signals when the system controller sets the  $\overline{\text{CMDVCC}}$  high or  $\overline{\text{OFF}}$  goes low due to a fault or card removal:

- RST goes low at the end of  $t_1$ .
- CLK is set low at the end of  $t_2$ .
- I/O goes low at the end of  $t_3$ . Out of reception mode.
- $V_{\text{CC}}$  is shut down at the end of time  $t_4$ . After a delay  $t_5$  (discharge of the  $V_{\text{CC}}$  capacitor),  $V_{\text{CC}}$  is low.



**Figure 4: Deactivation Sequence**

## 9 $\overline{\text{OFF}}$ and Fault Detection

There are two different cases that the system controller can monitor the  $\overline{\text{OFF}}$  signal: to query regarding the card presence outside card sessions, or for fault detection during card sessions.

Outside a card session: In this condition,  $\overline{\text{CMDVCC}}$  is always high,  $\overline{\text{OFF}}$  is low if the card is not present, and high if the card is present. Because it is outside a card session, any fault detection will not act upon the  $\overline{\text{OFF}}$  signal. No deactivation is required during this time.

During a card session:  $\overline{\text{CMDVCC}}$  is always low, and  $\overline{\text{OFF}}$  falls low if the card is extracted or if any fault detection is detected. At the same time that  $\overline{\text{OFF}}$  is set low, the sequencer starts the deactivation process.

The Figure 5 shows the timing diagram for the signals  $\overline{\text{CMDVCC}}$ , PRES, and  $\overline{\text{OFF}}$  during a card session and outside the card session:

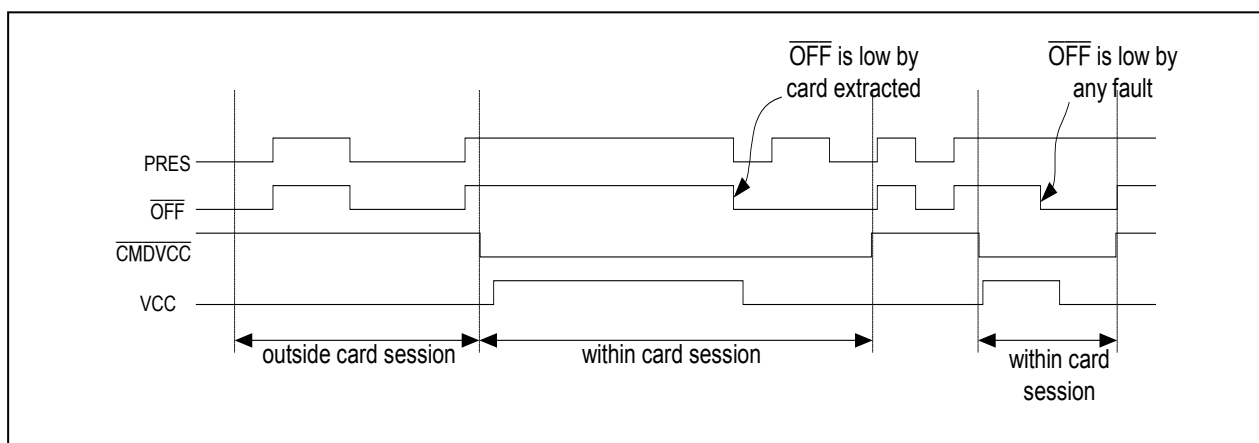


Figure 5: Timing Diagram – Management of the Interrupt Line  $\overline{\text{OFF}}$

## 10 I/O Circuitry and Timing

The states of the I/O, AUX1, and AUX2 pins are low after power on reset and they are in high when the activation sequencer turns on the I/O reception state. See the [Activation Sequence](#) section for more details on when the I/O reception is enabled. The states of I/OUC, AUX1UC, and AUX2UC are high after power on reset.

Within a card session and when the I/O reception state is turn on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected then both I/O lines return to their neutral state.

Figure 6 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output. The delay between the I/O signals is shown in Figure 7.

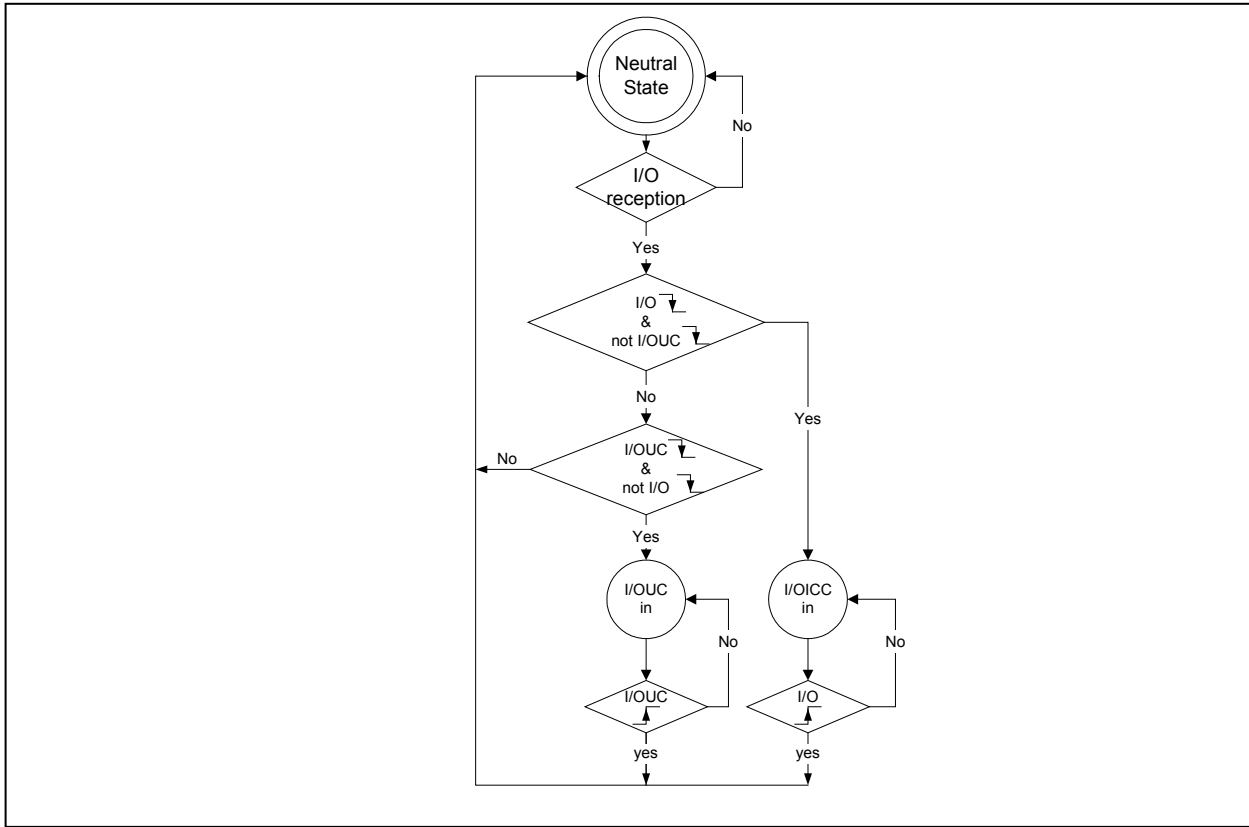


Figure 6: I/O and I/OUC State Diagram

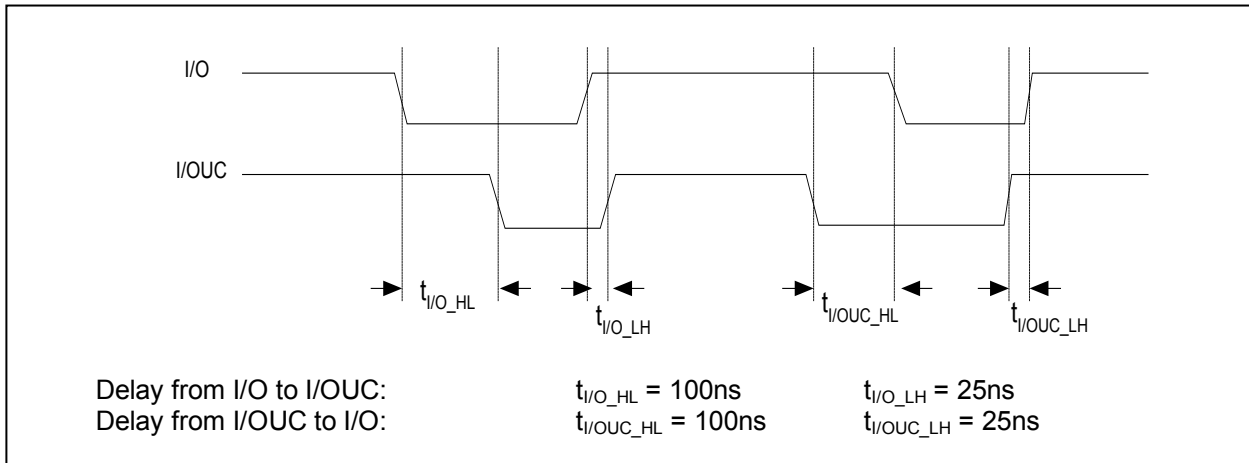


Figure 7: I/O - I/OUC Delays Timing Diagram



## 12 Electrical Specification

### 12.1 Absolute Maximum Ratings

Operation outside these rating limits may cause permanent damage to the device. The smart card interface pins are protected against short circuits to  $V_{CC}$ , ground, and each other.

Parameter	Rating
Supply Voltage $V_{DD}$	-0.5 to 6.0 VDC
Supply Voltage $V_{PC}$	-0.5 to 6.0 VDC
Input Voltage for Digital Inputs	-0.3 to ( $V_{DD} + 0.5$ ) VDC
Storage Temperature	-60 to 150°C
Pin Voltage (except card interface)	-0.3 to ( $V_{DD} + 0.5$ ) VDC
Pin Voltage (card interface)	-0.3 to ( $V_{CC} + 0.5$ ) VDC
ESD Tolerance – Card interface pins	+/- 6kV
ESD Tolerance – Other pins	+/- 2kV

\*Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.

Note: Smart Card pins are protected against shorts between any combinations of Smart Card pins.

### 12.2 Recommended Operating Conditions

Parameter	Rating
Supply Voltage $V_{DD}$	2.7 to 5.5 VDC
Supply Voltage $V_{PC}$	4.75 to 5.5 VDC
NDS Supply Voltage $V_{PC}$	4.85 to 5.5 VDC
Ambient Operating Temperature	-40°C to +85°C
Input Voltage for Digital Inputs	0V to $V_{DD} + 0.3V$

### 12.3 Package Thermal Parameters

Package	Rating
28 SO	44 °C / W
32QFN	47 °C / W (with bottom pad soldered)
32QFN	78 °C / W (without bottom pad soldered)
20QFN	53 °C / W (with the bottom pad soldered)
20QFN	90 °C / W (without the bottom pad soldered)

## 12.4 Smart Card Interface Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Card Power Supply (<math>V_{CC}</math>) Regulator</b>						
<b>General conditions, <math>-40^{\circ}\text{C} &lt; T &lt; 85^{\circ}\text{C}</math>, <math>4.75\text{v} &lt; V_{PC} &lt; 5.5\text{v}</math>, <math>2.7\text{v} &lt; V_{DD} &lt; 5.5\text{v}</math></b>						
<b>NDS conditions, <math>4.85\text{v} &lt; V_{PC} &lt; 5.5\text{v}</math></b>						
$V_{CC}$	Card supply voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode $I_{CC} = 1\text{mA}$	-0.1		0.4	V
		Active mode; $I_{CC} < 65\text{mA}$ ; 5v	4.60		5.25	V
		Active mode; $I_{CC} < 65\text{mA}$ ; 5v, NDS condition	4.75		5.25	V
		Active mode; $I_{CC} < 90\text{mA}$ ; 5v	4.55		5.25	V
		Active mode; $I_{CC} < 90\text{mA}$ ; 3v	2.80		3.2	V
		Active mode; single pulse of 100mA for 2 $\mu\text{s}$ ; 5 volt, fixed load = 25mA	4.6		5.25	V
		Active mode; single pulse of 100mA for 2 $\mu\text{s}$ ; 3v, fixed load = 25mA	2.76		3.2	V
		Active mode; current pulses of 40nAs with peak $ I_{CC}  < 200\text{mA}$ , $t < 400\text{ns}$ ; 5v	4.6		5.25	V
		Active mode; current pulses of 40nAs with peak $ I_{CC}  < 200\text{mA}$ , $t < 400\text{ns}$ ; 5v, NDS condition	4.65		5.25	V
		Active mode; current pulses of 40nAs with peak $ I_{CC}  < 200\text{mA}$ , $t < 400\text{ns}$ ; 3v	2.76		3.2	V
$V_{CCrip}$	$V_{CC}$ Ripple	$f_{RIPPLE} = 20\text{K} - 200\text{MHz}$			350	mV
$I_{CCmax}$	Card supply output current	Static load current, $V_{CC} > 4.6$	65			mA
		Static load current, $V_{CC} > 4.55$ or 2.7 volts as selected	90			mA
$I_{CCF}$	$I_{CC}$ fault current		90		150	mA
$V_{SR} - V_{SF}$	$V_{CC}$ slew rate -	$C_F = 3.3\mu\text{F}$ on $V_{CC}$	0.02	0.050	0.08	V/ $\mu\text{s}$
$V_{SRN} - V_{SFN}$	$V_{CC}$ slew rate	$C_F = 1.0\mu\text{F}$ on $V_{CC}$ NDS applications	0.06	0.160	0.26	V/ $\mu\text{s}$
$C_F$	External filter capacitor ( $V_{CC}$ to GND)	$C_F$ should be ceramic with low ESR ( $< 100\text{m}\Omega$ ).	1	3.3	5	$\mu\text{F}$
$C_{FNDS}$	External filter capacitor ( $V_{CC}$ to GND)	NDS applications $C_F$ should be ceramic with low ESR ( $< 100\text{m}\Omega$ ).	0.5	1.0	1.5	$\mu\text{F}$



Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC.</b>						
<b>I<sub>SHORTL</sub>, I<sub>SHORTH</sub>, and V<sub>INACT</sub> requirements do not pertain to I/OUC, AUX1UC, and AUX2UC.</b>						
V <sub>OH</sub>	Output level, high (I/O, AUX1, AUX2)	I <sub>OH</sub> = 0	0.9 V <sub>CC</sub>		V <sub>CC</sub> +0.1	V
		I <sub>OH</sub> = -40μA	0.75 V <sub>CC</sub>		V <sub>CC</sub> +0.1	V
V <sub>OH</sub>	Output level, high (I/OUC, AUX1UC, AUX2UC)	I <sub>OH</sub> = 0	0.9 V <sub>DD</sub>		V <sub>DD</sub> +0.1	V
		I <sub>OH</sub> = -40μA	0.75 V <sub>DD</sub>		V <sub>DD</sub> +0.1	V
V <sub>OL</sub>	Output level, low	I <sub>OL</sub> =1mA			0.3	V
V <sub>IH</sub>	Input level, high (I/O, AUX1, AUX2)		1.8		V <sub>CC</sub> +0.30	V
V <sub>IH</sub>	Input level, high (I/OUC, AUX1UC, AUX2UC)		1.8		V <sub>DD</sub> +0.30	V
V <sub>IL</sub>	Input level, low		-0.3		0.8	V
V <sub>INACT</sub>	Output voltage when outside of session	I <sub>OL</sub> = 0			0.1	V
		I <sub>OL</sub> = 1mA			0.3	V
I <sub>LEAK</sub>	Input leakage	V <sub>IH</sub> = V <sub>CC</sub>			10	μA
I <sub>IL</sub>	Input current, low	V <sub>IL</sub> = 0			0.65	mA
I <sub>SHORTL</sub>	Short circuit output current	For output low, shorted to V <sub>CC</sub> through 33 ohms			15	mA
I <sub>SHORTH</sub>	Short circuit output current	For output high, shorted to ground through 33 ohms			15	mA
t <sub>R</sub> , t <sub>F</sub>	Output rise time, fall times	For I/O, AUX1, AUX2, C <sub>L</sub> = 80pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, C <sub>L</sub> =50Pf, 10% to 90%.			100	ns
t <sub>IR</sub> , t <sub>IF</sub>	Input rise, fall times				1	μs
R <sub>PU</sub>	Internal pull-up resistor	Output stable for >200ns	8	11	14	kΩ
FD <sub>MAX</sub>	Maximum data rate				1	MHz
T <sub>FDIO</sub>	Delay, I/O to I/OUC, AUX1 to AUX1UC, AUX2 to AUX2UC, I/OUC to I/O, AUX1UC to AUX1, AUX2UC to AUX2 (respectively falling edge to falling edge and rising edge to rising edge)	Edge from master to slave, measured at 50%	60	100	200	ns
T <sub>RDIO</sub>				25	90	ns
C <sub>IN</sub>	Input capacitance				10	pF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Reset and Clock for card interface, RST, CLK</b>						
V <sub>OH</sub>	Output level, high	I <sub>OH</sub> = -200μA	0.9 V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>OL</sub>	Output level, low	I <sub>OL</sub> = 200μA	0		0.3	V
V <sub>INACT</sub>	Output voltage when outside of session	I <sub>OL</sub> = 0			0.1	V
		I <sub>OL</sub> = 1mA			0.3	V
I <sub>RST_LIM</sub>	Output current limit, RST				30	mA
I <sub>CLK_LIM</sub>	Output current limit, CLK				70	mA
CLK <sub>SR3V</sub>	CLK slew rate	V <sub>CC</sub> = 3V	0.3			V/ns
CLK <sub>SR5V</sub>	CLK slew rate	V <sub>CC</sub> = 5V	0.5			V/ns
t <sub>R</sub> , t <sub>F</sub>	Output rise time, fall time	C <sub>L</sub> = 35pF for CLK, 10% to 90%			8	ns
		C <sub>L</sub> = 200pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK	C <sub>L</sub> = 35pF, F <sub>CLK</sub> ≤ 20MHz	45		55	%

## 12.5 Characteristics: Digital Signals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Digital I/O Except for OSC I/O</b>						
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage		0.7 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2mA			0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	V <sub>DD</sub> - 0.45			V
R <sub>OUT</sub>	Pull-up resistor, $\overline{\text{OFF}}$		16	21	24	kΩ
I <sub>IL1</sub>	Input Leakage Current	GND < V <sub>IN</sub> < V <sub>DD</sub>	-5		5	μA
<b>Oscillator (XTALIN) I/O Parameters</b>						
V <sub>ILXTAL</sub>	Input Low Voltage - XTALIN		-0.3		0.3 V <sub>DD</sub>	V
V <sub>IHXTAL</sub>	Input High Voltage - XTALIN		0.7 V <sub>DD</sub>		V <sub>DD</sub> +0.3	V
I <sub>ILXTAL</sub>	Input Current - XTALIN	GND < V <sub>IN</sub> < V <sub>DD</sub>	-30		30	μA
f <sub>MAX</sub>	Max freq. Osc or external clock				27	MHz
δ <sub>in</sub>	External input duty cycle limit	t <sub>R/F</sub> < 10% f <sub>IN</sub> , 45% < δ <sub>CLK</sub> < 55%	48		52	%

## 12.6 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD}$	Supply Current			2.7	7.0	mA
$I_{PC}$	Supply Current	$V_{CC}$ on, ICC=0 I/O, AUX1, AUX2=high, Clock not toggling		450	650	$\mu$ A
$I_{PCOFF}$	$V_{PC}$ supply current when $V_{CC} = 0$	$\overline{CMDVCC}$ High		345	550	$\mu$ A

## 12.7 Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DDF}$	$V_{DD}$ fault ( $V_{DD}$ Voltage supervisor threshold)	No external resistor on VDDF_ADJ pin	2.15		2.4	V
$V_{PCF}$	$V_{PC}$ fault ( $V_{PC}$ Voltage supervisor threshold)	$V_{PC} < V_{CC}$ , a transient event		$V_{CC} - 0.2$		V
$V_{CCF}$	$V_{CC}$ fault ( $V_{CC}$ Voltage supervisor threshold)	$V_{CC} = 5v$	4.20		4.55	V
		$V_{CC} = 3v$	2.5		2.7	V
$T_F$	Die over temperature fault		115		145	$^{\circ}$ C

### 13 Mechanical Drawing (20QFN)

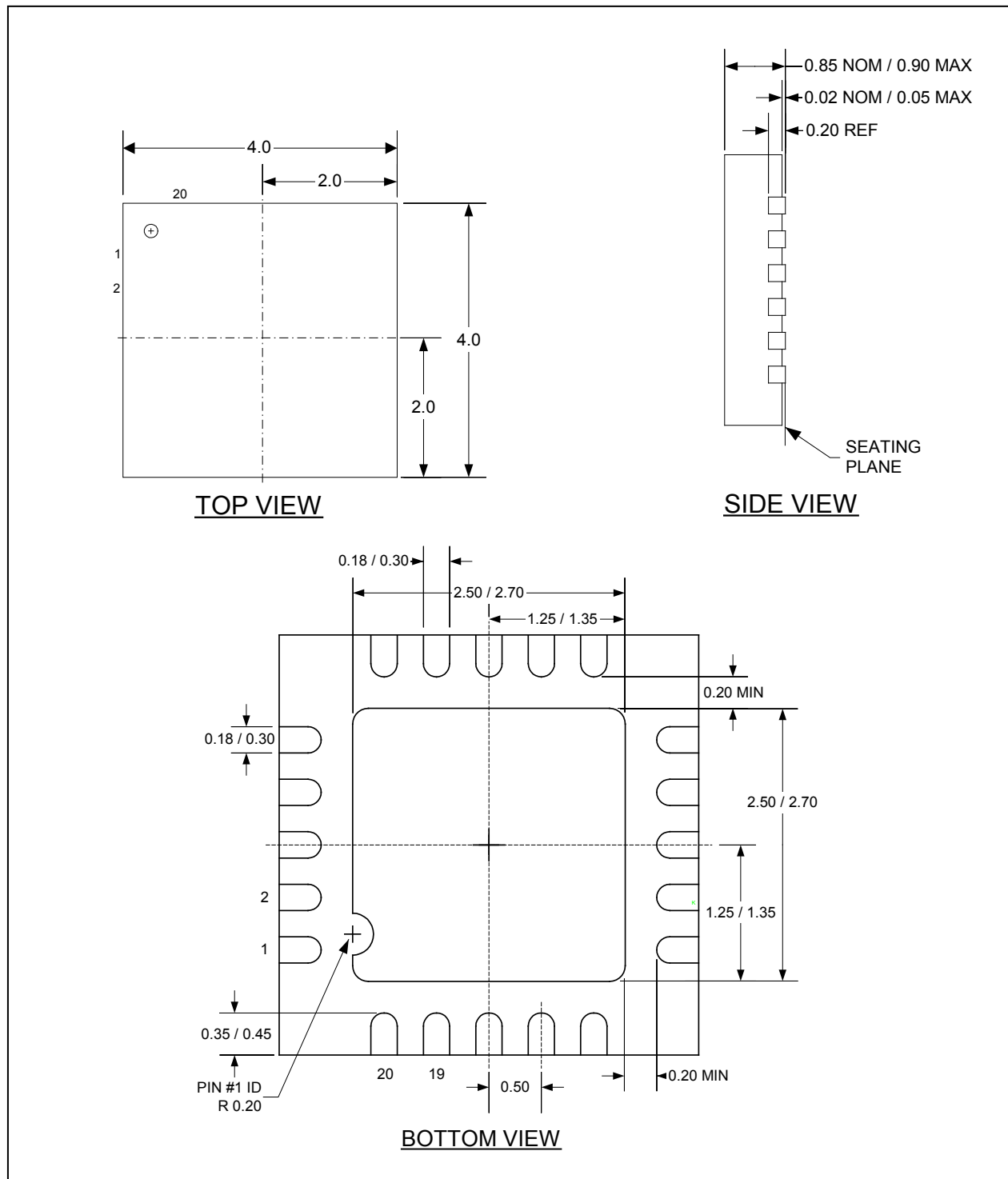


Figure 9: 20QFN Mechanical Drawing

### 14 Package Pin Designation (20QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

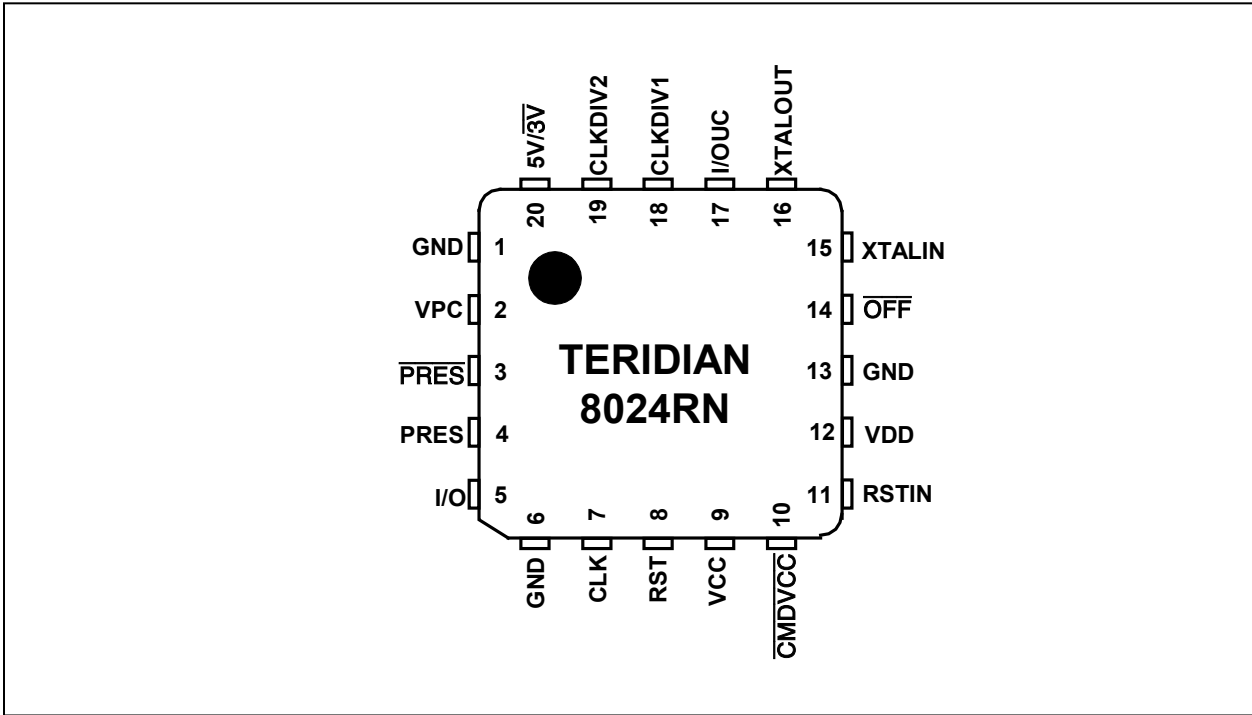


Figure 10: 20QFN Pin Out

### 15 Mechanical Drawing (32QFN)

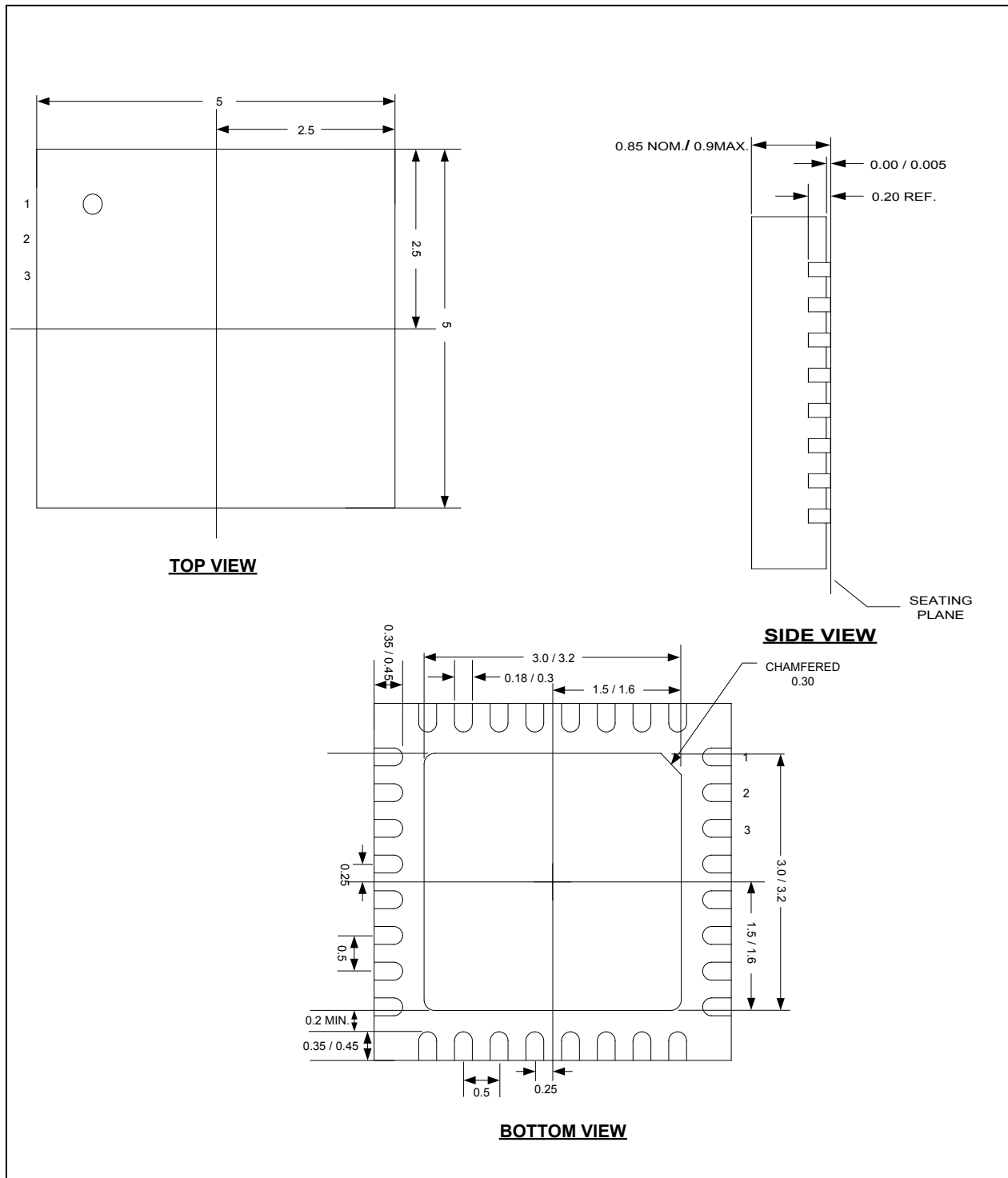


Figure 11: 32QFN Mechanical Drawing

### 16 Package Pin Designation (32QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

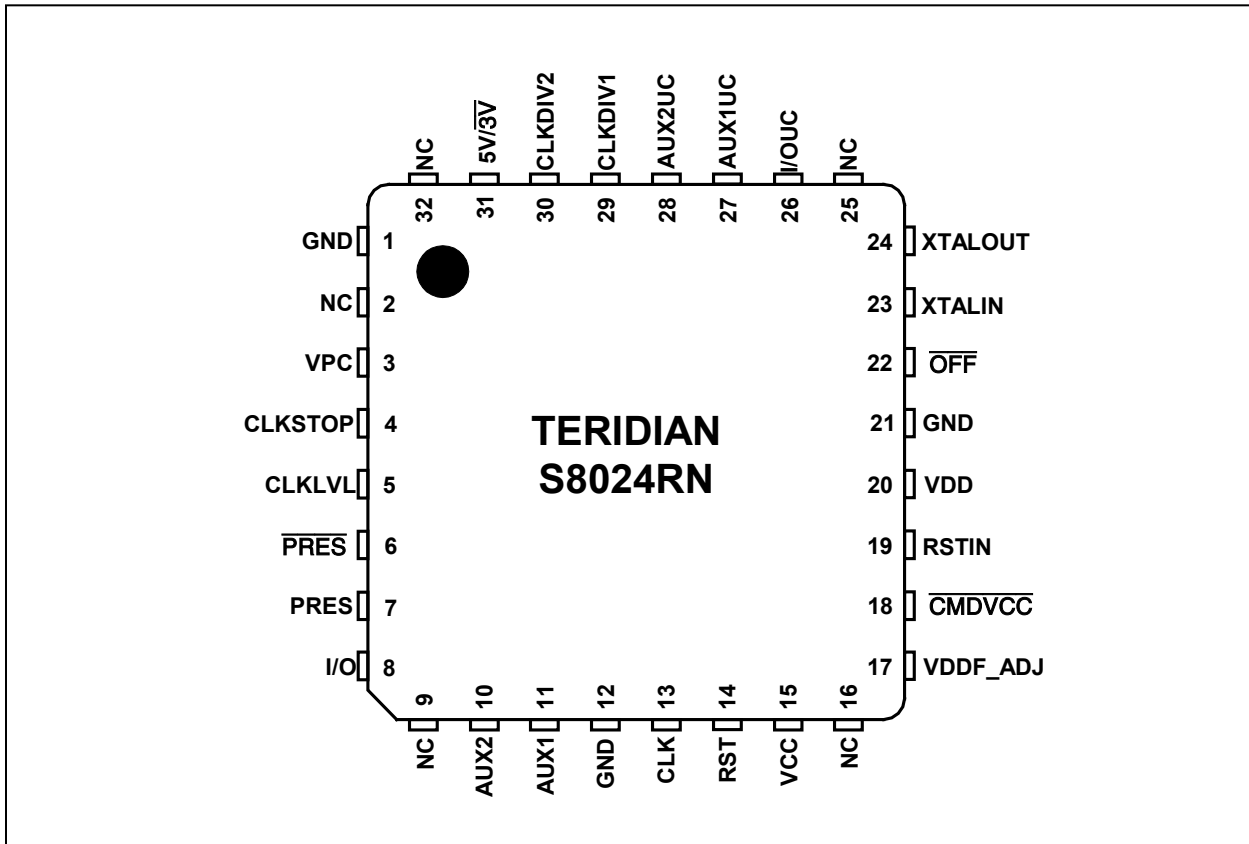


Figure 12: 32QFN Pin Out

### 17 Mechanical Drawing (SO)

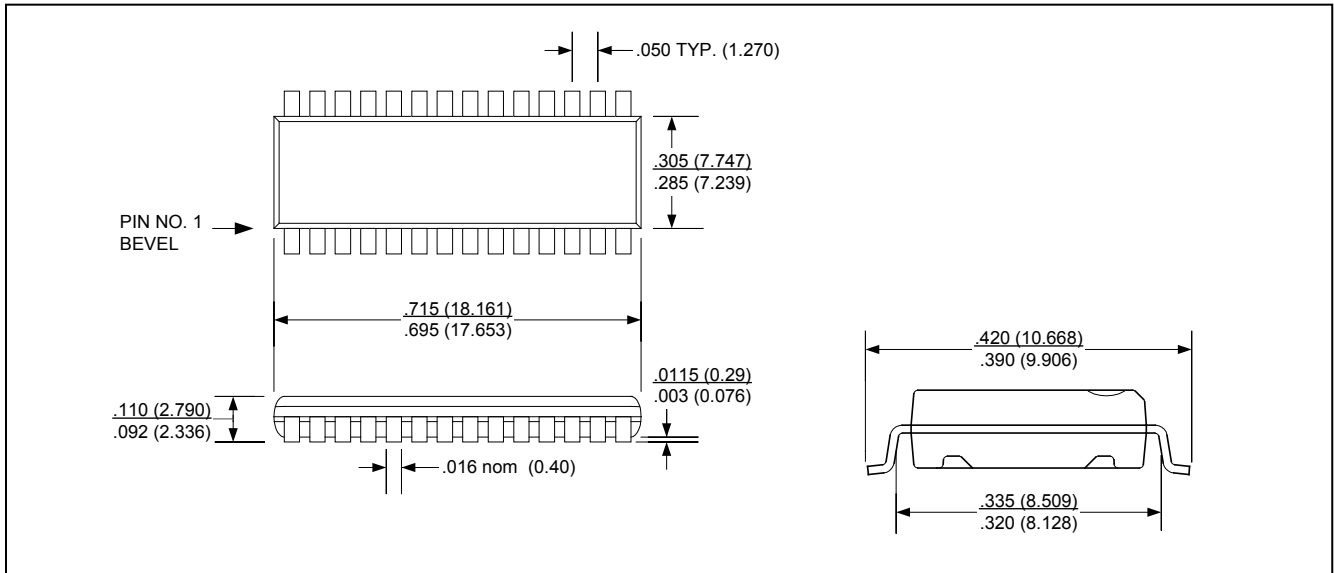


Figure 13: 28 Lead SO

### 18 Package Pin Designation (SO)

CAUTION: Use handling procedures necessary for a static sensitive component

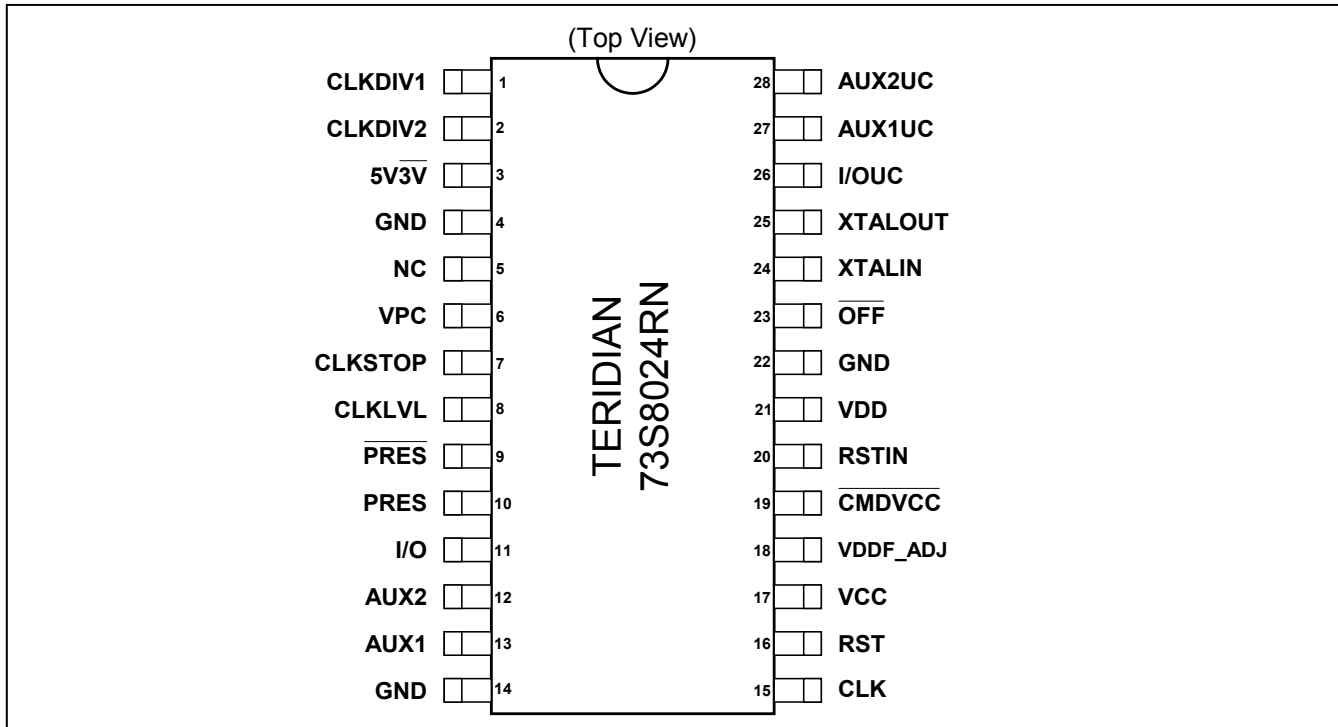


Figure 14: 28SO 73S8024RN Pin Out



## 19 Ordering Information

Part Description	Order No.	Packaging Mark
73S8024RN-SOL 28-pin Lead-Free SO	73S8024RN-IL/F	73S8024RN-IL
73S8024RN-SOL 28-pin Lead-Free SO Tape / Reel	73S8024RN-ILR/F	73S8024RN-IL
73S8024RN-32QFN 32-pin Lead-Free QFN	73S8024RN-IM/F	S8024RN
73S8024RN-32QFN 32-pin Lead-Free QFN Tape / Reel	73S8024RN-IMR/F	S8024RN
73S8024RN-20QFN 20-pin Lead-Free QFN	73S8024RN-20IM/F	8024RN
73S8024RN-20QFN 20-pin Lead-Free QFN Tape / Reel	73S8024RN-20IMR/F	8024RN

## 20 Related Documentation

The following 73S8024RN documents are available from Maxim:

*73S8024RN Data Sheet (this document)*  
*73S8024RN Combination 28SO/20QFN Demo Board User Guide*  
*73S8024RN 28SO Demo Board User's Guide*  
*Achieving EMV Electrical Compliance with the TERIDIAN 73S8024RN*  
*Dual Footprint Layout*  
*73S8024RN vs NXP TDA8024T*  
*Implementing the TERIDIAN 73S8024RN in NDS Applications*

## 21 Contact Information

For more information about Maxim products or to check the availability of the 73S8024RN, contact technical support at [www.maxim-ic.com/support](http://www.maxim-ic.com/support).

## Revision History

Revision	Date	Description
1.1	5/18/2004	First publication.
1.2	11/5/2004	
1.3	4/27/2005	Added 20QFN package option and ordering information. Updated 32 QFN ordering information.
1.4	7/15/2005	
1.5	8/23/2005	
1.6	12/5/2007	Removes leaded package options, replaces 32QFN punched with SAWN mechanical dimensions, update 28SO package dimensions.
1.7	1/17/2008	Changed dimension of bottom exposed pad on 32QFN mechanical package figure.
1.8	1/19/2009	In <a href="#">Figure 1</a> , modified the device block diagram to make pin 2 a no connect. Also, changed the pin description. In <a href="#">Figure 9</a> , changed the mechanical drawing for the 20QFN package. Added the NDS logo to <a href="#">page 1</a> and assigned document number. Added the Related Documentation and the Contact Information sections.
1.9	5/27/2010	Changed dimension of bottom exposed pad on 32QFN mechanical package figure.
2	6/12	Corrected the Order Numbers for the 73S8024RN-32QFN. Added Maxim logo and Contact Information.

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[73S8024RN-32IMR/F](#)