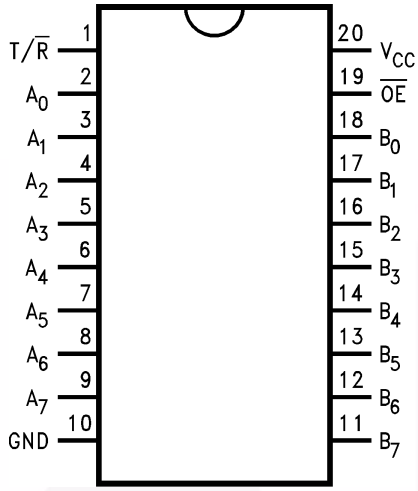
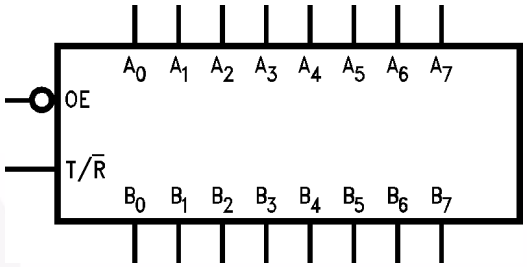
Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

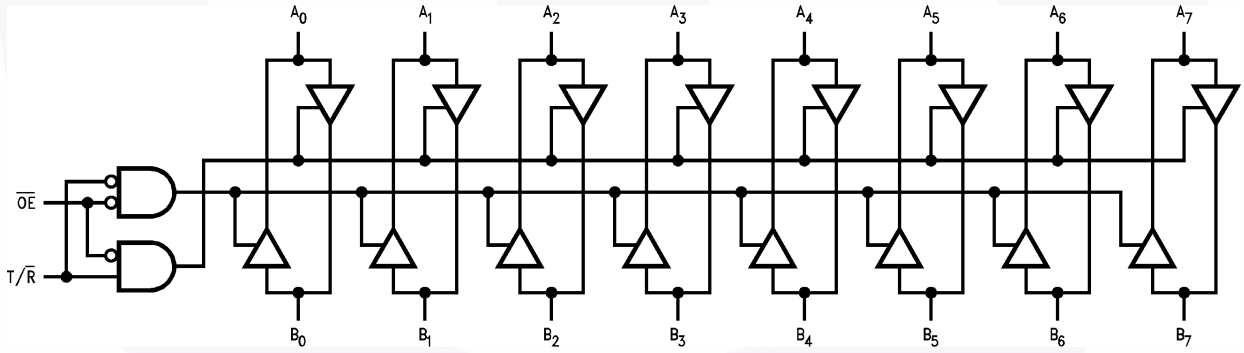
Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–55°C to +125°C
T_J	Junction Temperature Under Bias	–55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
V_{IN}	Input Voltage(1)	–0.5V to +7.0V
I_{IN}	Input Current(1)	–30mA to +5.0mA
V_O	Voltage Applied to Any Output Disabled or Power-off State HIGH State	 –0.5V to 5.5V –0.5V to V_{CC}
	Current Applied to Output in LOW State	twice the rated I_{OL} (mA)
	DC Latchup Source Current	–500mA
	Over Voltage Latchup (I/O)	10V

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	–40°C to +85°C
V_{CC}	Supply Voltage	+4.5V to +5.5V
$\Delta V / \Delta t$	Minimum Input Edge Rate Data Input Enable Input	 50mV/ns 20mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage			Recognized HIGH Signal	2.0			V
V_{IL}	Input LOW Voltage			Recognized LOW Signal			0.8	V
V_{CD}	Input Clamp Diode Voltage		Min.	I_{IN} = –18 mA ($\overline{OE}$, T/$\overline{R}$)			–1.2	V
V_{OH}	Output HIGH Voltage		Min.	I_{OH} = –3 mA (A_n, B_n)	2.5			V
			Min.	I_{OH} = –32 mA (A_n, B_n)	2.0			
V_{OL}	Output LOW Voltage		Min.	I_{OL} = 64 mA (A_n, B_n)			0.55	V
I_{IH}	Input HIGH Current		Max.	V_{IN} = 2.7V ($\overline{OE}$, T/$\overline{R}$)			1	µA
				V_{IN} = V_{CC} ($\overline{OE}$, T/$\overline{R}$)			1	
I_{BVI}	Input HIGH Current Breakdown Test		Max.	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)			7	µA
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max.	V_{IN} = 5.5V (A_n, B_n)			100	µA
I_{IL}	Input LOW Current		Max.	V_{IN} = 0.5V ($\overline{OE}$, T/$\overline{R}$)			–1	µA
				V_{IN} = 0.0V ($\overline{OE}$, T/$\overline{R}$)			–1	
V_{ID}	Input Leakage Test		0.0	I_{ID} = 1.9 µA ($\overline{OE}$, T/$\overline{R}$), All Other Pins Grounded	4.75			V
I_{IH} + I_{OZH}	Output Leakage Current		0–5.5V	V_{OUT} = 2.7V (A_n, B_n), $\overline{OE}$ = 2.0V			10	µA
I_{IL} + I_{OZL}	Output Leakage Current		0–5.5V	V_{OUT} = 0.5V (A_n, B_n), $\overline{OE}$ = 2.0V			–10	µA
I_{OS}	Output Short-Circuit Current		Max.	V_{OUT} = 0.0V (A_n, B_n)	–100		–275	mA
I_{CEX}	Output HIGH Leakage Current		Max.	V_{OUT} = V_{CC} (A_n, B_n)			50	µA
I_{ZZ}	Bus Drainage Test		0.0	V_{OUT} = 5.5V (A_n, B_n), All Others GND			100	µA
I_{CCH}	Power Supply Current		Max.	All Outputs HIGH			50	µA
I_{CCL}	Power Supply Current		Max.	All Outputs LOW			30	mA
I_{CCZ}	Power Supply Current		Max.	$\overline{OE}$ = V_{CC}, T/$\overline{R}$ = GND or V_{CC}, All Other GND or V_{CC}			50	µA
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled	Max.	V_I = V_{CC} – 2.1V			2.5	mA
		Outputs 3-STATE		$\overline{OE}$, T/$\overline{R}$ V_I = V_{CC} – 2.1V			2.5	mA
		Outputs 3-STATE		Data Input V_I = V_{CC} – 2.1V, All Others at V_{CC} or GND.			50	µA
I_{CCD}	Dynamic I_{CC} No Load		Max.	Outputs Open, $\overline{OE}$ = GND, T/$\overline{R}$ = GND or V_{CC}, One Bit Toggling, 50% Duty Cycle			0.1	mA/ MHz

DC Electrical Characteristics

SOIC package.

Symbol	Parameter	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω	Min.	Typ.	Max.	Units
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	T_A = 25°C[2]		0.7	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	T_A = 25°C[2]	–1.3	–1.0		V
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	5.0	T_A = 25°C[4]	2.7	3.1		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	T_A = 25°C[3]	2.0	1.7		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	T_A = 25°C[3]		0.9	0.6	V

Notes:

2. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.
3. Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.
4. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

SOIC and SSOP package.

Symbol	Parameter	T_A = +25°C, V_{CC} = +5V, C_L = 50pF			T_A = –55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF		T_A = –40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Outputs	1.0	2.1	3.6	1.0	4.8	1.0	3.6	ns
t_{PHL}		1.0	2.4	3.6	1.0	4.8	1.0	3.6	
t_{PZH}	Output Enable Time	1.5	3.2	6.0	1.0	6.7	1.5	6.0	ns
t_{PZL}		1.5	3.7	6.0	2.0	7.5	1.5	6.0	
t_{PHZ}	Output Disable Time	1.0	3.6	6.1	1.7	7.4	1.0	6.1	ns
t_{PLZ}		1.0	3.3	5.6	1.7	6.5	1.0	5.6	

Extended AC Electrical Characteristics

SOIC package.

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$, 8 Outputs Switching[5]			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$, 1 Output Switching[6]		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$, 8 Outputs Switching[7]		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{TOGGLE}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns
t_{PHL}	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5	
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	9.5	ns
t_{PZL}		1.5		6.5	2.5	7.5	2.5	11.0	
t_{PHZ}	Output Disable Time	1.0		6.5		[8]		[8]	ns
t_{PLZ}		1.0		5.6					

Notes:

5. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
6. This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load. This specification pertains to single output switching only.
7. This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
8. The 3-STATE delays are dominated by the RC network (500Ω, 250pF) on the output and have been excluded from the datasheet.

Skew

SOIC package.

Symbol	Parameter	T_A = –40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF, 8 Outputs Switching[11]	T_A = –40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 250pF, 8 Outputs Switching[12]	Units
		Max.	Max.	
t_{OSHL}[9]	Pin to Pin Skew, HL Transitions	1.3	2.3	ns
t_{OSLH}[9]	Pin to Pin Skew, LH Transitions	1.0	1.8	ns
t_{PS}[13]	Duty Cycle, LH–HL Skew	2.0	3.5	ns
t_{OST}[9]	Pin to Pin Skew, LH/HL Transitions	2.0	3.5	ns
t_{PV}[10]	Device to Device Skew, LH/HL Transitions	2.0	3.5	ns

Notes:

9. Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.
10. Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.
11. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)
12. These specifications guaranteed but not tested. The limits represent propagation delays with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
13. This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

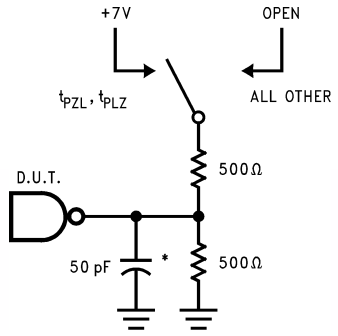
Capacitance

Symbol	Parameter	Conditions T_A = 25°C	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 0V ($\overline{OE}$, T/$\overline{R}$)	5.0	pF
$C_{I/O}$[14]	I/O Capacitance	V_{CC} = 5.0V (A_n, B_n)	11.0	pF

Note:

14. $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

Figure 1. Standard AC Test Load

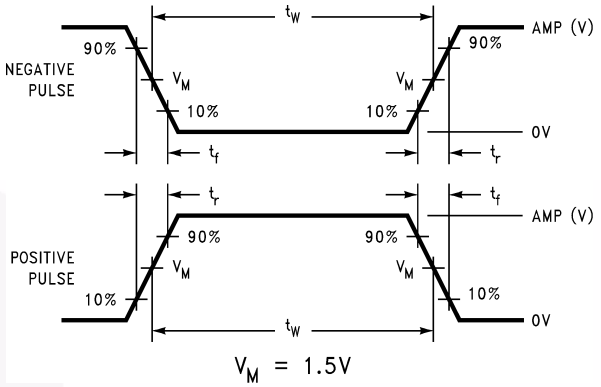


Figure 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1MHz	500ns	2.5ns	2.5ns

Figure 3. Test Input Signal Requirements

AC Waveforms

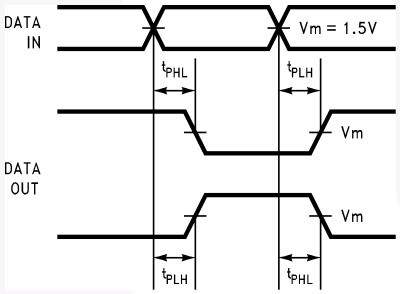


Figure 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

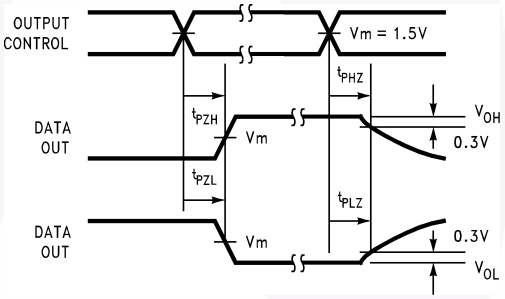


Figure 6. 3-STATE Output HIGH and LOW Enable and Disable Times

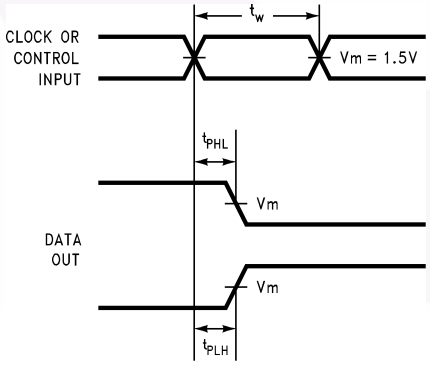


Figure 5. Propagation Delay, Pulse Width Waveforms

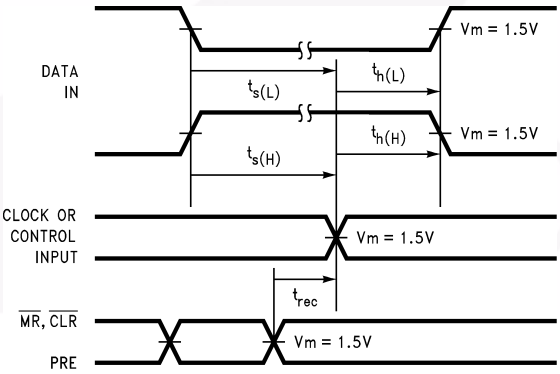


Figure 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions

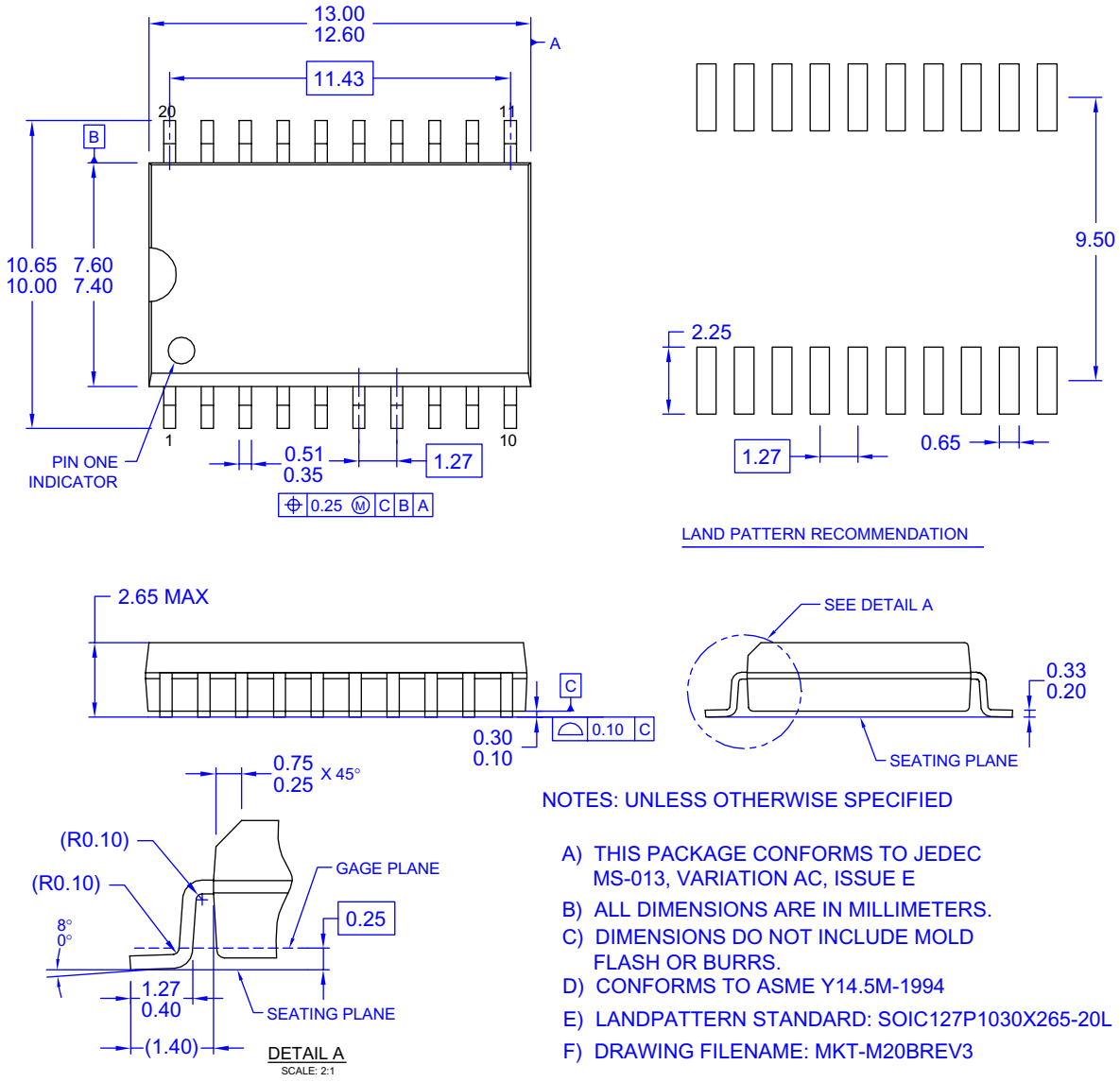


Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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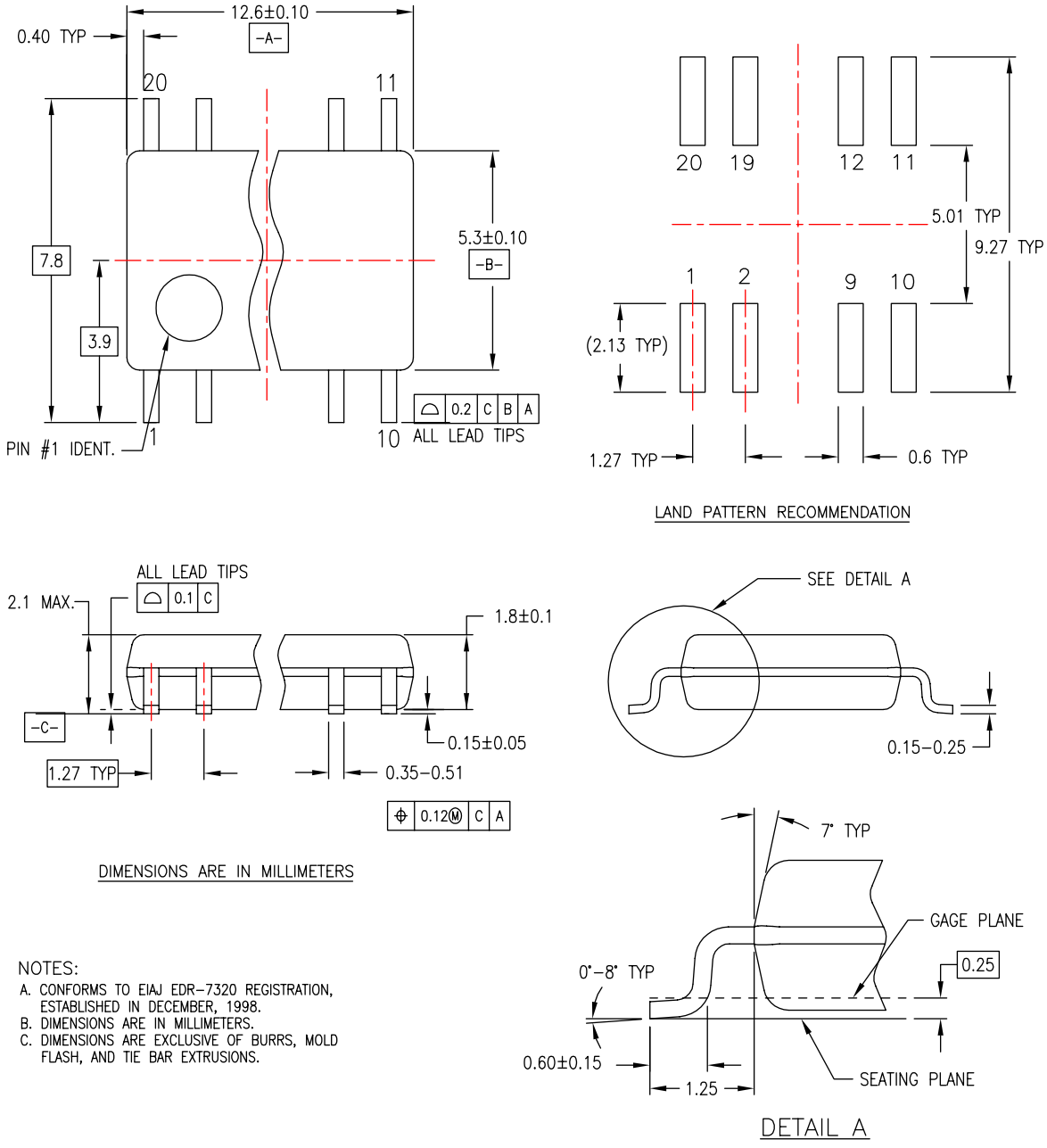
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
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M20DREVC

Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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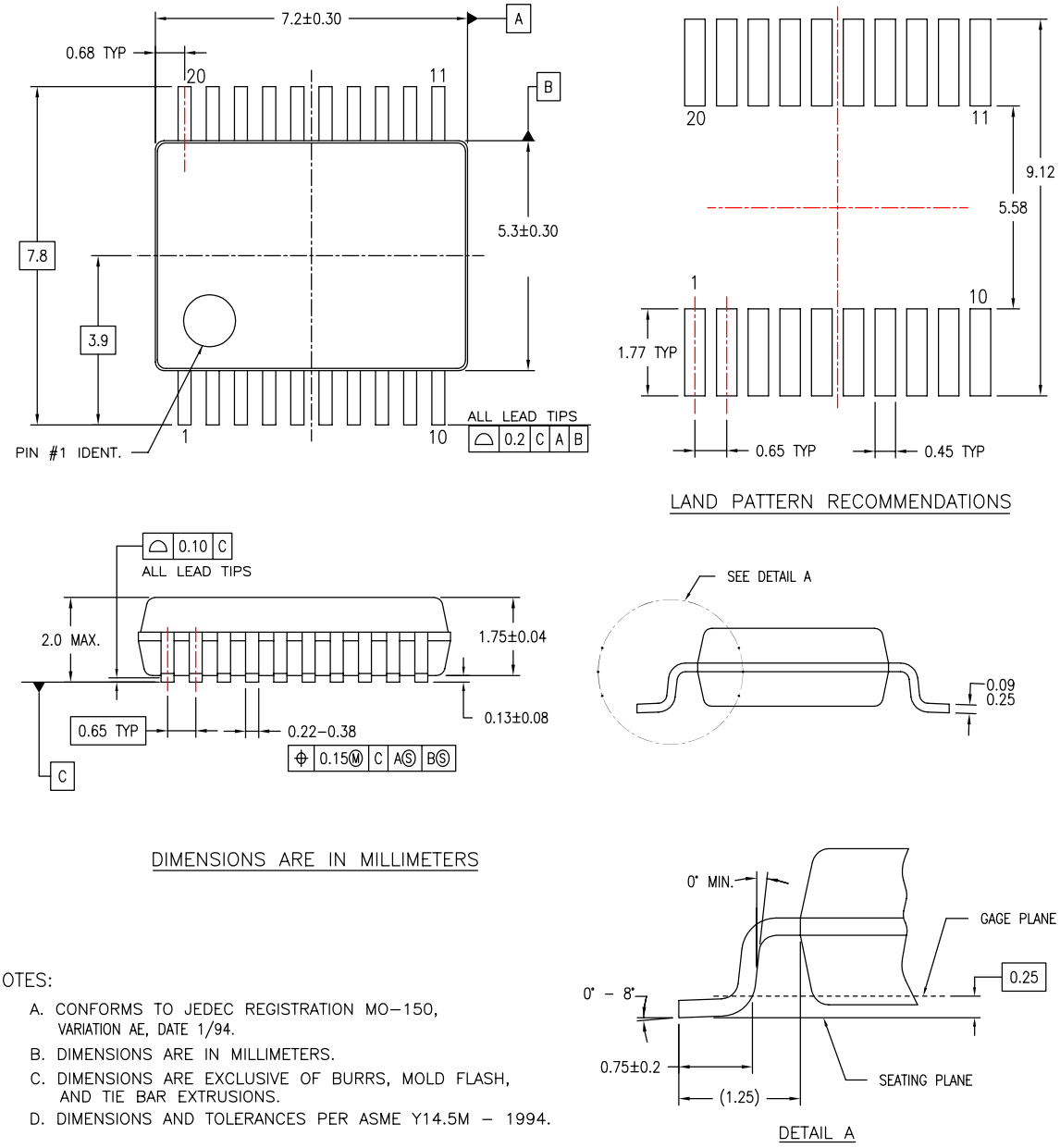
Physical Dimensions (Continued)



NOTES:

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D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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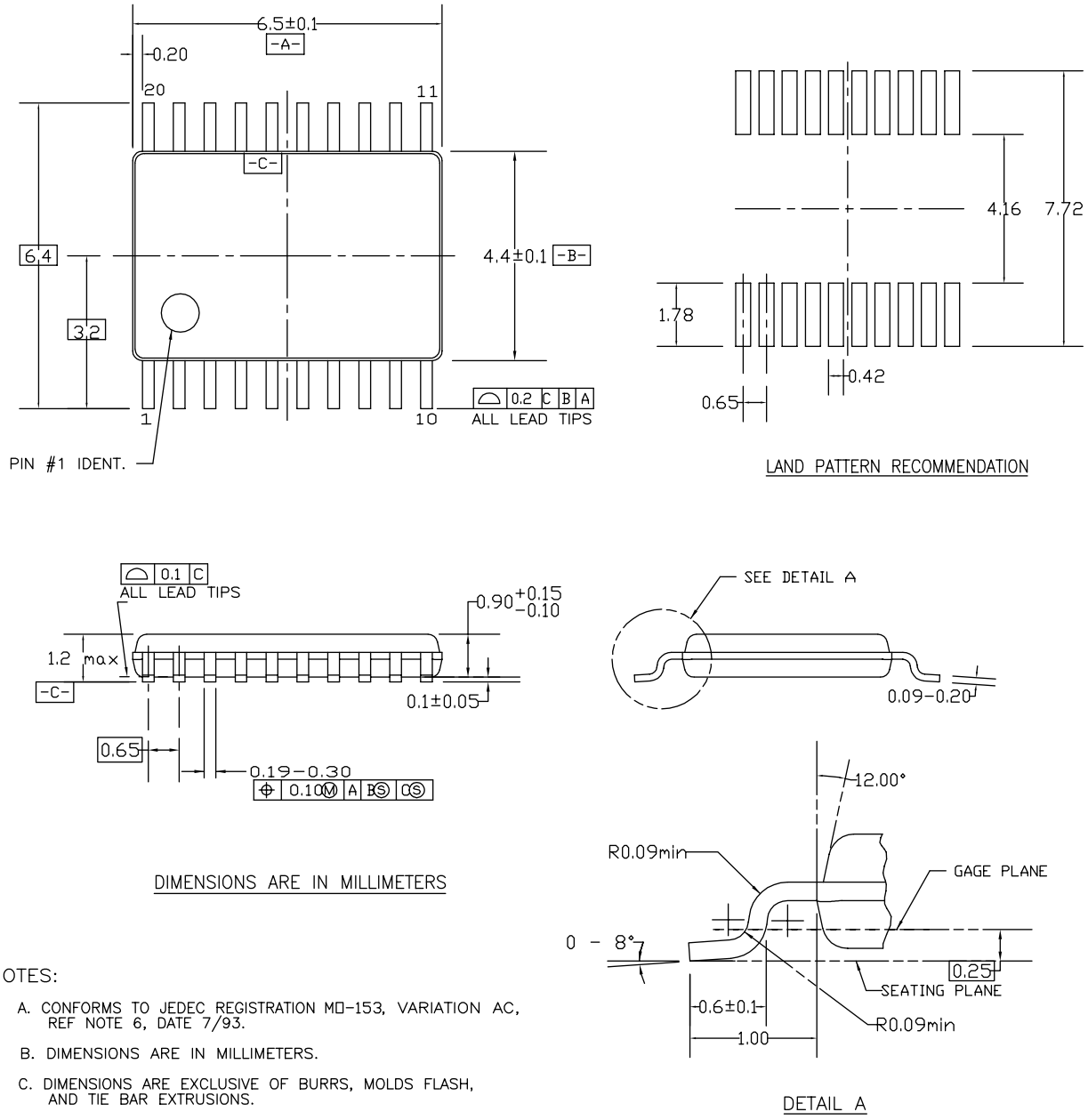
Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

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D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 11. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Rev. I32

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