Electrical specification

		Capacitance value					
		10	**15**	**22**	**33**	**47**	**68**
Unit	**1 pF**	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
	10 pF	**100 pF: 935.131.424.310**	**150 pF: 935.131.424.315**	**220 pF: 935.131.424.322**	**330 pF: 935.131.424.333**	**470 pF: 935.131.424.347**	**680 pF: 935.131.424.368**
	0.1 nF	**1 nF: 935.131.424.410**	**1.5 nF: 935.131.424.415**	**2.2 nF: 935.131.424.422**	**3.3 nF: 935.131.424.433**	**4.7 nF: 935.131.424.447**	**6.8 nF: 935.131.424.468**
	1 nF	**10 nF: 935.131.424.510**	**15 nF: 935.131.424.515**	**22 nF: 935.131.424.522**	**33 nF: 935.131.424.533**	**47 nF: 935.131.424.547 935.131.724.547**	*Contact IPDIA Sales*
	10 nF	**100 nF: 935.131.424.610**					

(*) Thinner thickness (as low as 100 µm thick) available, see Low Profile Silicon Capacitor product: LPSC

(**) Extended temperature range (up to +250 °C) available, see Xtreme Temperature Silicon Capacitor product: XTSC

(***) Other values on request.

Parameters	Value
Capacitance range	*100 pF to 100 nF*$^{(***)}$
Capacitance tolerances	*±15 %*$^{(***)}$
Operating temperature range	*-55 °C to 150 °C* $^{(**)}$
Storage temperatures	*- 70 °C to 165 °C*
Temperature coefficient	*<±0.5 %, from -55 °C to +150 °C*
Breakdown voltage (BV)	*11, 30 V*$^{(***)}$
Capacitance variation versus RVDC	*0.1 % /V (from 0 V to RVDC)*
Equivalent Serial Inductor (ESL)	*Max 100 pH*
Equivalent Serial Resistor (ESR)	*Max 400mΩ*$^{(***)}$
Insulation resistance	*100GΩ min @ 3V,from -55°C to +150°C*
Ageing	*Negligible, < 0.001 % / 1000h*
Reliability	*FIT<0.017 parts / billion hours,*
Capacitor height	*Max 400 µm* $^{(*)}$

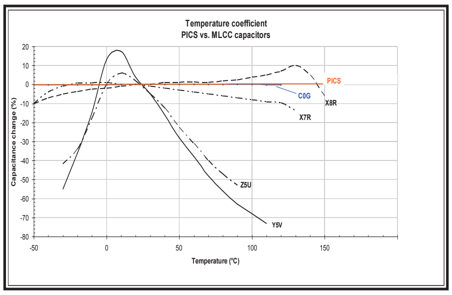


Fig.1 Capacitance change versus temperature variation compared with alternative dielectrics

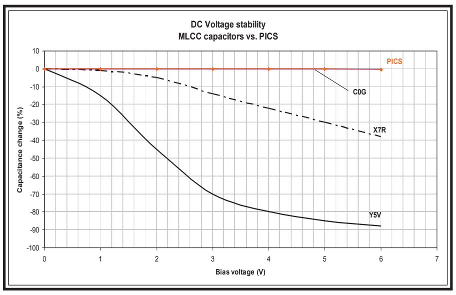


Fig.2 Capacitance change versus voltage variation compared with alternative dielectrics

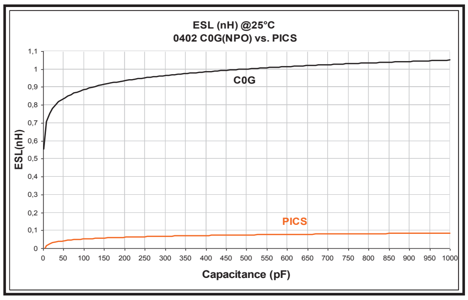


Fig.3 ESL versus capacitance value compared with alternative dielectrics

Part Number

935.131. **B.2** **S.** **U** **xx** →

Breakdown Voltage
4 = 11V
7 = 30V

Size
4 = 0402

Unit
0 = 10 f
1 = 0.1 p
2 = 1 p
3 = 10 p
4 = 0.1 n
5 = 1 n
6 = 10 n
7 = 0.1 µ
8 = 1 µ
9 = 10 u

Value (E6)
10
15
22
33
47
68

i.e.: 100 nF/0402 case (HSSC type)
→ 935.131.424.610

Termination and Outline

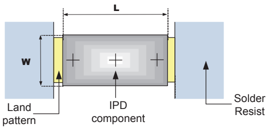
Termination

Lead-free nickel/solder coating compatible with automatic soldering technologies: reflow and manual.

Typical dimensions, all dimensions in mm.

Package outline

Typ.		0402
Comp. size	L	1.16±0.05
	W	0.66±0.05



(0402 PCB footprint)

Packaging

Tape and reel, tray, waffle pack or wafer delivery.

For more information, please visit: http://www.ipdia.com
To contact us, email to: sales@ipdia.com

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Document identifier: CL431 111 615 137

IPD Capacitor Assembly Set Up

Rev 1.0

Application Note

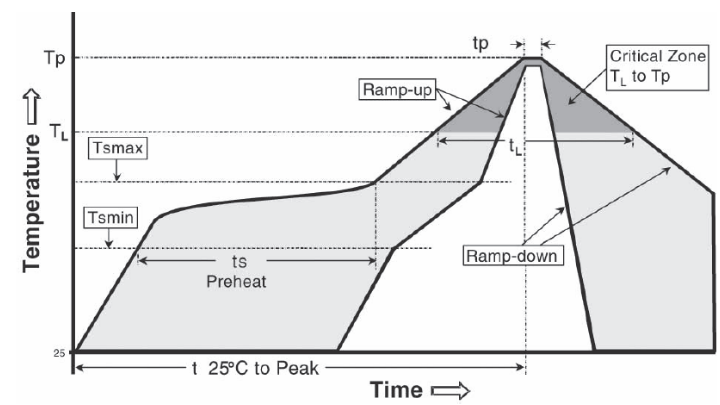
Outline

Silicon Capacitor for surface mounting device (SMD) assembly is a Wafer Level Chip Scale Packaging with the following features:

- Package dedicated to solve tombstoning effect of small SMD package;
- Package compatible with SMD assembly;
- Package without underfilling step;
- Interconnect available with various optional finishing for specific assembly.

Assembly consideration

- Standard pick & place equipment dedicated to WLCSP down to 400µm pitch.
- Solder paste type 3 in most cases of EIA size.
- Reflow has to be done with standard lead-free profile (for SAC alloys) or according to JEDEC recommendations J-STD 020D-01.

	Lead	**Leadfree**
	**Tp: 235 °C**	**Tp: 260 °C**
	TL: 183 °C	**TL: 217 °C**
	Ts min: 100 °C	**Ts min: 150 °C**
	Ts max: 150 °C	**Ts max: 200 °C**
	tL: 60-150 s	**tL: 60-150 s**

Process recommendation

After soldering, no solder paste should touch the side of the capacitor die as that might results in leakage currents due to remaining flux.

In order to use IPDiA standard capacitors within the JEDEC format and recommendation, the solder flux must be cleaned after reflow soldering step.
Notes: for a proper flux cleaning process, “rosin” flux type (R) or “water soluble” flux type (WS) is recommended for the solder printing material. “No clean” flux (NC) solder paste is not recommended.

In case the flux is not cleaned after the reflow soldering, the standard JEDEC would probably not be appropriate and the solder volume must be controlled:

- using smallest aperture design for the stencil, and using finer solder paste type 4 or 5 for a proper printing process.
- Mirroring pads would be the best recommendation

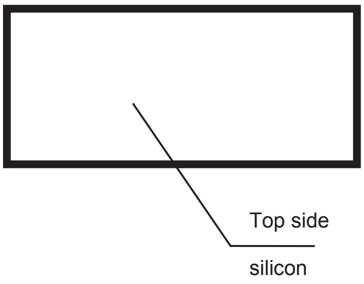
ipdia
The 3D Silicon Leader

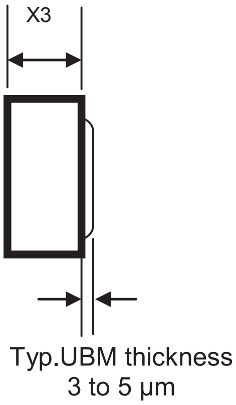
Pad recommendation

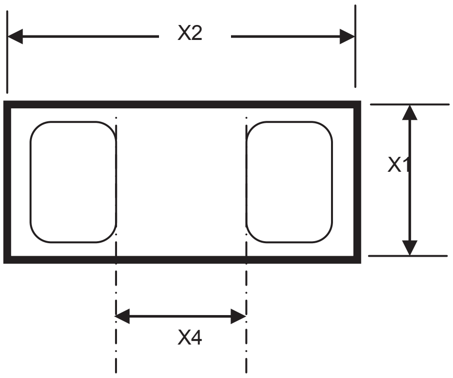
The capacitor is compatible with generic requirements for flip chip design (IPC7094).
Standard IPDiA 3D package can be compliant with established EIA size (0201, 0402, 0603, …).

Die size and land pattern dimensions is set up according to following range :

EIA size	0201	0402	0603	0805	1206	1812
Dimension max(X1 x X2) mm	0.86x0.66	1.26x0.76	1.86x1.16	2.26x1.46	3.46x1.86	4.76x3.66
Typical . die thickness X3 (mm)	0.1 or 0.4					
Typical pad size* (mm)	0.15x0.40	0.30x0.50	0.40x0.90	0.50x1.20	0.60x1.60	0.90x3.40
Typical pad separation (X4 mm)	0.3	0.4	0.8	1	2	2.7







After soldering, no solder paste should touch the side of the capacitor die as that might result in leakage currents due to remaining flux.

Manual Handling Considerations

These capacitors are designed to be mounted with a standard SMT line, using solder printing step, pick and place machine and a final reflow soldering step. In case of manual handling and mounting conditions, please follow below recommendations:

- Minimize mechanical pressure on the capacitors (use of a vacuum nozzle is recommended).
- Use of organic tip instead of metal tip for the nozzle.
- Minimize temperature shocks (Substrate pre-heating is recommended).
- No wire bonding on 0402 47nF, 0402 100nF, 1206 1µF and 1812 3,3µF

Process steps:

- On substrate, form the solder meniscus on each land pattern targeting 100 µm height after reflow (screen printing, dispensing solder paste or by wire soldering).
- Pick the capacitor from the tape & reel or the Gel Pack keeping backside visible using a vacuum nozzle and organic tip.
- Temporary place the capacitor on land pattern assuming the solder paste (Flux) will stick and maintain the capacitor.
- Reflow the assembly module with a dedicated thermal profile (see reflow recommendation profile).

Murata:

935131424410-T3N 935131424510-T3N 935131424533-T3N 935131424610-T3N 935131424310-T3A 935131424310-T3N 935131424347-T3N 935131424522-T1N 935131424522-T3N 935131424547-T1N 935131424547-T3N 935131424610-T3A 935131724547-T3N 935131424347-T1N 935131424310-T1N 935131724547-T1N