Absolute Maximum Ratings (T_A = 25°C)

V_{DELB} 25V
V_{DRVP} 36V
V_{DRVN} . . . . . -20V
V_{DDP}, V_{DD} 6.5V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package.	40	7.5

V_{DRVL} 6.5V
Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Maximum Continuous Junction Temperature . . . . . 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 40mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, over temperature from -40°C to 85°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
V_S	Supply Voltage		3		5.5	V
I_S	Quiescent Current	Enabled, LX not switching		1.6	2.5	mA
		Disabled, EL7520		5	30	µA
		Disabled, EL7520A		640	800	µA
F_{OSC}	Oscillator Frequency		900	1000	1100	kHz
BOOST						
V_{REF}	Reference Voltage	T_A = 25°C	1.19	1.215	1.235	V
			1.187	1.215	1.238	V
C_{REF}	V_{REF} Capacitor			100		nF
V_{FBB}	Feedback Reference Voltage	T_A = 25°C	1.192	1.205	1.218	V
			1.188	1.205	1.222	V
V_{F_FBB}	FBB Fault Trip Point	V_{FBB} falling		1		V
D_{MAX}	Maximum Duty Cycle		85			%
Eff	Boost Efficiency	Test with 24mΩ $R_{DS(ON)}$ MOSFET, I_{LOAD} = 400mA		90		%
$I(V_{REF})$	Feedback Input Bias Current	PI mode, V_{FBB} = 1.35V		50	500	nA
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	C_{INT} = 2.2nF, I_{OUT} = 200mA V_{IN} = 3V to 5.5V		0.05		%/V
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation - "P" Mode	C_{INT} pin strapped to V_{DD}		3		%
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation - "PI" Mode	I_{OUT} = 10mA to 200mA		0.1		%
V_{CINT_T}	CINT PI Mode Select Threshold			4.7	4.8	V
V_{ON} LDO						
V_{FBP}	FBP Regulation Voltage	I_{DRVP} = 0.2mA, T_A = 25°C	1.181	1.211	1.229	V
		I_{DRVP} = 0.2mA	1.177	1.211	1.233	V
V_{F_FBP}	FBP Fault Trip Point	V_{FBP} falling	0.95	1	1.05	V
I_{FBP}	FBP Input Bias Current	V_{FBP} = 1.35V	-250		250	nA
GMP	FBP Effective Transconductance	V_{DRVP} = 25V, I_{DRVP} = 0.2 to 2mA		50		mS

Electrical Specifications V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 40mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, over temperature from -40°C to 85°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
$\Delta V_{ON}/\Delta I(V_{ON})$	V_{ON} Load Regulation	$I(V_{ON})$ = 0mA to 20mA		-0.5		%
I_{DRVP}	DRVP Sink Current	V_{FBP} = 1.1V, V_{DRVP} = 25V	2	4		mA
I_{L_DRVP}	DRVP Leakage Current	V_{FBL} = 1.5V, V_{DRVL} = 35V		0.1	5	µA
V_{OFF} LDO						
V_{FBN}	FBN Regulation Voltage	I_{DRVN} = 0.2mA, T_A = 25°C	0.173	0.203	0.233	V
		I_{DRVN} = 0.2mA	0.171	0.203	0.235	V
V_{F_FBN}	FBN Fault Trip Point	V_{FBN} falling	0.38	0.4	0.48	V
I_{FBN}	FBN Input Bias Current	V_{FBN} = 1.25V	-250		250	nA
GMN	FBN Effective Transconductance	V_{DRVN} = -6V, I_{DRVN} = 0.2mA to 2mA		50		mS
$\Delta V_{OFF}/\Delta I(V_{OFF})$	V_{OFF} Load Regulation	$I(V_{OFF})$ = 0mA to 20mA		-0.15		%
I_{DRVN}	DRVN Source Current	V_{FBN} = 0.3V, V_{DRVN} = -6V	2	4		mA
I_{L_DRVN}	DRVN Leakage Current	V_{FBN} = 0V, V_{DRVN} = -20V		0.1	5	µA
V_{LOGIC} LDO						
V_{FBL}	FBL Regulation Voltage	I_{DRVL} = 1mA, T_A = 25°C	1.176	1.2	1.224	V
		I_{DRVL} = 1mA	1.174	1.2	1.226	V
V_{F_FBL}	FBL Fault Trip Point	V_{FBL} falling	0.90	1	1.05	V
I_{FBL}	FBL Input Bias Current	V_{FBL} = 1.25V	-500		500	nA
GML	FBL Effective Transconductance	V_{DRVL} = 2.5V, I_{DRVP} = 1mA to 8mA		200		mS
$\Delta V_{LOGIC}/\Delta I(V_{LOGIC})$	V_{LOGIC} Load Regulation	$I(V_{LOGIC})$ = 0mA to 500mA		-0.5		%
I_{DRVL}	DRVL Sink Current	V_{FBL} = 1.1V, V_{DRVL} = 2.5V	5	16		mA
I_{L_DRVL}	DRVL Leakage Current	V_{FBL} = 1.5V, V_{DRVL} = 5.5V		0.1	5	µA
SEQUENCING						
t_{ON}	Turn On Delay	C_{DLY} = 0.1µF		30		ms
t_{SS}	Soft-start Time	C_{DLY} = 0.1µF		2		ms
t_{DEL1}	Delay Between A_{VDD} and V_{OFF}	C_{DLY} = 0.1µF		10		ms
t_{DEL2}	Delay Between V_{ON} and V_{OFF}	C_{DLY} = 0.1µF		17		ms
t_{DEL3}	Delay Between V_{OFF} and Delayed V_{BOOST}	C_{DLY} = 0.1µF		10		ms
I_{DELB}	DELB Pull-down Current	V_{DELB} > 0.6V		50		µA
		V_{DELB} < 0.6V		1.4		mA
C_{DEL}	Delay Capacitor			100		nF
FAULT DETECTION						
T_{FAULT}	Fault Time Out	C_{DLY} = 0.1µF		50		ms
OT	Over-temperature Threshold			140		°C
I_{PG}	PG Pull-down Current	VPG > 0.6V		15		µA
		VPG < 0.6V		1.7		mA
LOGIC						
V_{HI}	Logic High Threshold		2.2			V
V_{LO}	Logic Low Threshold				0.8	V
I_{LOW}	Logic Low bias Current		-1	0.1	1	µA
I_{HIGH}	Logic High bias Current		12	18	24	µA

Typical Performance Curves

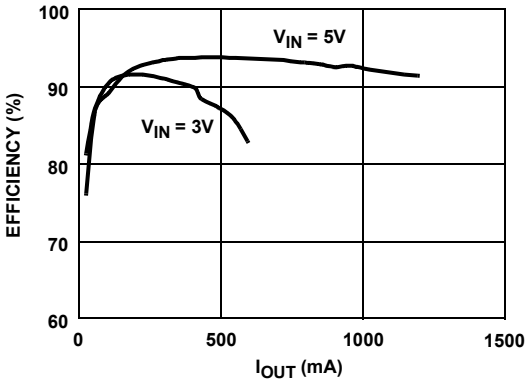


FIGURE 1. V_{BOOST} EFFICIENCY vs I_{OUT} (PI MODE)

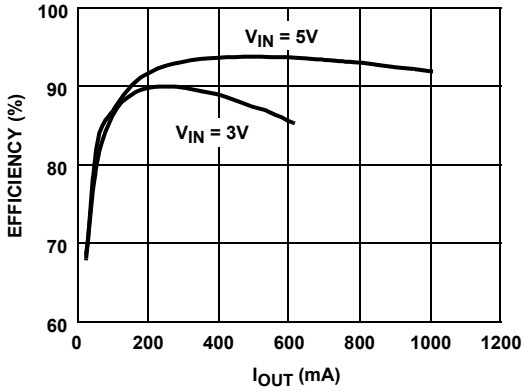


FIGURE 2. V_{BOOST} EFFICIENCY vs I_{OUT} (P MODE)

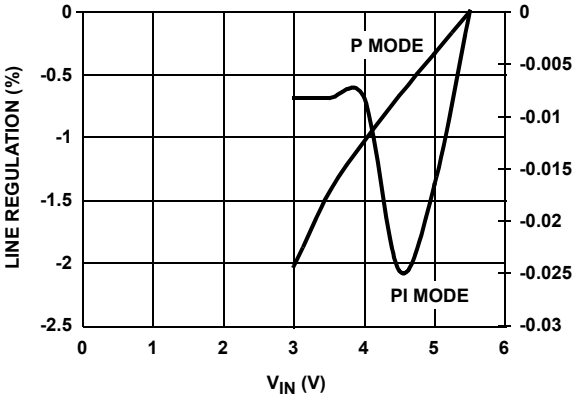


FIGURE 3. V_{BOOST} LINE REGULATION

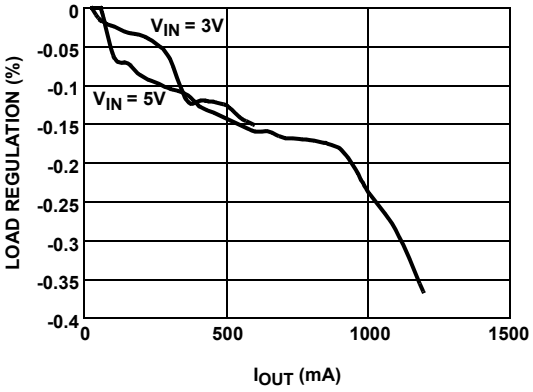


FIGURE 4. V_{BOOST} LOAD REGULATION (PI MODE)

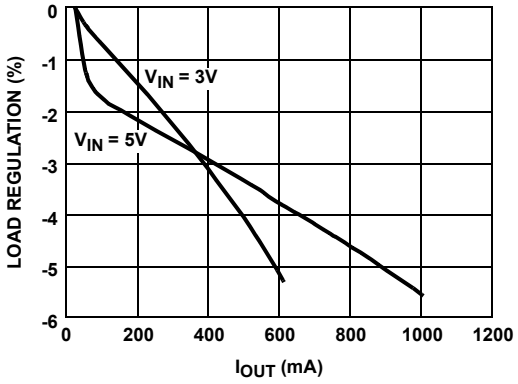


FIGURE 5. V_{BOOST} LOAD REGULATION (P MODE)

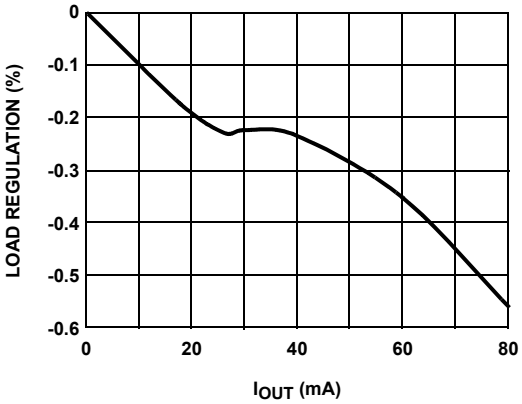


FIGURE 6. V_{ON} LOAD REGULATION

Typical Performance Curves (Continued)

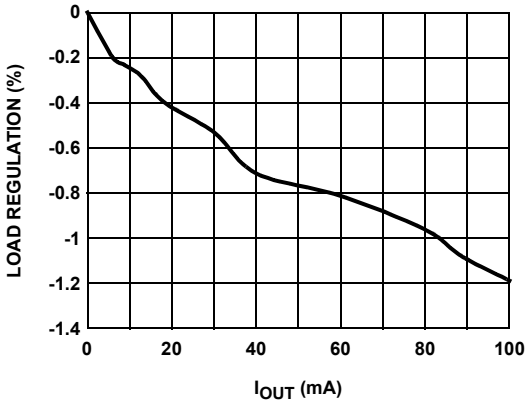


FIGURE 7. V_{OFF} LOAD REGULATION

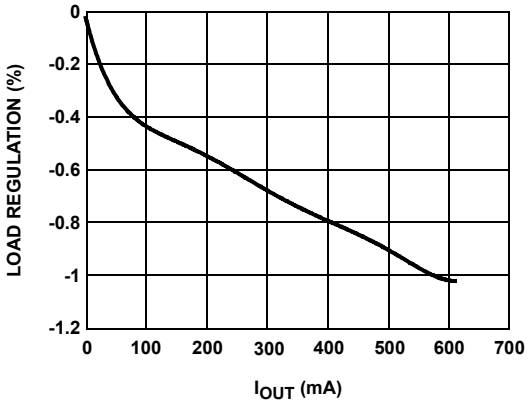


FIGURE 8. V_{LOGIC} LOAD REGULATION

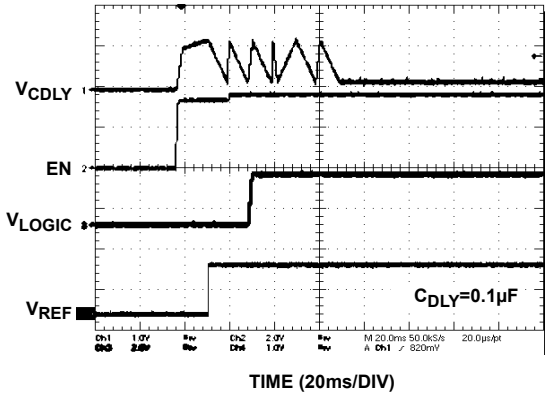


FIGURE 9. EL7520 START-UP SEQUENCE

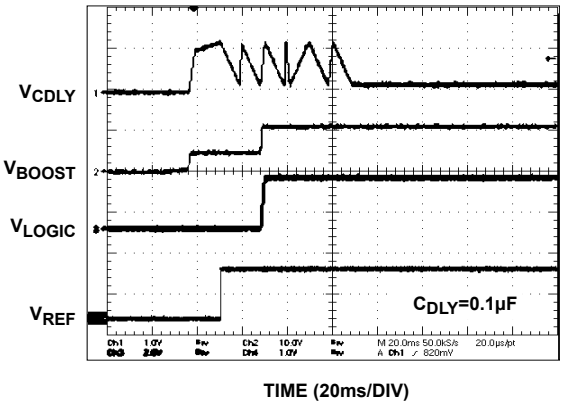


FIGURE 10. EL7520 START-UP SEQUENCE

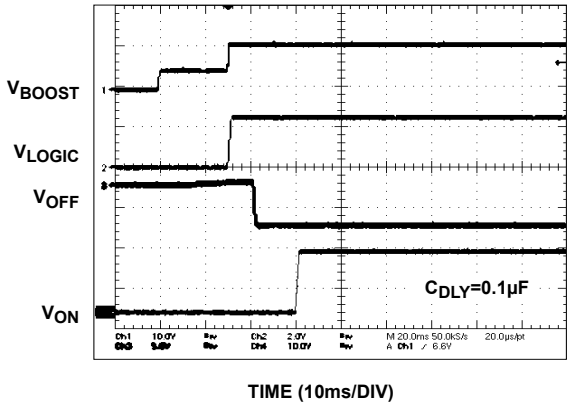


FIGURE 11. EL7520 START-UP SEQUENCE

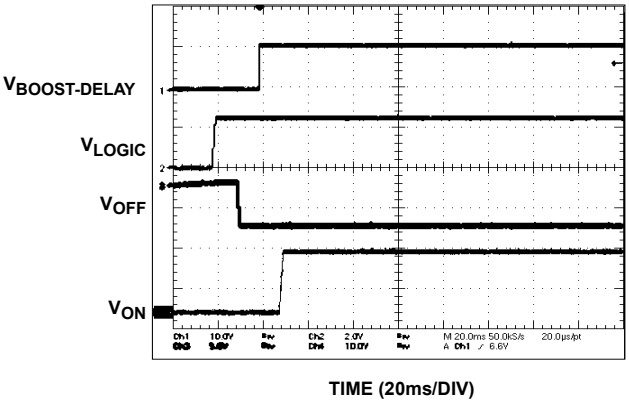


FIGURE 12. EL7520 START-UP SEQUENCE

Typical Performance Curves (Continued)

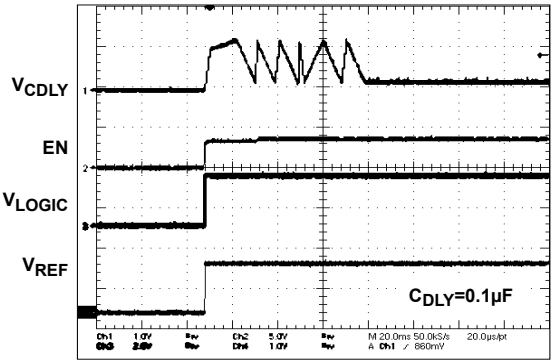


FIGURE 13. EL7520A START-UP SEQUENCE

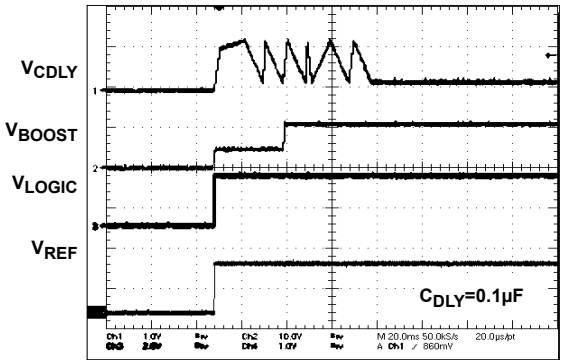


FIGURE 14. EL7520A START-UP SEQUENCE

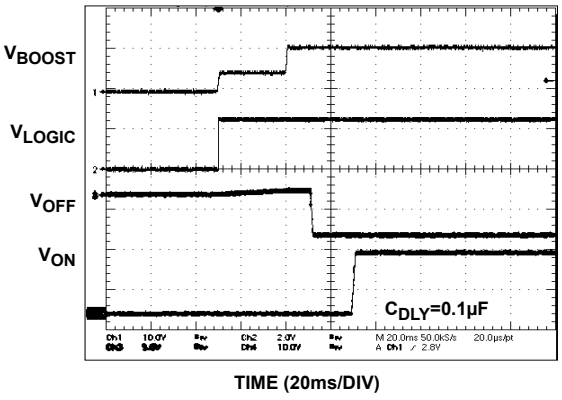


FIGURE 15. EL7520A START-UP SEQUENCE

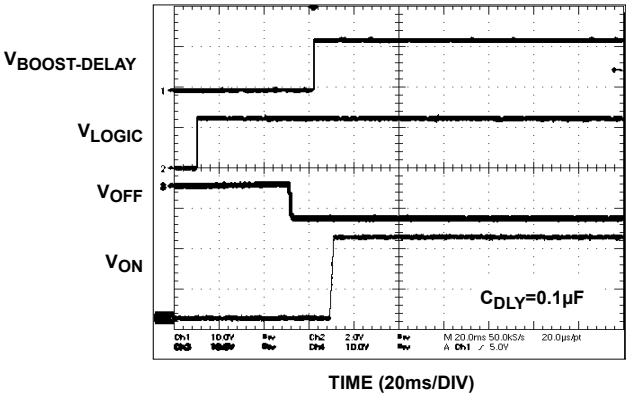


FIGURE 16. EL7520A START-UP SEQUENCE

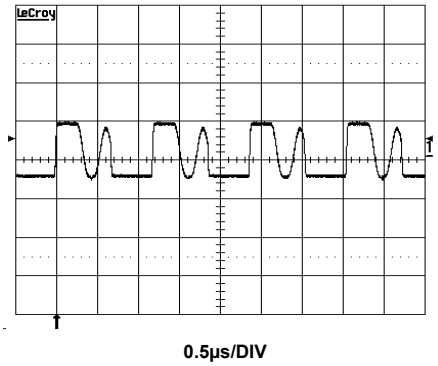
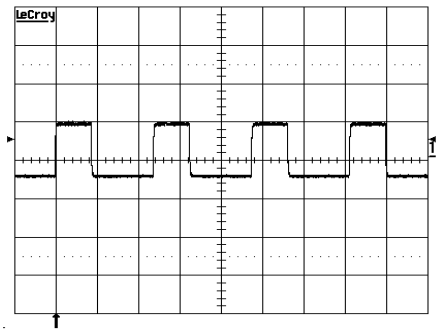


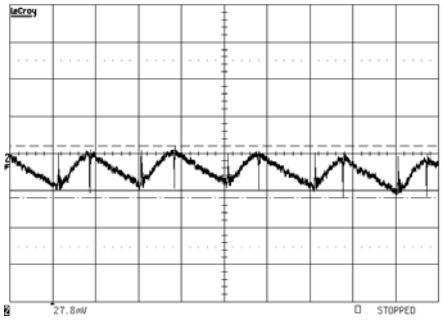
FIGURE 17. LX WAVEFORM-DISCONTINUOUS MODE

Typical Performance Curves (Continued)



0.5µs/DIV

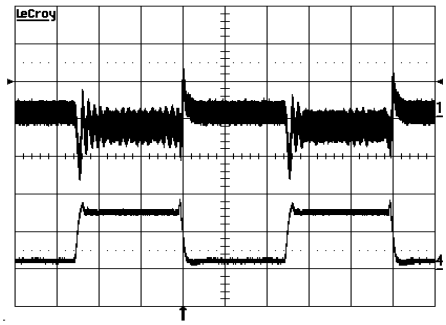
FIGURE 18. LX WAVEFORM-CONTINUOUS MODE



20mV/DIV

FIGURE 19. V_{BOOST} OUTPUT VOLTAGE RIPPLE

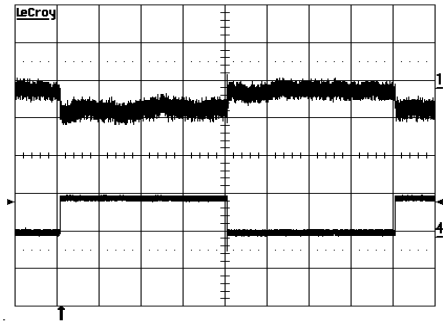
CH1=V_{BOOST}, 100mV/DIV
CH4=LOAD CURRENT, 200mA/DIV



0.2ms/DIV

FIGURE 20. V_{BOOST} TRANSIENT RESPONSE

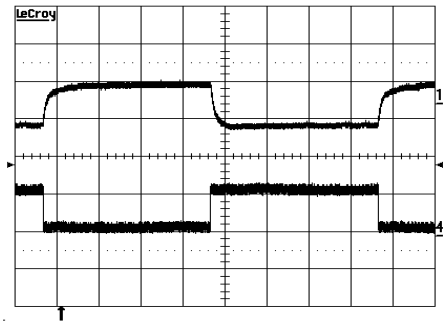
CH1=V_{LOGIC}, 20mV/DIV
CH4=LOAD CURRENT, 100mA/DIV



50µs/DIV

FIGURE 21. V_{LOGIC} TRANSIENT RESPONSE

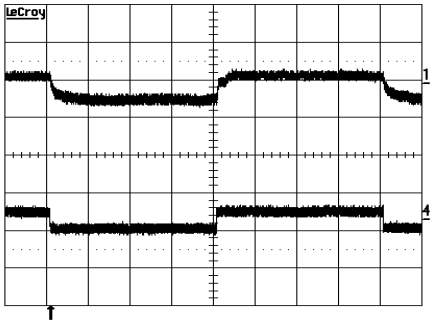
CH1=V_{ON}, 100mV/DIV
CH4=LOAD CURRENT, 50mA/DIV



50µs/DIV

FIGURE 22. V_{ON} TRANSIENT RESPONSE

CH1=V_{OFF}, 50mV/DIV
CH4=LOAD CURRENT, 50mA/DIV



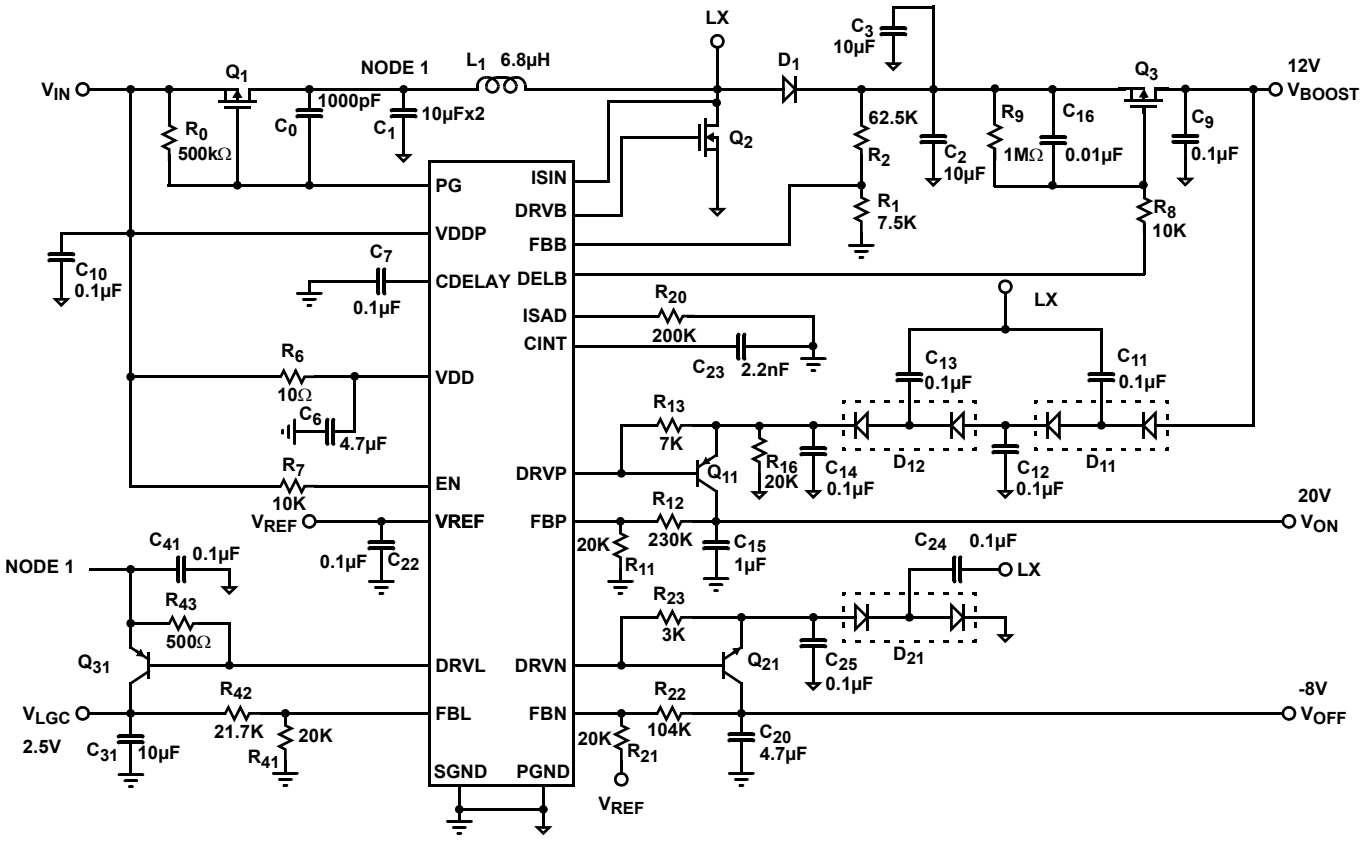
50µs/DIV

FIGURE 23. V_{OFF} TRANSIENT RESPONSE

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION DESCRIPTION
1	CDLY	With a capacitor connected from this pin to GND sets the delay time for start-up sequence and sets the fault timeout time
2	DRVB	Gate driver output for the external N channel switch; the pulse voltage follows the input voltage
3	PGND	Power GND
4	ISAD	With a resistor connected from this pin to GND sets the current limit of the external N channel FET
5	ISIN	Sense the drain voltage of the external N channel FET and connected to the internal current limit comparator
6	DELB	Active low control output for optional delay control for external V_{BOOST} P channel FET; when fault is detected, this pin goes to high
7	SGND	Low noise signal ground
8	FBB	Boost regulator voltage feedback input pin; regulates to 1.2V nominal
9	CINT	V_{BOOST} integrator output, connect 2.2nF to analog GND for PI mode or connect to V_{REF} for P mode operation
10	VREF	Bandgap voltage bypass terminal; bypass with a 0.1µF to analog GND; can be used as charge pump reference
11	FBN	Negative LDO voltage feedback input pin; regulates to 0.2V nominal
12	DRVN	Negative LDO base drive; open drain of an internal P channel MOSFET
13	FBL	Logic LDO voltage feedback input pin; regulates to 1.2V nominal
14	DRVL	Logic LDO base drive; open drain of an internal N channel MOSFET
15	FBP	Positive LDO voltage feedback input pin; regulates to 1.2V nominal
16	DRVP	Positive LDO base drive; open drain of an internal N channel MOSFET
17	EN	Enable pin for the chip; high enable; low disabled
18	VDD	Positive supply for all internal circuitry except DRVB
19	VDDP	Positive supply for external N channel FET gate drive (DRVB)
20	PG	Output gate drive of the external fault protection P channel FET; when chip is disabled or when a fault has been detected, this pin is high

Typical Application



Applications Information

The EL7520 and EL7520A provide a multiple output power supply solution for TFT-LCD applications. The system consists of a high efficiency boost controller and three low cost linear-regulator controllers (V_{ON}, V_{OFF}, and V_{LOGIC}).

The block diagram of the whole part is shown in Figure 24. Table 1 lists the recommended components.

TABLE 1. RECOMMENDED COMPONENTS

DESIGNATION	DESCRIPTION
C1, C2, C3, C31	10µF, 16V, X7R ceramic capacitor (1206) TDK C3216X7R1C106M
C20	4.7µF, 16V X5R ceramic capacitor (1206) TDK C3216X5R1A475K
C15	1µF, 25V X7R ceramic capacitor (1206) TDK C3216X7R1E105K
D1	1A 20V low leakage schottky rectifier (CASE 457-04) ON SEMI MBRM120ET3
D11, D12, D21	200mA 30V schottky barrier diode (SOT-23) Fairchild BAT54S
L1	6.8mH 1.3A inductor TDK SLF6025T-6R8M1R3-PF

TABLE 1. RECOMMENDED COMPONENTS (Continued)

DESIGNATION	DESCRIPTION
Q1	-2.4 -20V P-channel 1.8V specified PowerTrench MOSFET (SuperSOT-3) Fairchild FDN304P
Q2	6.3A 30V single N-channel logic level PowerTrench MOSFET (SOT-23) Fairchild FDC655AN
Q3	-2A –30V single P-channel logic level PowerTrench MOSFET (SuperSOT-3) Fairchild FDN360P
Q11	200mA 40V PNP amplifier (SOT-23) Fairchild MMBT3906
Q21	200mA 40V NPN amplifier (SOT-23) Fairchild MMBT3904
Q31	1A 30V PNP low saturation amplifier (SOT-23) Fairchild FMMT549

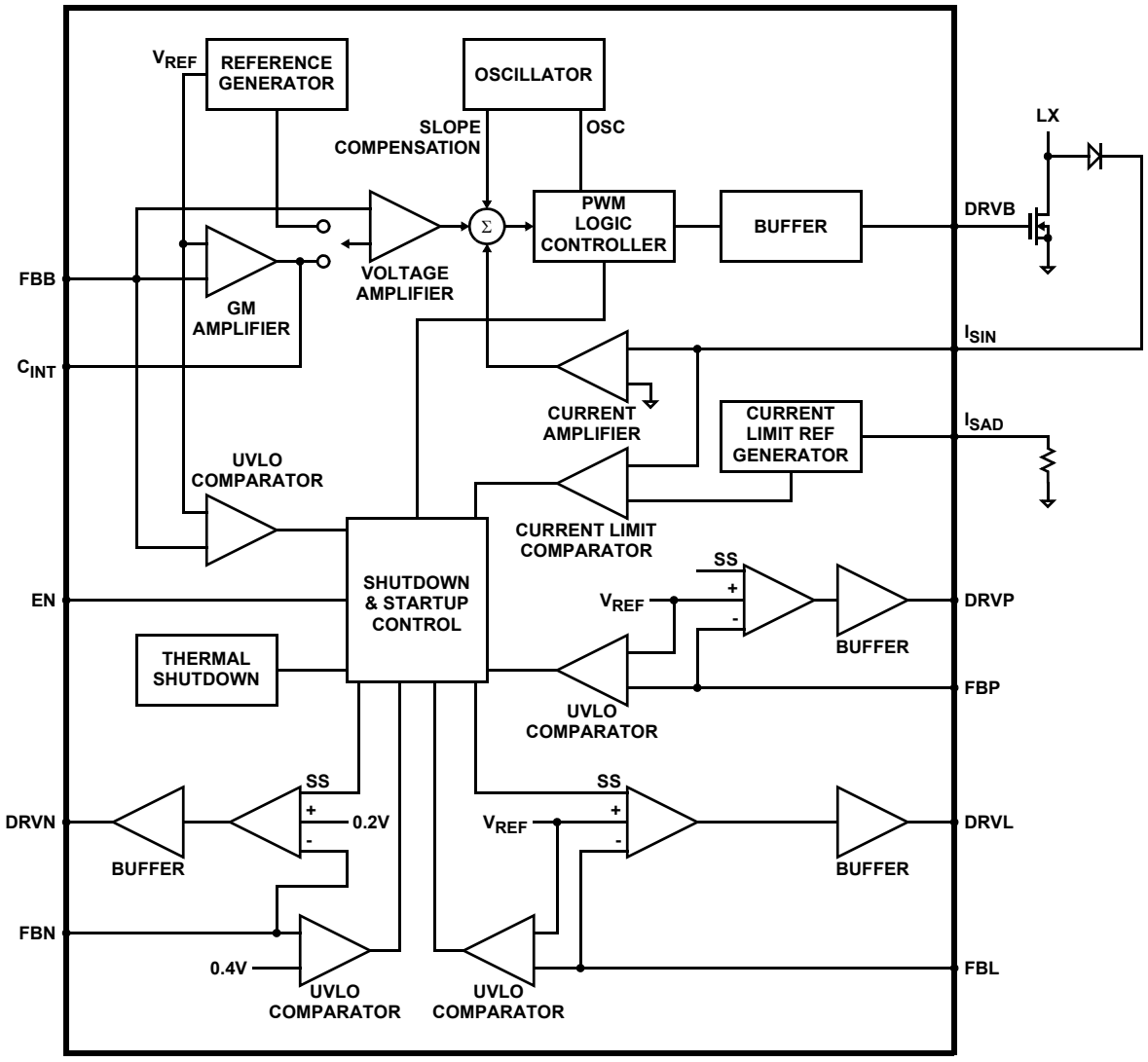


FIGURE 24. BLOCK DIAGRAM

Boost Converter

The main boost converter is a current mode PWM controller operating at a fixed frequency. The 1MHz switching frequency enables the use of low profile inductor and multilayer ceramic capacitors, which results in a compact, low-cost power system for LCD panel design.

The boost converter can operate in continuous or discontinuous inductor current mode. The EL7520 and EL7520A are designed for continuous current mode, but they can also operate in discontinuous current mode at light load. In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by:

$$\frac{V_{BOOST}}{V_{IN}} = \frac{1}{1-D}$$

Where D is the duty cycle of switching MOSFET.

Figure 25 shows the function diagram of the boost controller. It uses a summing amplifier architecture consisting of GM stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by the following equation:

$$V_{BOOST} = \frac{R_1 + R_2}{R_1} \times V_{REF}$$

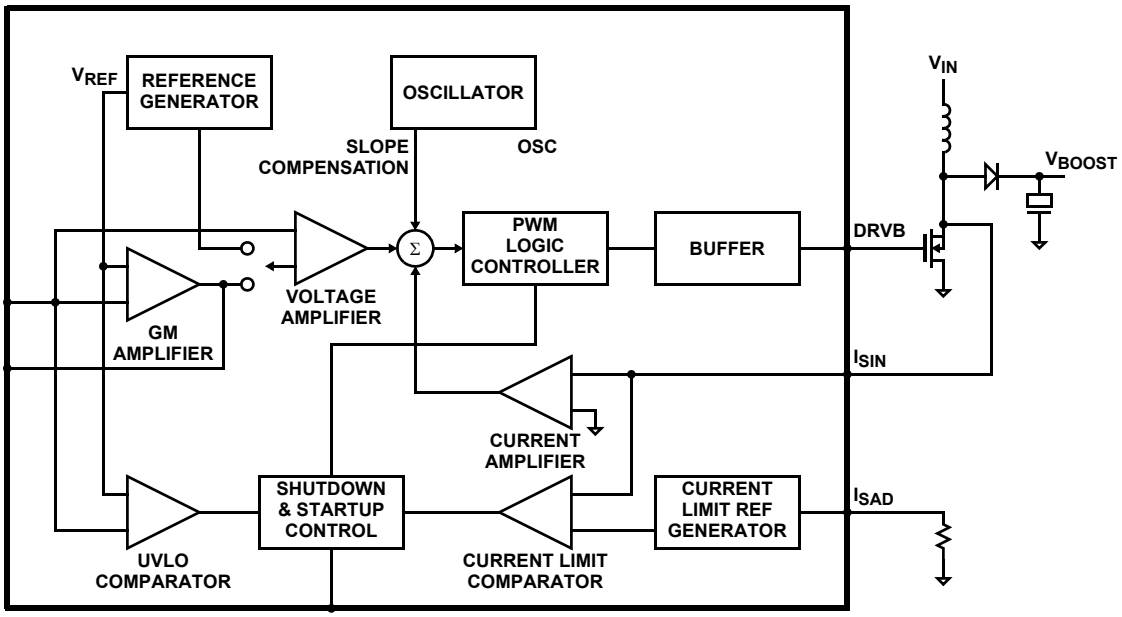


FIGURE 25. FUNCTION DIAGRAM OF THE BOOST CONTROLLER

The internal current limit circuitry is shown in Figure 26. The circuit senses the voltage across the $R_{DS(ON)}$ when the MOSFET is on; then compare it to the internal voltage reference to realize the current limit. The internal voltage reference is generated by a 10µA current and any additional current set at I_{SAD} pin flowing through an 8kΩ resistor. The voltage reference is based on the following equation:

$$V_{THRESHOLD} = \left(\frac{V_{ISAD}}{R_1} + 10\mu A\right) \times 8K$$

Where V_{ISAD} is the voltage at pin I_{SAD}.

$$V_{ISAD} = V_{REF} - V_{BE} - 1K \times I_{SAD}$$

$$I_{SAD} = \frac{V_{ISAD}}{R1}$$

Where $V_{BE} \approx 0.7V$

The external resistor R_1 should be chosen in the order of 100K to generate µA of current.

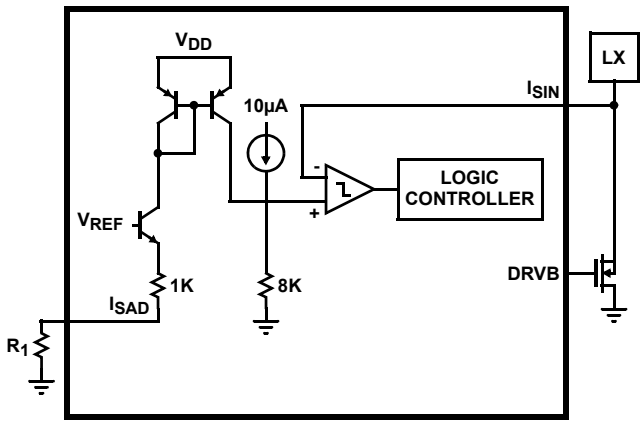


FIGURE 26. CURRENT LIMIT BLOCK DIAGRAM

Hence the maximum output current is determined by the following equation:

$$I_{OMAX} = \left(\frac{V_{THRESHOLD}}{R_{DSON}} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O}$$

Where ΔI_L is the peak to peak inductor ripple current, and is set by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S}$$

f_S is the switching frequency; D is the duty cycle.

$$D = \frac{V_O - V_{IN}}{V_O}$$

Input Capacitor

The input capacitor is used to supply the current to the converter. It is recommended that C_{IN} be larger than 10µF. The reflected ripple voltage will be smaller with larger C_{IN}. The voltage rating of input capacitor should be larger than maximum input voltage.

Boost Inductor

A 3.3µH inductor is recommended due to the fixed internal slope compensation. The inductor must be able to handle the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1-D}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

Switching MOSFET

Due to the parasitic inductance of the trace, the MOSFET will experience spikes higher that the output voltage when the MOSFET turns off. Thus, a MOSFET with enough voltage margin is needed.

The $R_{DS(ON)}$ of the MOSFET is critical for power dissipation and current limit. A MOSFET with low $R_{DS(ON)}$ is desired to get high efficiency and output current, but very low $R_{DS(ON)}$ will reduce the loop stability. A MOSFET with 20mΩ to 50mΩ $R_{DS(ON)}$ is recommended. Some recommended MOSFETs are shown in following table.

TABLE 2. RECOMMENDED MOSFETs

PART NUMBER	MANUFACTURER	FEATURE
FDC655AN	Fairchild Semiconductor	6.3A, 30V, $R_{DS(ON)}$ = 23mΩ
FDS4488	Fairchild Semiconductor	7.9A, 30V, $R_{DS(ON)}$ = 22mΩ
Si7844DP	Vishay	10A, 30V, $R_{DS(ON)}$ = 22mΩ
SI6928DQ	Vishay	20A, 30V, $R_{DS(ON)}$ = 30mΩ

Rectifier Diode

A high-speed diode is desired due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The rectifier diode must meet the output current and peak inductor current requirements.

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_S}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Compensation

The EL7520 and EL7520A can operate in either P mode or PI mode. Connecting C_{INT} pin directly to V_{IN} will enable P mode. For better load regulation, use PI mode with a 2.2nF capacitor between C_{INT} and ground.

Linear-Regulator Controllers (V_{ON}, V_{LOGIC}, and V_{OFF})

The EL7520, EL7520A include three independent linear-regulator controllers, in which two are positive output voltage (V_{ON} and V_{LOGIC}), and one is negative. The V_{ON}, V_{OFF}, and V_{LOGIC} linear-regulator controller functional diagrams, applications circuits are shown in Figures 27, 28, and 29 respectively.

Calculation of the Linear Regulator Base-Emitter Resistors (R_{BL}, R_{BP} and R_{BN})

For the pass transistor of the linear regulator, low frequency gain (Hfe) and unity gain freq. (f_T) are usually specified in the datasheet. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/Hfe$. Therefore, in order to maintain phase margin at low frequency, the best choice for a pass device is often a high frequency low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor R_{BE} (R_{BP}, R_{BL}, R_{BN} in the Functional Block Diagram), which increase the pole frequency to: $f_p = f_T*(1+ Hfe *re/R_{BE})/Hfe$, where re = KT/qIc. So choose the lowest value R_{BE} in the design as long as there is still enough base current (I_B) to support the maximum output current (I_C).

We will take as an example the V_{LOGIC} linear regulator. If a Fairchild FMMT549 PNP transistor is used as the external pass transistor, Q31 in the application diagram, then for a maximum V_{LOGIC} operating requirement of 500mA the data sheet indicates Hfe_min = 100.

The base-emitter saturation voltage is: Vbe_max = 1.25V (note this is normally a Vbe ~ 0.7V, however, for the Q5 transistor an internal Darlington arrangement is used to increase it's current gain, giving a 'base-emitter' voltage of 2 x V_{BE}).

(Note that using a high current Darlington PNP transistor for Q5 requires that $V_{IN} > V_{LOGIC} + 2V$. Should a lower input voltage be required, then an ordinary high gain PNP transistor should be selected for Q5 so as to allow a lower collector-emitter saturation voltage).

For the EL7520, EL7520A, the minimum drive current is: I_DRVL_min = 8mA

The minimum base-emitter resistor, R_{BL}, can now be calculated as:

R_{BL}_min = V_{BE}_max/(I_DRVL_min - Ic/Hfe_min) = 1.25V/(8mA - 500mA/100) = 417Ω

This is the minimum value that can be used - so, we now choose a convenient value greater than this minimum value; say 500Ω. Larger values may be used to reduce quiescent current, however, regulation may be adversely affected, by supply noise if R_{BL} is made too high in value.

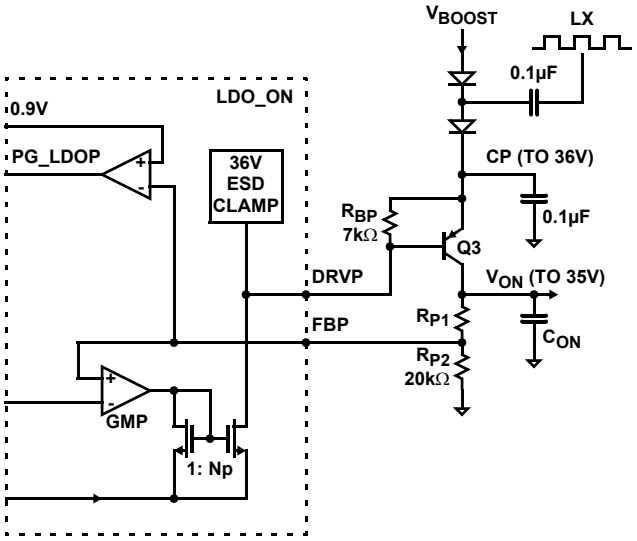


FIGURE 27. V_{ON} FUNCTIONAL BLOCK DIAGRAM

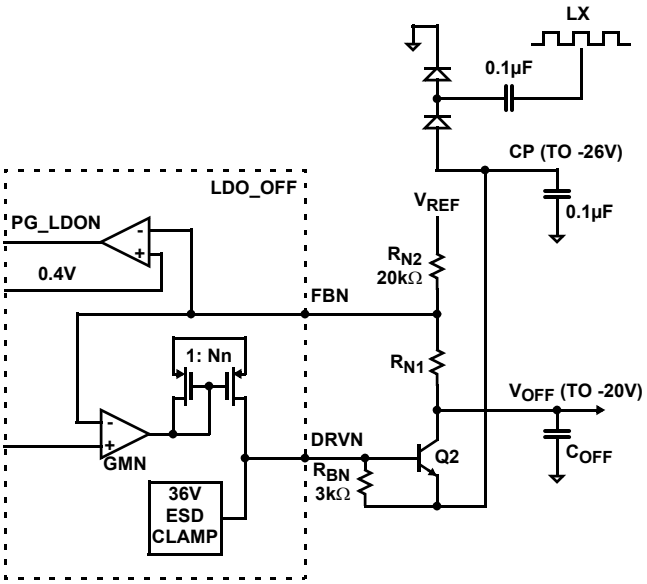


FIGURE 28. V_{OFF} FUNCTIONAL BLOCK DIAGRAM

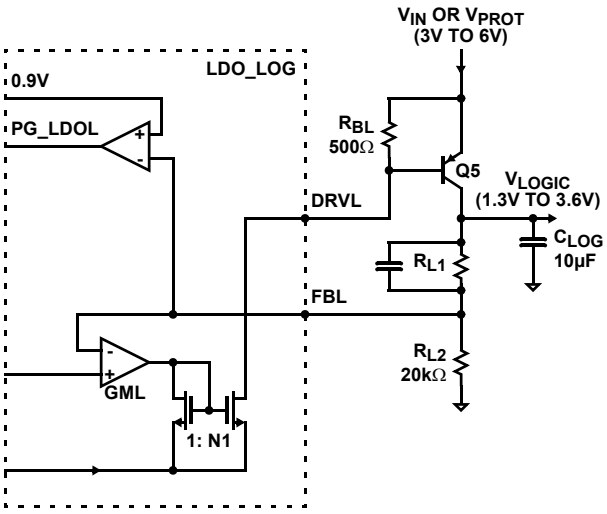


FIGURE 29. V_{LOGIC} FUNCTIONAL BLOCK DIAGRAM

The V_{ON} power supply is used to power the positive supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO_ON). The LDO_ON regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 4mA drive current, which is sufficient for up to 40mA or more output current under the low dropout condition (forced beta of 10). Typical V_{ON} voltage supported by EL7520, EL7520A range from +15V to +36V. A fault comparator is also included for monitoring the output voltage. The under-voltage threshold is set at 25% below the 1.2V reference.

The V_{OFF} power supply is used to power the negative supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO_OFF). The LDO_OFF regulator uses an external NPN transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 4mA drive current, which is sufficient for up to 40mA or more output current under the low dropout condition (forced beta of 10). Typical V_{OFF} voltage supported by EL7520, EL7520A range from -5V to -20V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 200mV above the 0.2V reference level.

The V_{LOGIC} power supply is used to power the logic circuitry within the LCD panel. The DC/DC may be powered directly from the low voltage input, 3.3V or 5.0V, or it may be powered through the fault protection switch. The LDO_LOGIC regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 16mA drive current, which is sufficient for up to 160mA or more output current

under the low dropout condition (forced beta of 10). Typical V_{LOGIC} voltage supported by EL7520, EL7520A range from +1.3V to V_{DD}-0.2V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 25% below the 1.2V reference.

Set-Up LDOs Output Voltage

Refer to Typical Application Diagram, the output voltages of V_{ON}, V_{OFF}, and V_{LOGIC} are determined by the following equations:

$$V_{ON} = V_{REF} \times \left(1 + \frac{R_{12}}{R_{11}}\right)$$

$$V_{OFF} = V_{REFN} + \frac{R_{22}}{R_{21}} \times (V_{REFN} - V_{REF})$$

$$V_{LOGIC} = V_{REF} \times \left(1 + \frac{R_{42}}{R_{41}}\right)$$

Where V_{REF} = 1.2V, V_{REFN} = 0.2V.

Charge Pump

To generate an output voltage higher than V_{BOOST}, single or multi stages of charge pumps are needed. The number of stage is determined by the input and output voltage. For positive charge pump stages:

$$N_{POSITIVE} \geq \frac{V_{OUT} + V_{CE} - V_{INPUT}}{V_{INPUT} - 2 \times V_F}$$

where V_{CE} is the dropout voltage of the pass component of the linear regulator. It ranges from 0.3V to 1V depending on the transistor. V_F is the forward-voltage of the charge pump rectifier diode.

The number of negative charge pump stages is given by:

$$N_{NEGATIVE} \geq \frac{|V_{OUTPUT}| + V_{CE}}{V_{INPUT} - 2 \times V_F}$$

To achieve high efficiency and low material cost, the lowest number of charge pump stages, which can meet the above requirements, is always preferred.

Charge Pump Output Capacitors

A ceramic capacitor with low ESR is recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be chosen by the following equation:

$$C_{OUT} \geq \frac{I_{OUT}}{2 \times V_{RIPPLE} \times f_{OSC}}$$

Where f_{SOC} is the switching frequency.

Start-Up Sequence

Figures 30 and 31 show detailed start-up sequence waveforms, EL7520 and EL7520A, respectively. For a successful power-up, there should be six peaks at V_{CDLY}. When a fault is detected, the device will latch off until either EN is toggled or the input supply is recycled.

If EN is L, the device is powered down. If EN is H, and the input voltage (V_{DD}) exceeds 2.5V, an internal current source starts to charge C_{DLY} to an upper threshold using a fast ramp followed by a slow ramp. If EN is low at this point, the C_{DLY} ramp will be delayed until EN goes high.

The first four ramps on C_{DLY} (two up, two down) are used to initialize the fault protection switch and to check whether there is a fault condition on C_{DLY} or V_{REF}. If a fault is detected, the outputs and the input protection will turn off and the chip will power down. For EL7520A, V_{REF} will stay on.

If no fault is found, C_{CDLY} continues ramping up and down until the sequence is completed.

During the second ramp, the device checks the status of V_{REF} and over temperature. At the peak of the second ramp, PG output goes low and enables the input protection PMOS Q1. Q1 is a controlled FET used to prevent in-rush current into V_{BOOST} before V_{BOOST} is enabled internally. Its rate of turn on is controlled by C_o. When a fault is detected, Q1 will turn off and disconnect the inductor from V_{IN}.

With the input protection FET on, NODE1 (See Typical Application Diagram) will rise to ~V_{IN}. Initially the boost is not enabled so V_{BOOST} rises to V_{IN}-V_{DIODE} through the output diode. Hence, there is a step at V_{BOOST} during this part of the start-up sequence. If this step is not desirable, an external PMOS FET can be used to delay the output until the boost is enabled internally. The delayed output appears at A_{VDD}.

For EL7520, V_{BOOST} and V_{LOGIC} soft-start at the beginning of the third ramp. The soft-start ramp depends on the value of the C_{DLY} capacitor. For C_{DLY} of 220nF, the soft-start time is ~2ms. EL7520A is the same as EL7520 except that V_{REF} and V_{LOGIC} turn on once input voltage exceeds 2.5V.

V_{OFF} turns on at the start of the fourth peak. At the fifth peak, DELB gate goes low to turn on the external PMOS Q4 to generate a delayed V_{BOOST} output.

V_{ON} is enabled at the beginning of the sixth ramp. A_{VDD}, PG, V_{OFF}, DELB and V_{ON} are checked at end of this ramp.

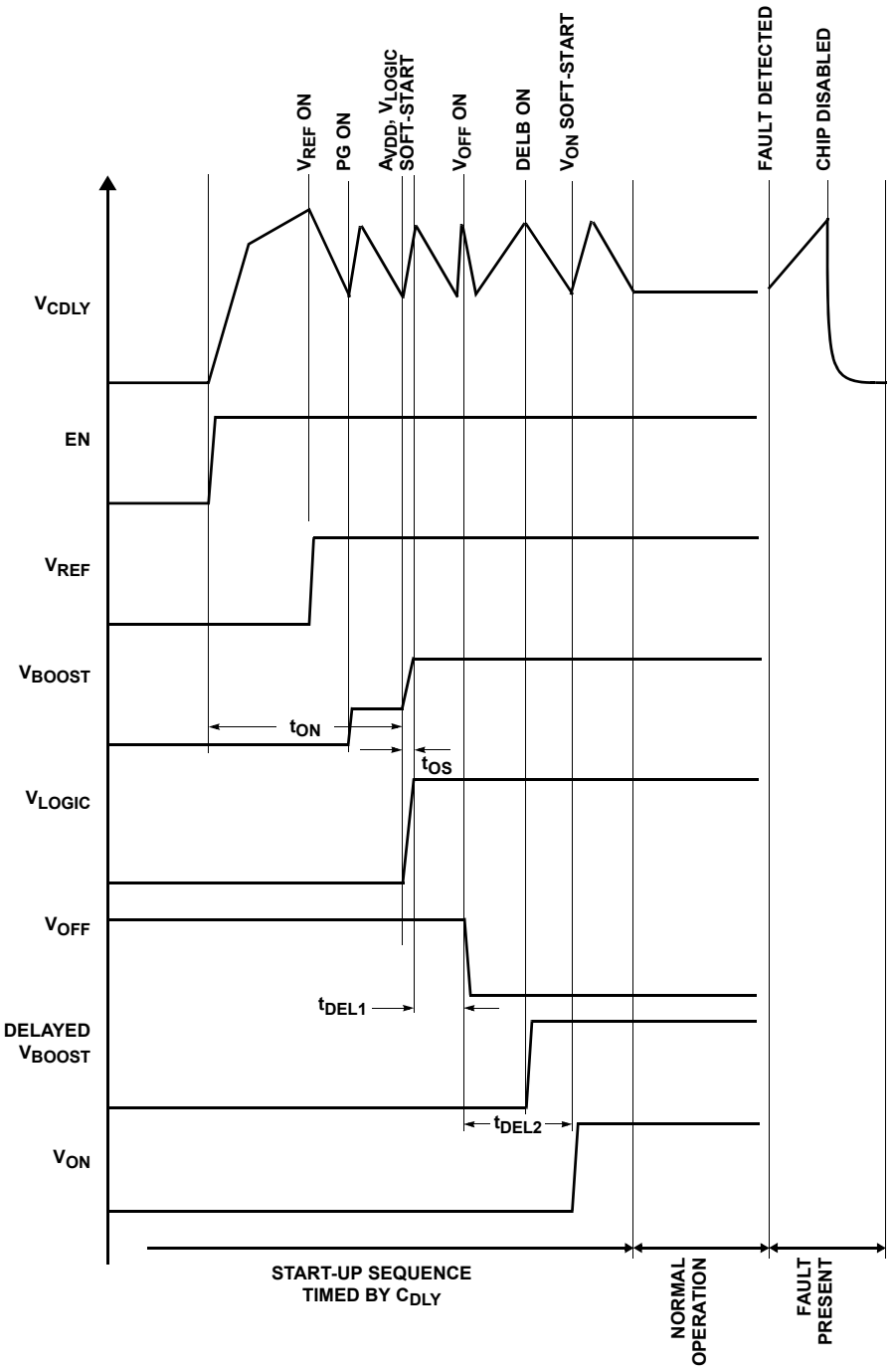


FIGURE 30. EL7520 START-UP SEQUENCE

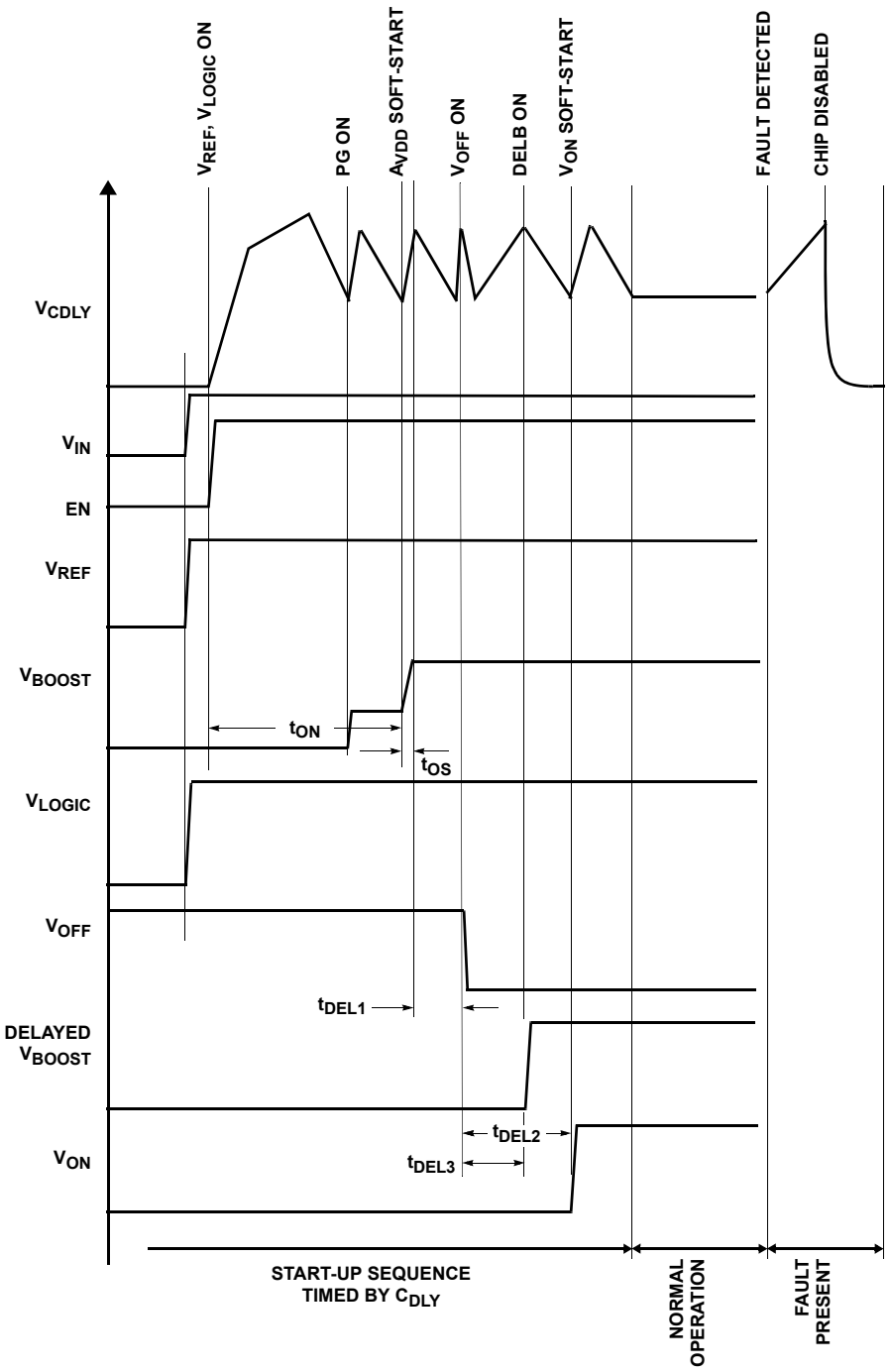


FIGURE 31. EL7520A START-UP SEQUENCE

Over-Temperature Protection

An internal temperature sensor continuously monitor the die temperature. In the event that the die temperature exceeds the thermal trip point, the device will shut down. The upper and lower trigger points are typically set to 130°C and -90°C respectively.

Layout Recommendation

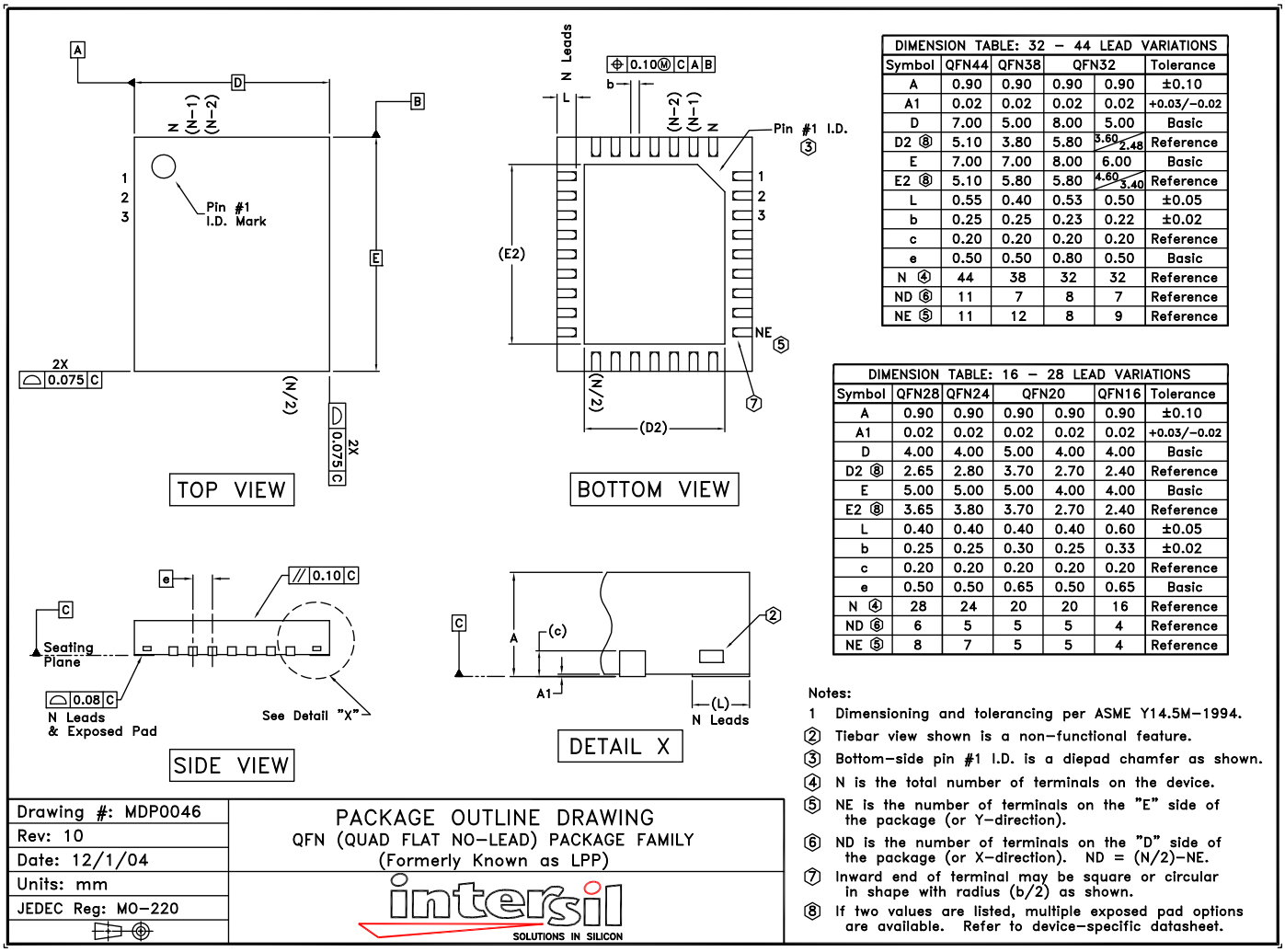
The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{REF} and V_{DD} bypass capacitors close to the pins.
3. Reduce the loop with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point.

A demo board is available to illustrate the proper layout implementation.

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	7.00	5.00	8.00	5.00	Basic
D2 (8)	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 (8)	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N (4)	44	38	32	32	Reference
ND (6)	11	7	8	7	Reference
NE (5)	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS					
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/–0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 (8)	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 (8)	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N (4)	28	24	20	20	16	Reference
ND (6)	6	5	5	5	4	Reference
NE (5)	8	7	5	5	4	Reference

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y–direction).
6. ND is the number of terminals on the "D" side of the package (or X–direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

Drawing #: MDP0046	PACKAGE OUTLINE DRAWING QFN (QUAD FLAT NO–LEAD) PACKAGE FAMILY (Formerly Known as LPP)
Rev: 10	
Date: 12/1/04	
Units: mm	
JEDEC Reg: MO–220	intersil SOLUTIONS IN SILICON

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

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