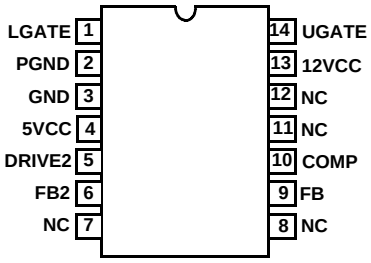
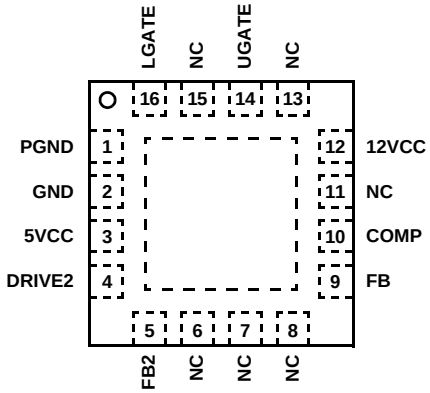
Pinouts

ISL6529, ISL6529A (SOIC)
TOP VIEW



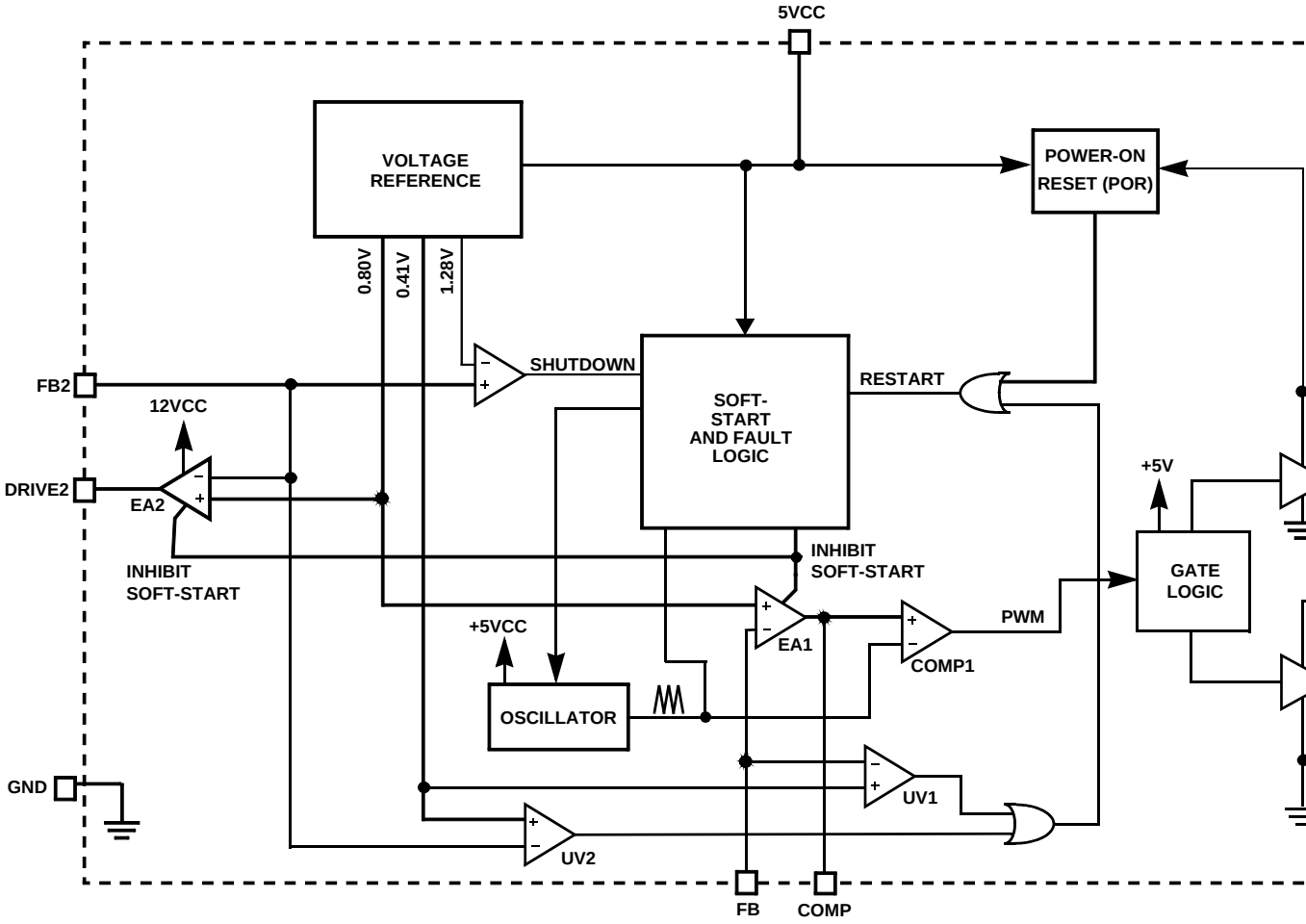
NC = NO INTERNAL CONNECTION

ISL6529, ISL6529A (QFN)
TOP VIEW

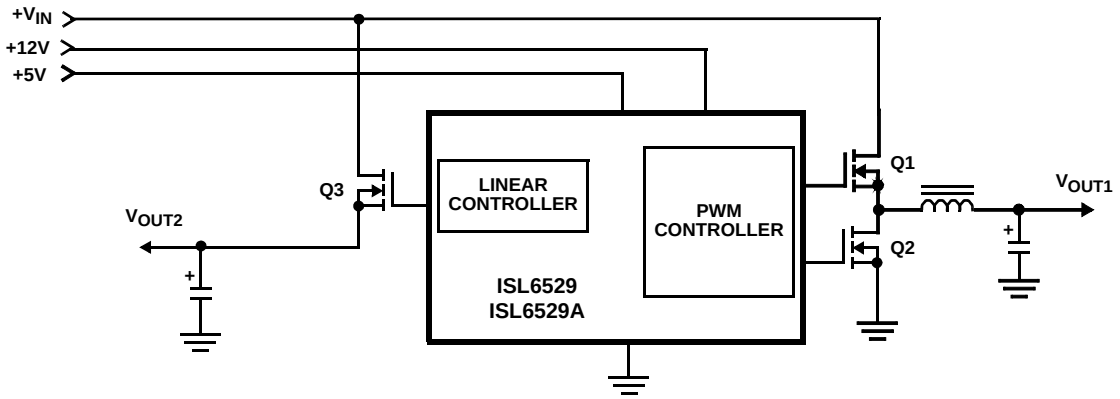


NC = NO INTERNAL CONNECTION

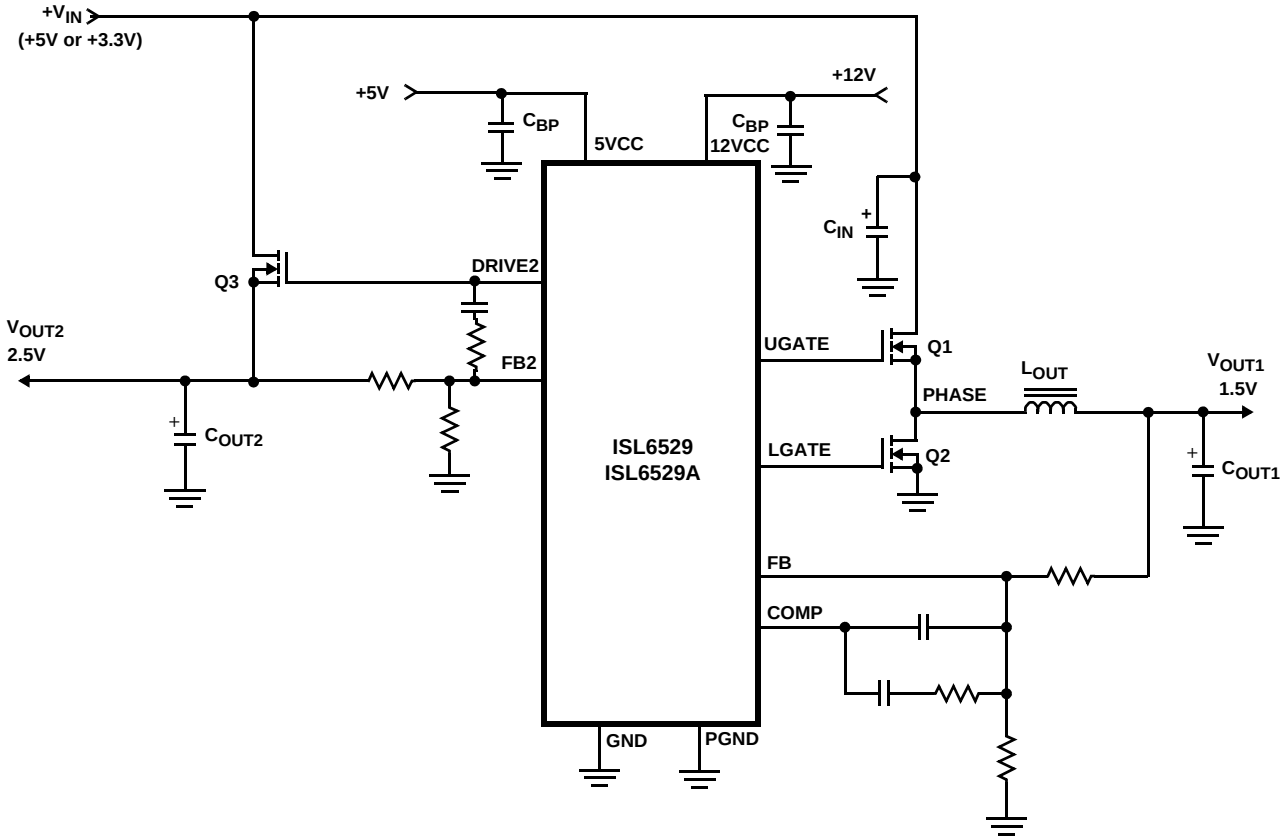
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

UGATE, LGATE, DRIVE2,. . . . . GND - 0.3V to 12VCC
5VCC . . . . . GND - 0.3V to +7V
12VCC . . . . . GND - 0.3V to +14V
FB, FB2, COMP, ... GND - 0.3V to 5VCC + 0.3V
ESD Classification . . . . . Class 4kV

Operating Conditions

Supply Voltage on 5VCC . . . . . +5V ±10%
Supply Voltage on 12VCC . . . . . +12V ±10%
Supply Voltage to drain of Upper MOSFETs . . . +3.3V to +5V ±10%
Ambient Temperature Range. . . . . 0°C to 70°C
Junction Temperature Range . . . . . 0°C to 125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	68	NA
QFN Package (Notes 2, 3).	36	5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current 12VCC	I_{CC}	UGATE, LGATE and DRIVE2 Open	-	2.7	3.0	mA
Nominal Supply Current 5VCC	I_{CC}	UGATE, LGATE and DRIVE2 Open	-	3.5	4.5	mA
POWER-ON RESET						
Rising 5VCC Threshold		12VCC = 12V	4.25	4.4	4.5	V
Falling 5VCCThreshold		12VCC = 12V	3.75	3.82	4.0	V
Rising 12VCC Threshold		5VCC = 5V	9.6	10.3	10.8	V
Falling 12VCCThreshold		5VCC = 5V	9.3	9.6	10.2	V
OSCILLATOR AND SOFT-START						
Free Running Frequency	F_{OSC}		550	600	650	kHz
Ramp Amplitude	DV_{OSC}		-	1.5	-	V_{P-P}
Soft-Start Interval	T_{SS}		3.1	3.45	3.75	ms
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}		-	0.800	-	V
System Accuracy		ISL6529C	-2.0	-	+2.0	%
		ISL6529AC	-1.0	-	+1.0	%
PWM CONTROLLER ERROR AMPLIFIER						
DC Gain		R_L = 10K, C_L = 10pF	-	80	-	dB
Gain-Bandwidth Product	GBWP	R_L = 10K, C_L = 10pF	-	15	-	MHz
Slew Rate	SR	R_L = 10K, C_L = 10pF	-	6	-	V/µs
FB Input Current	$\lvert I_I \rvert$	V_{FB} = 0.8V	-	20	150	nA
COMP High Output Voltage	V_{OUT} High		3.0	4.5	-	V
COMP Low Output Voltage	V_{OUT} Low		-	0.5	1.0	V
COMP High Output, Source Current	I_{OUT} High		-2.5	-6.8	-	mA

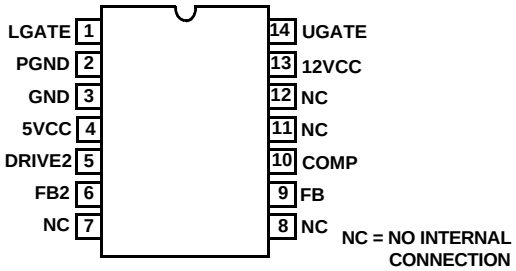
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
COMP Low Output, Sink Current	I_{OUT} Low		2.5	3.5	-	mA
Undervoltage Level (V_{FB}/V_{REF})	V_{UV}		-	51.5	-	%
PWM CONTROLLER GATE DRIVERS						
UGATE and LGATE Maximum Voltage	V_{HGATE}	12VCC = 12V	11	12	-	V
UGATE and LGATE Minimum Voltage	V_{LGATE}	12VCC = 12V	-	0	0.5	V
UGATE and LGATE Source Current	I_{GATE}	12VCC = 12V	-	-1	-	A
UGATE and LGATE Sink Current	I_{GATE}	12VCC = 12V	-	1	-	A
UGATE and LGATE OUTPUT IMPEDANCE	$R_{DS(on)}$	12VCC = 12V	-	3.1	4.3	Ω
LINEAR REGULATOR (DRIVE2)						
DC Gain		R_L = 10K, C_L = 10pF	-	80	-	dB
Gain-Bandwidth Product	GBWP	R_L = 10K, C_L = 10pF	-	15	-	MHz
Slew Rate	SR	R_L = 10K, C_L = 10pF	-	6	-	V/µs
FB2 Input Current	$\|I_I\|$	V_{FB2} = 0.8V	-	20	150	nA
Drive2 High Output Voltage	V_{OUT} High		9.5	10.3	-	V
Drive2 Low Output Voltage	V_{OUT} Low		-	0.1	1.0	V
Drive2 High Output Source Current	I_{OUT} High		-0.7	-1.4	-	mA
Drive2 Low Output Sink Current	I_{OUT} Low		0.85	1.2	-	mA
Over-Voltage Level (V_{FB2}/V_{REF})	V_{OV}	Percent of Nominal	-	160	-	%
Under-Voltage Level (V_{FB2}/V_{REF})	V_{UV}	Percent of Nominal	-	51.5	-	%
REGULATOR ISOLATION						
Change in Linear Regulator Output Voltage (Note 4)	ΔVout	Linear Output = 2.5V, 6A Load Change on PWM	-	<0.5	-	%
Change in PWM Regulator Output Voltage (Note 4)	ΔVout	PWM Output = 1.5V, 1A Load Change on Linear	-	<0.5	-	%

NOTE:

4. Measured in the evaluation board.

Functional Pin Descriptions



LGATE (Pin 1), (Pin 16 QFN)

Lower gate drive output. Connect to gate of the low-side MOSFET.

PGND (Pin 2), (Pin 1 QFN)

This pin is the power ground return for the lower gate driver.

GND (Pin 3), (Pin 2 QFN)

Signal ground for the IC. All voltage levels are measured with respect to this pin. Place via close to pin to minimize impedance path to ground plane.

5VCC (Pin 4), (Pin 3 QFN)

Provide a well decoupled 5V bias supply for the IC to this pin. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

DRIVE2 (Pin 5), (Pin 4 QFN)

Connect this pin to the gate terminal of an external N-Channel MOSFET transistor. This pin provides the gate voltage for the linear regulator pass transistor. It also provides a means of compensating the error amplifier for applications where the user needs to optimize the regulator transient response.

FB2 (Pin 6), (Pin 5 QFN)

Connect the output of the linear regulator to this pin through a properly sized resistor divider. The voltage at this pin is regulated to 0.8V. This pin is also monitored for undervoltage events.

Pulling and holding FB2 above 1.28V shuts down both regulators. Releasing FB2 initiates soft-start on both regulators.

NC (Pins 7, 8, 11, and 12), (Pins 6, 7, 8, 11, 13 and 15 QFN)

No internal connection.

FB (Pin 9), (Pin 9 QFN) and COMP (Pin 10), (Pin 10 QFN)

FB and COMP are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the standard synchronous rectified buck converter.

12VCC(Pin 13), (Pin 12 QFN)

Provides bias voltage for the gate drivers.The voltage at this pin is monitored for Power-On Reset (POR) purposes.

UGATE (Pin 14), (Pin 14 QFN)

Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the MOSFET.

Description

Operation Overview

The ISL6529 monitors and precisely controls two output voltage levels. Refer to the *Block Diagram, Simplified Power System Diagram*, and *Typical Application Schematic* on pp. 2–3. The controller is intended for use in graphics cards or embedded processor applications with 5V and 12V bias input available. The IC integrates both a standard buck PWM controller and a linear controller. The PWM controller is designed to regulate the high current GPU voltage (V_{OUT1}). The PWM controller regulates the output voltage to a level programmed by a resistor divider. The linear controller is designed to regulate the lower current local memory voltage (V_{OUT2}) through an external N-Channel MOS pass transistor.

Initialization

The ISL6529 automatically initializes upon application of input power. Special sequencing of the input supplies is not necessary. The POR function continually monitors the input bias supply voltage at the 5VCC and 12VCC pins. The POR function initiates soft-start operation after these supply voltages exceed their POR threshold voltages.

Soft-Start

The POR function initiates the digital soft-start sequence. Both the linear regulator error amplifier and PWM error amplifier reference inputs are forced to track a voltage level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator regulates the output relative to the tracked soft-start voltage, slowly charging the output capacitor(s). Simultaneously, the linear output follows the smooth ramp of the soft-start function into normal regulation.

Figure 1 shows the soft-start sequence of an ISL6529 evaluation board powered by an ATX supply. Note the uniform linear output voltage rise of the two ISL6529 output voltages. Once the voltage on 5VCC crosses the POR thresholds, both outputs begin their soft-start sequence. The triangle waveform from the PWM oscillator is compared to the rising error amplifier output voltage. As the error amplifier voltage increases, the pulse-width on the PWM increases to reach its steady-state duty cycle. The error amplifier reference of the linear controller also rises relative to the soft-start reference.

Figure 2 shows the controlled stepped output voltage rise and associated charging current of a 390µF polymer capacitor. By providing many small steps of current that effectively charge the output capacitor, the potentially large peak current resulting from a sudden, uncontrolled voltage rise is eliminated.

The clock for the DAC producing the 30mV steps is approximately 18.5kHz, so there is a 18.5kHz ripple current component that lasts for the approximate 2.8ms start-up interval. A few clock cycles are used for initialization to insure that soft-start begins near zero volts.

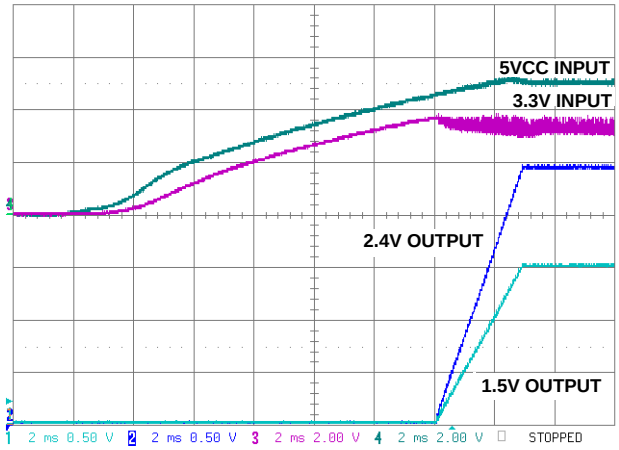


FIGURE 1. ATX SUPPLY POWERING AN ISL6529 EVALUATION BOARD

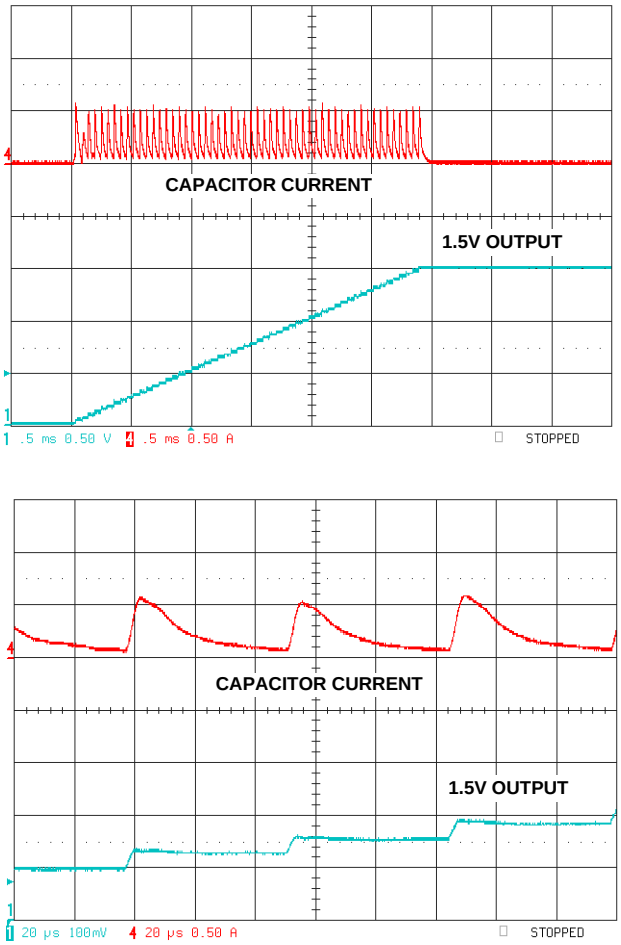


FIGURE 2. TOP SCOPE TRACES ARE VOLTAGE RAMP AND CAPACITOR CURRENT. LOWER TRACES ARE TIME AND VOLTAGE EXPANSION OF UPPER SCOPE TRACES.

Undervoltage Protection

The FB and FB2 pins are monitored during converter operation by two separate undervoltage (UV) comparators. If the FB voltage drops below 51.5% of the reference voltage (0.41V), a fault signal is generated. The internal fault logic shuts down both regulators simultaneously when the fault signal triggers a restart.

Figure 3 illustrates the protection feature responding to a UV event on V_{OUT1}. At time t0, VOUT1 has dropped below 51.5% of the nominal output voltage. Both outputs are quickly shut down and the internal soft-start function begins producing soft-start ramps. The delay interval, t0 to t3, seen by the output is equivalent to three soft-start cycles. After a short delay interval of 10.5ms, the fourth internal soft-start cycle initiates a normal soft-start ramp of the output, at time t3. Both outputs are brought back into regulation by time t4, as long as the UV event has cleared.

Had the cause of the UV still been present after the delay interval, the UV protection circuitry becomes active approximately 875ms into the soft-start interval. A fault signal could then be generated and the outputs once again shut down. The resulting hiccup mode style of protection would continue to repeat indefinitely.

Output Voltage Selection

The output voltage of the PWM converter can be programmed to any level between V_{IN} (i.e. +3.3V) and the internal reference, 0.8V. An external resistor divider is used to scale the output voltage relative to the reference voltage and feed it back to the inverting input of the error amplifier (see Figure 4).

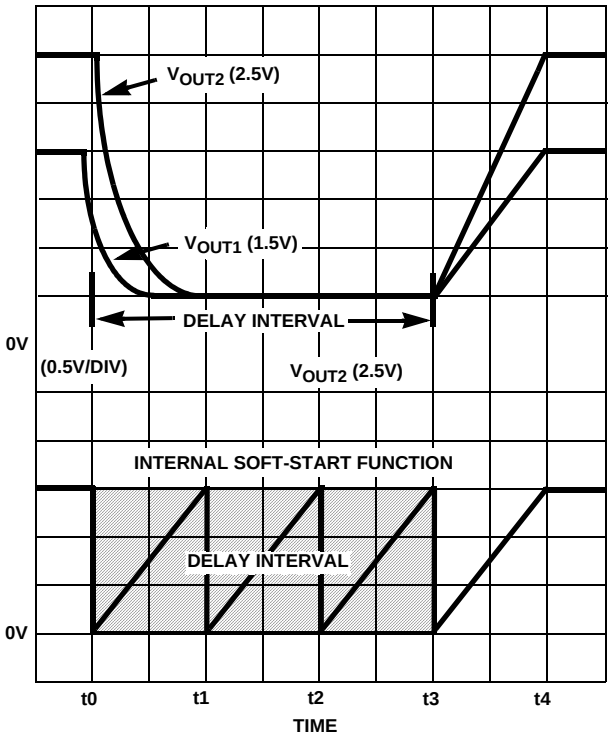


FIGURE 3. UNDERVOLTAGE PROTECTION RESPONSE

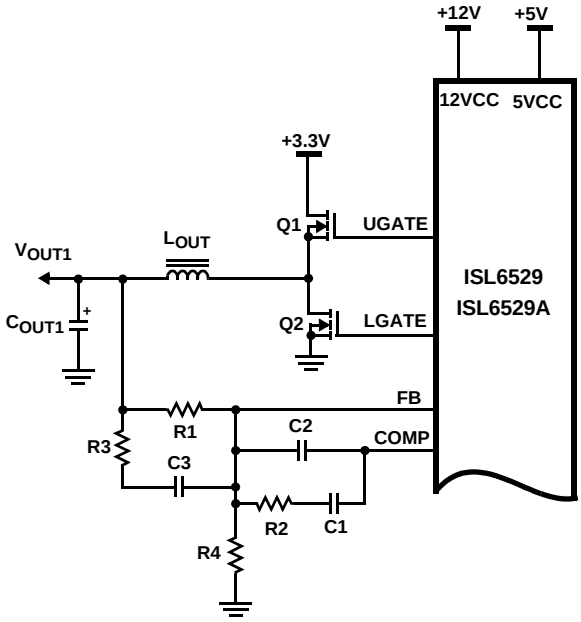


FIGURE 4. OUTPUT VOLTAGE SELECTION OF THE PWM

However, since the value of R1 affects the values of the rest of the compensation components, it is advisable to keep its value less than 5kΩ. Depending on the value chosen for R1, R4 can be calculated based on the following equation:

$$R4 = \frac{R1 \times 0.8V}{V_{OUT1} - 0.8V} \quad \text{(EQ. 1)}$$

If the output voltage desired is 0.8V, simply route VOUT1 back to the FB pin through R1, but do not populate R4.

The linear regulator output voltage is also set by means of an external resistor divider as shown in Figure 5. The two resistors used to set the output voltage should not exceed a parallel equivalent value, referred to as R_{FB}, of 5kΩ. This restriction is due to the manner of implementation of the soft-start function. The following relationship must be met:

$$R_{FB} = \frac{R5 \times R6}{R5 + R6} < 5k\Omega \quad \text{(EQ. 2)}$$

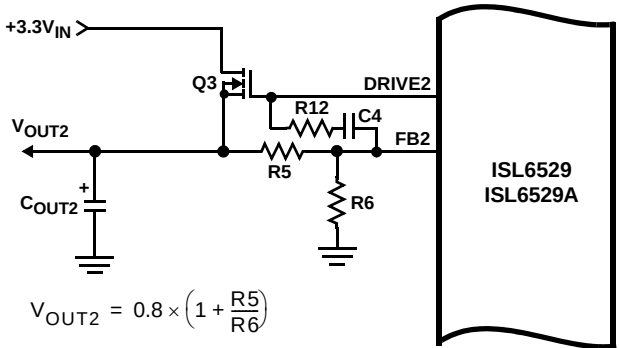


FIGURE 5. OUTPUT VOLTAGE SELECTION OF THE LINEAR

To ensure the parallel combination of the feedback resistors meets this criteria, choose a target value for R_{FB} of less than 5kΩ and then apply the following equations:

$$R5 = \frac{V_{OUT2}}{V_{REF}} \times R_{FB} \quad \text{(EQ. 3)}$$

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT2} - V_{REF}} \quad \text{(EQ. 4)}$$

where V_{OUT2} is the desired linear regulator output voltage and V_{REF} is the internal reference voltage, 0.8V. For an output voltage of 0.8V, simply populate R5 with a value less than 5kΩ and do not populate R6.

Converter Shutdown

Pulling and holding the FB2 pin above a typical threshold of 1.28V will shut down both regulators. Upon release of the FB2 pin, the regulators enter into a soft-start cycle which brings both outputs back into regulation.

PWM Controller Feedback Compensation

A simplified representation of the voltage-mode control loop used for output regulation by the converter is shown in Figure 6. The output voltage, V_{OUT}, is fed back to the negative input of the error amplifier which is regulated to the reference voltage level, V_{REF}. The error amplifier output, $V_{E/A}$, is compared with the triangle wave produced by the oscillator, V_{OSC}, to provide a pulse-width modulated (PWM) signal from the PWM comparator. This signal is then used to switch the MOSFET and produce a PWM waveform with an amplitude of V_{IN} at the PHASE node. The square-wave PHASE voltage is then smoothed by the output filter, L_{OUT} and C_{OUT}, to produce a DC voltage level.

The modulator transfer function is defined as $V_{OUT}/V_{E/A}$. The internal PWM comparator and driver circuits equate to a DC gain block dominated by the supply voltage, V_{IN}, divided by the peak-to-peak magnitude of the triangle wave, ΔV_{OSC}. The output filter components, L_{OUT} and C_{OUT}, shape the overall modulator small-signal transfer function by contributing a double pole break frequency at F_{LC} and a zero at F_{ESR}.

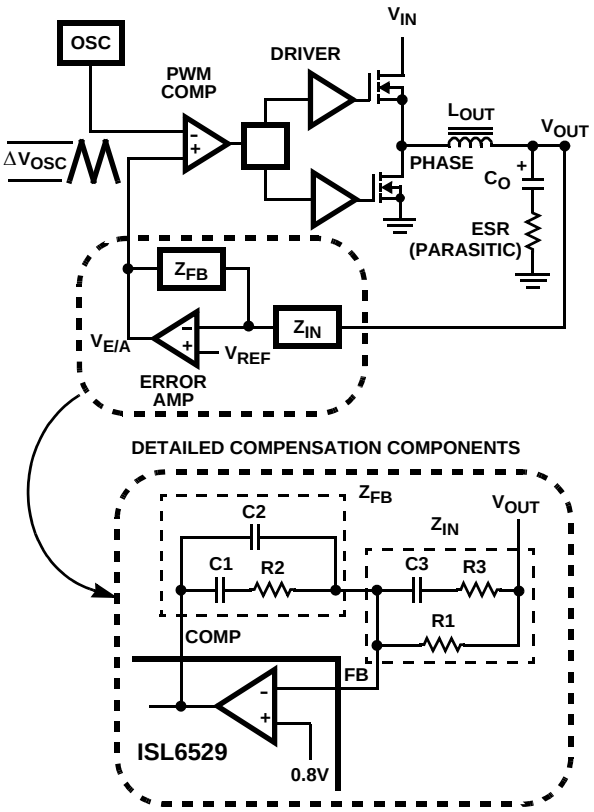


FIGURE 6. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad \text{(EQ. 5)}$$

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(EQ. 6)}$$

The compensation network consists of the error amplifier and the impedance networks Z_{IN} and Z_{FB}. They provide the link between the modulator transfer function and a controllable closed loop transfer function of V_{OUT}/V_{REF}. The goal of component selection for the compensation network is to provide a loop gain with high 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees.

Compensation Break Frequency Equations

Poles:

$$F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)} \quad \text{(EQ. 8)}$$

$$F_{P2} = \frac{1}{2\pi \times R3 \times C3} \quad \text{(EQ. 9)}$$

Zeros:

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \quad \text{(EQ. 10)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \quad \text{(EQ. 11)}$$

Follow this procedure for selecting compensation components by locating the poles and zeros of the compensation network:

1. Set the loop gain (R2/R1) to provide a converter bandwidth of one quarter of the switching frequency.
2. Place the first compensation zero, F_{Z1}, below the output filter double pole (~75% F_{LC}).
3. Position the second compensation zero, F_{Z2}, at the output filter double pole, F_{LC}.
4. Locate the first compensation pole, F_{P1}, at the output filter ESR zero, F_{ESR}.
5. Position the second compensation pole at half the converter switching frequency, F_{SW}.
6. Check gain against error amplifier's open-loop gain.
7. Estimate phase margin; repeat if necessary.

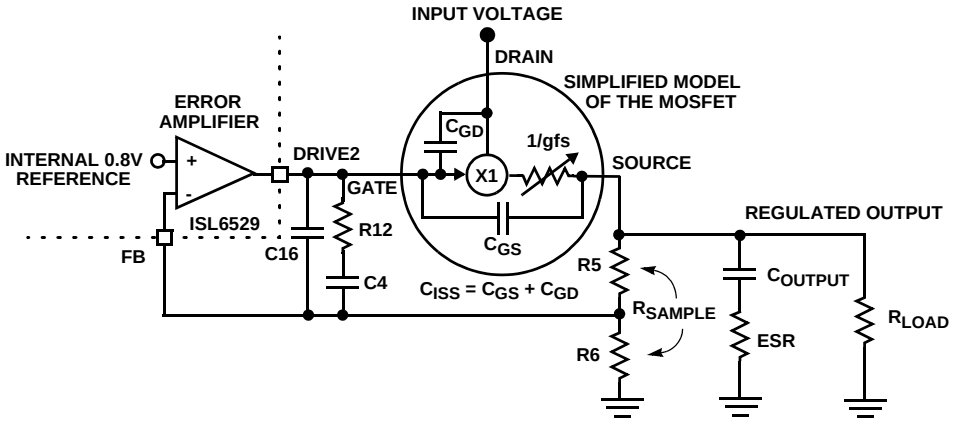


FIGURE 7. FIGURE A. SIMPLIFIED DIAGRAM OF THE LINEAR VOLTAGE REGULATOR

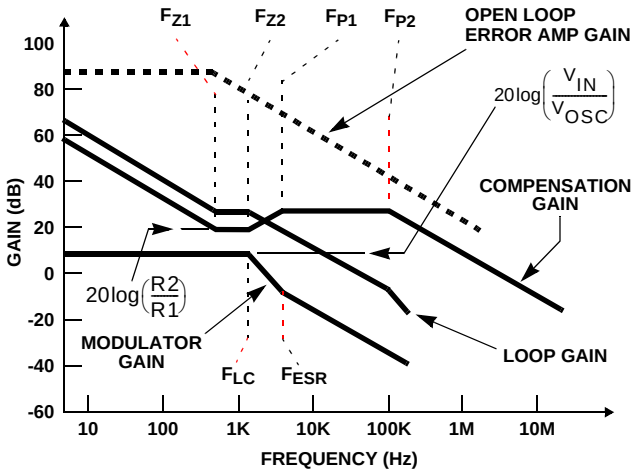


FIGURE 8. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Figure 8 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual modulator gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown in Figure 8. Using the above procedure should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

Linear Regulator Compensation

The linear regulator in the ISL6529 is not internally compensated and therefore allows the user to optimize regulator performance with regard to transient load response. Although the compensation network shown in the application examples in this data sheet provide conservative compensation for a variety of loads, performance can be enhanced with attention to load requirements.

Low ESR capacitors can cause stability concerns in discrete IC regulators. Even regulators that are internally compensated can become unstable when these capacitors are placed across their output. There have been suggestions to add series resistance to these capacitors to stabilize the regulator. This approach seems self defeating and throws away a desirable quality.

Component Considerations

Many unsuspected poles and zeros develop with the selection of external components and operating conditions like output MOSFET transistors, output filter capacitors and load current. These elements will be discussed beginning with the influence of the MOSFET series output resistance, the 1/gfs term shown in Figure 7. At low load currents and low transconductance, the effective output resistance can be as high as several kilohms. The low MOSFET gfs with accompanying high series resistance and large values of output capacitance form a low frequency pole that for many cases becomes the dominate pole in the system and often results in a stable no load system. As the load current is increased, the MOSFET series output resistance is reduced and moves the output pole into a higher frequency region, adding phase shift that can result in a marginally stable or unstable system.

Low output capacitor ESR can result in stability problems as mentioned above. In contrast, high output capacitor ESR can improve the system stability. The capacitor and its series resistance function as a zero, often canceling other poles in the loop. Figure 9 shows a system simulation with a 300µF, 100mΩ high ESR output capacitor. A single 10pF capacitor from input to output of the error amplifier stabilizes the system for load currents through the 1mA to 3A range.

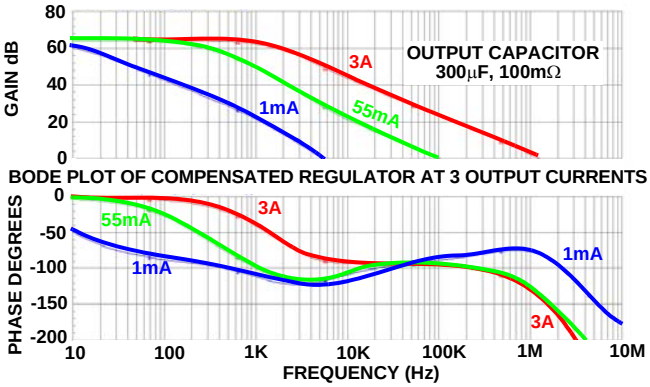


FIGURE 9. LOOP RESPONSE WITH ONLY C16 = 10pF COMPENSATION

Contrast this with Figure 10 that shows a Bode plot of simulations of this regulator operating with a 100µF, 5mΩ low ESR output capacitor. Note the phase approaching 180° at high current. This is in contrast to the response previously shown with the 300µF high ESR capacitor. The 300µF output capacitor and its ESR provide phase lead to cancel or offset the pole formed with the MOSFET output resistance and 300µF capacitance. Also notice that system stability varies widely with load current. A system can oscillate at no load and be stable at full load, The converse is also possible. Oscillation can also occur at load currents between the current extremes.

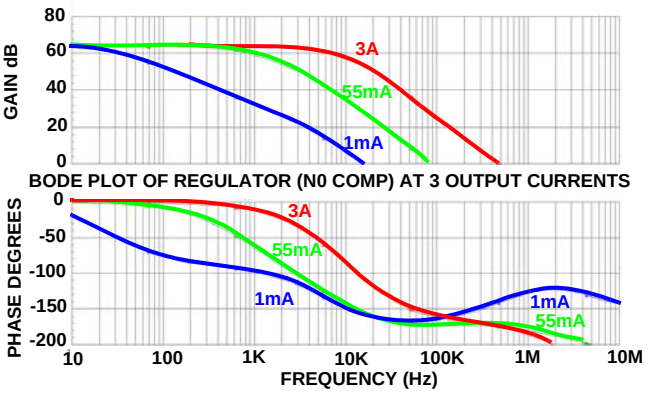


FIGURE 10. LOOP RESPONSE WITH ONLY 100µF, 5mΩ OUTPUT CAPACITOR

The Compensation Network

To provide for system stability with a low ESR output capacitor, where pole cancellation by the capacitor is outside the frequencies of interest, a phase lead network must be used to compensate for the phase lag resulting from MOSFET output resistance and the output capacitor.

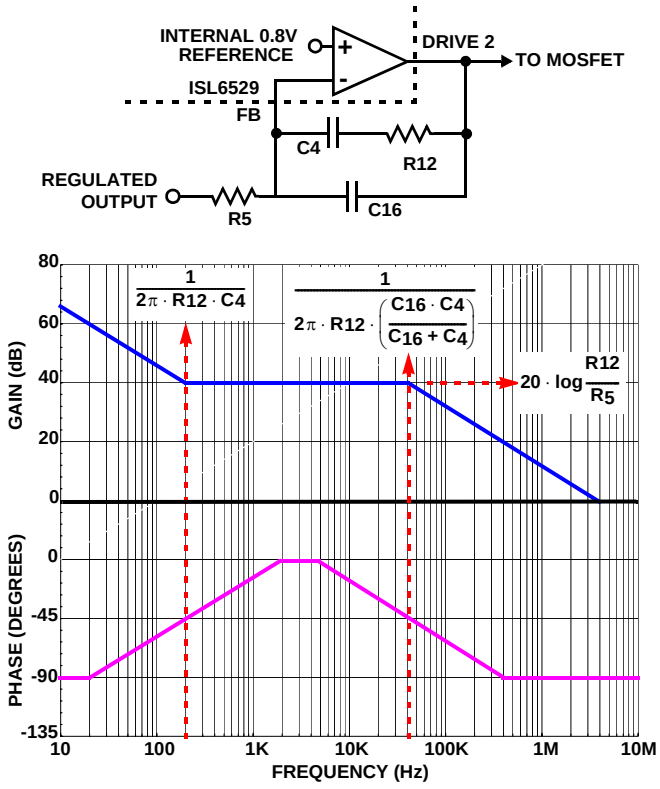


FIGURE 11. SCHEMATIC AND BODE PLOT OF COMPENSATION NETWORK

Figure 11 shows the type II compensation network configuration and a simplified straight line representation of the network response. By using the equations in Figure 11, the values of R12 and C4 can be adjusted to the frequency where phase lead begins. The second equation shows the upper frequency where phase advance is complete. After capacitor C4 becomes effectively an ac short, the mid band gain is set by the R12/R5 ratio as shown on Figure 11.

Several simulations illustrate the compensation with the more difficult 5mΩ, 100µF output capacitor. Figure 10 previously showed the Bode plots where the phase response comes dangerously near the oscillatory 180° state at unity gain. A type II network applied across the error amplifier inverting input to the output can be configured to perform this function.

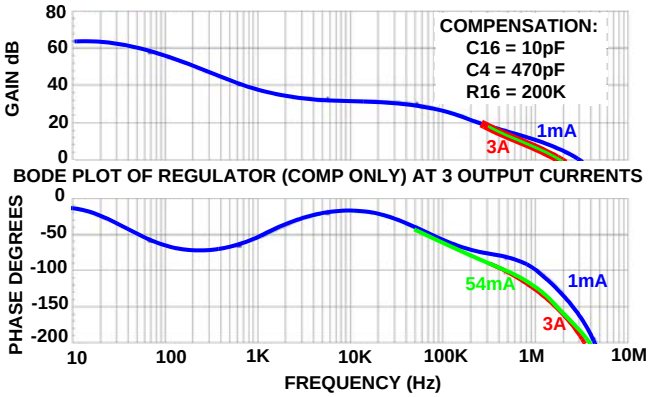


FIGURE 12. LOOP RESPONSE WITH COMPENSATION NETWORK ONLY

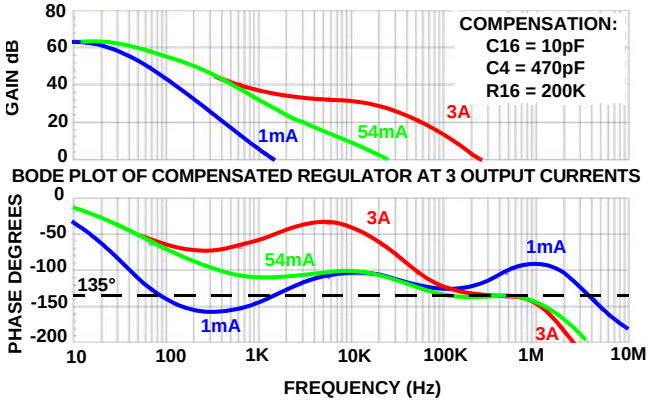


FIGURE 13. INVERTING INPUT TO OUTPUT GAIN AND PHASE WITH COMPENSATION AND 100µF, 5mΩ OUTPUT CAPACITOR

Figure 12 shows the Bode plot of only the compensation network with the system to illustrate the phase boost in the system. Essentially the phase lead region must be moved to advance the phase where it is close to an oscillatory state. Increasing the value of C4 moves the response lower, aiding the lagging phase at low frequencies and low load current. This operation will reduce phase compensation at higher

frequencies and high load current. Figure 13 shows the results of the complete system with output capacitor and compensation network for 45° of phase margin.

Because of the large variety of capacitors, varying ESRs and PC board layouts, Table 1, based upon system simulations is provided as a starting point guide to aid in the selection of compensation networks for output capacitors values of 1µF, 10µF, 100µF and 1000µF with ESR values of 5mΩ, 30mΩ and 100mΩ for each capacitor value. The frequencies associated with the compensation elements are also shown to aid in component selection.

Parallel capacitors of the same value and type can be treated as a combination. For example three 100µF, 10mΩ capacitors may be treated as one 300µF, 3.3mΩ capacitor. Mixed capacitors require more attention. For example the compensation for a 1000µF, low ESR capacitor will suffice for a shunting 10µF, low ESR capacitor.

TABLE 1. COMPENSATION NETWORKS FOR LINEAR REGULATOR

CAP ESR	DETAIL	OUTPUT CAPACITOR			
		1µF	**10µF**	**100µF**	**1000µF**
5mΩ	**Comp Network**	C16 = 10pF R12 = 47K C4 = 200pF	C16 = 10pF R12 = 47K C4 = 470pF	C16 = 10pF R12 = 200K C4 = 470pF	C16 = 10pF R12 = 470K C4 = 470pF
	Low Fq Zero (C4 & R12)	17kHz	7.2kHz	1.7kHz	720Hz
	High Fq Pole (C16 & R12)	338kHz	338kHz	80kHz	34kHz
	MidbandGain R12/R5	20dB	20dB	33dB	40dB
	OUTPUT CAP & ESR Zero Fq	32MHz	3.2MHz	320kHz	32kHz
30mΩ	**Comp Network**	C16 = 10pF R12 = 47K C4 = 200pF	C16 = 10pF R12 = 47K C4 = 470pF	C16 = 10pF R12 = 200K C4 = 470pF	C16 = 10pF
	Low Fq Zero (C4 & R12)	17kHz	17kHz	1.7kHz	-
	High Fq Pole (C16 & R12)	338kHz	338kHz	80kHz	-
	Midband Gain R12/R5	20dB	20dB	33dB	-
	OUTPUT Cap & ESR Zero Fq	5.3MHz	530kHz	53kHz	5.3kHz
100mΩ	**Comp Network**	C16 = 10pF R12 = 47K C4 = 200pF	C16 = 10pF R12 = 47K C4 = 470pF	C16 = 10pF	C16= 10pF
	Low Fq Zero (C4 & R12)	17kHz	17kHz	-	-
	High Fq Pole (C16 & R12)	338kHz	338kHz	-	-
	Midband Gain R12/R5	20dB	20dB	-	-
	OUTPUT Cap & ESR Zero Fq	1.6MHz	160kHz	16kHz	1.6kHz

The final test for a system is transient load current performance. Ringing or oscillation indicates that the compensation network must be adjusted to assure stable operation with component and environmental variations. Figures 14 and 15 are scope shots that show the regulator with only with a 1500µF, 100mΩ capacitor with high frequency ringing with no compensation. A 27pF capacitor, C16 was added in Figure 15. The output step is about 260mV for the 3A load current for an ESR in the order of 90mΩ. After the load current is removed, the output network parasitics ring for about 5µs.

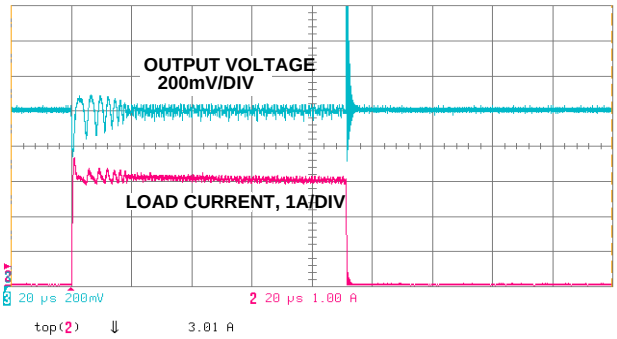


FIGURE 14. 3A TRANSIENT LOAD APPLIED TO THE REGULATOR NO COMPENSATION

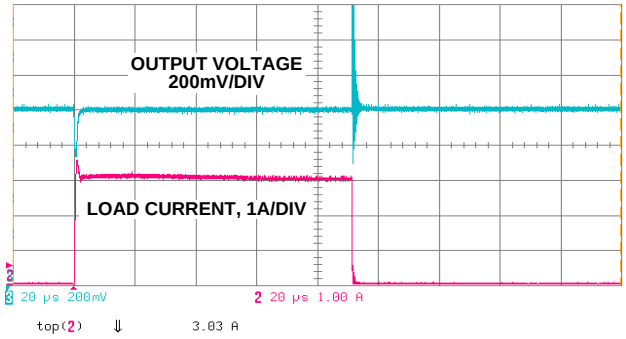


FIGURE 15. 3A TRANSIENT LOAD APPLIED TO THE REGULATOR 27pF COMPENSATION

Application Guidelines

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 600kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component layout and printed circuit board design minimizes the voltage spikes in the converters.

As an example, consider the turn-off transition of the PWM MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET and parasitic diode. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using the ISL6529, ISL6529A. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 16 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections through vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to the output inductor short. The power plane should support the input and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase node. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the UGATE pin to the MOSFET gate should be kept short and wide enough to easily handle the 1A of drive current.

The switching components should be placed close to the ISL6529, ISL6529A first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper MOSFET and lower diode and the load.

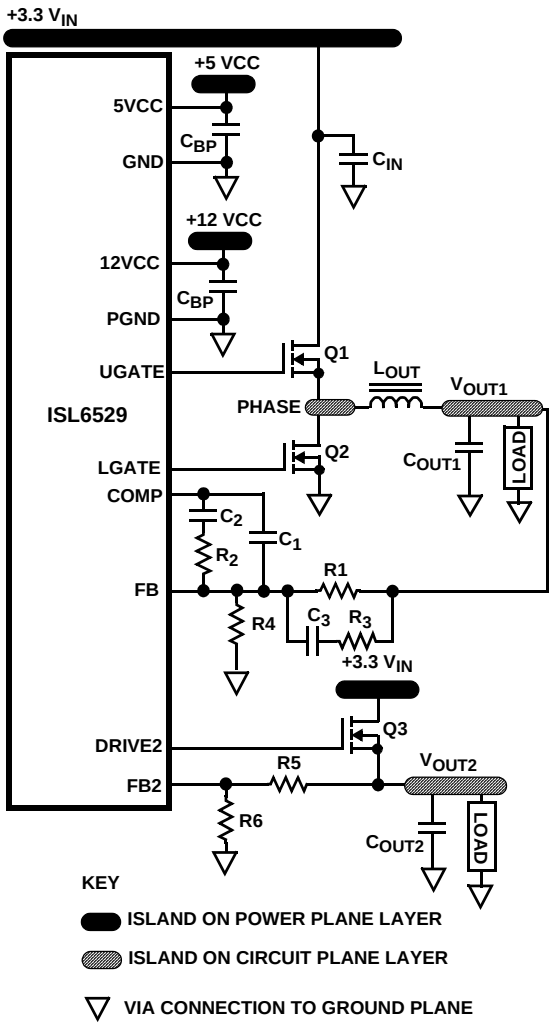


FIGURE 16. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Position the bypass capacitors, C_{BP}, close to the VCC pin with a via directly to the ground plane. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors for both regulators should also be located as close as possible to the relevant FB pin with vias tied straight to the ground plane as required.

Component Selection Guidelines

Output Capacitor Selection

Output capacitors are required to filter the output and supply the load transient current. The filtering requirements are a function of switching frequency and output current ripple. The load transient requirements are a function of the transient load current slew rate (di/dt) and magnitude. These requirements are generally met with a mix of capacitors and careful layout.

PWM Regulator Output Capacitors

Modern digital ICs can produce high transient load slew rates. High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor selection is generally determined by the effective series resistance (ESR) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Specialized low-ESR capacitors intended for switching-regulator applications are recommended for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient edge. Aluminum electrolytic, tantalum, and special polymer capacitor ESR values are related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

PWM Output Inductor Selection

The PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter response time to a load transient. The inductor value determines the converter's ripple current and the ripple voltage is also a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 11)}$$

$$\Delta V_{OUT} = \Delta I \times ESR \quad \text{(EQ. 12)}$$

Increasing the value of inductance reduces the output ripple current and voltage ripple. However, increasing the inductance value will slow the converter response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to slew the inductor current. Given a sufficiently fast control loop design, the ISL6529 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time

interval required to slew the inductor current from an initial current value to the final current level. During this interval the difference between the inductor current and the load current must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 13)}$$

$$t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \quad \text{(EQ. 14)}$$

where I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load.

With a +3.3V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 of the summation of the DC load current.

Use a mix of input bypass capacitors to control the voltage overshoot across the switching MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances. Connect them directly to ground with a via placed very close to the ceramic capacitor footprint.

For a through-hole design, several aluminum electrolytic capacitors may be needed. For surface mount designs, tantalum or special polymer capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up.

TRANSISTOR SELECTION/CONSIDERATIONS

The ISL6529, ISL6529A require three external transistors. One N-Channel MOSFET is used as the upper switch in a standard buck topology PWM converter. Another MOSFET is used as the lower synchronous switch. The linear controller drives the gate of an N-Channel MOS transistor used as the series pass element. The chosen MOSFET $r_{DS(ON)}$ determines the maximum drop out voltage of the regulator. For all practical purposes, the MOSFET appears as a variable resistor. All he MOSFET transistors should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

Upper MOSFET SWITCH Selection

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses account for a large portion of the power dissipation of the upper MOSFET. Switching losses also contribute to the overall MOSFET power loss.

$$P_{ConductionUpper} \cong I_o^2 \times r_{DS(on)} \times D \quad \text{(EQ. 15)}$$

$$P_{Switching} \cong \frac{1}{2} I_o \times V_{IN} \times t_{SW} \times F_{SW} \quad \text{(EQ. 16)}$$

where I_o is the maximum load current, D is the duty cycle of the converter (defined as V_O/V_{IN}), t_{SW} is the switching interval, and F_{SW} is the PWM switching frequency.

The lower MOSFET has only conduction losses since it switches with zero voltage across the device. Conduction loss is:

$$P_{ConductionLower} \cong I_o^2 \times r_{DS(on)} \times (1 - D) \quad \text{(EQ. 17)}$$

These equations assume linear voltage-current transitions and are approximations. The gate-charge losses are dissipated by the ISL6529 and do not heat the MOSFET. However, large gate-charge increases the switching interval, t_{SW}, which increases the upper MOSFET switching losses. Ensure that the MOSFET is within its maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature, air flow, and load current requirements.

The gate drive to the switching transistors ranges from slightly below 12V to ground. Because of the large voltage swing, logic-level transistors are not necessary in this application.

However, if logic-level transistors or transistors with low $V_{GS(on)}$ are used, close attention to layout guidelines should be exercised, as the low gate threshold could lead to some shoot-through despite counteracting circuitry present aboard the ISL6529.

N-Channel MOSFET Transistor Selection

The main criteria for selection of the linear regulator pass transistor is package selection for efficient removal of heat. Select a package and heatsink that maintains the junction temperature below the rating with a maximum expected ambient temperature.

The power dissipated in the linear regulator is:

$$P_{LINEAR} \cong I_O \times (V_{IN} - V_{OUT}) \quad \text{(EQ. 18)}$$

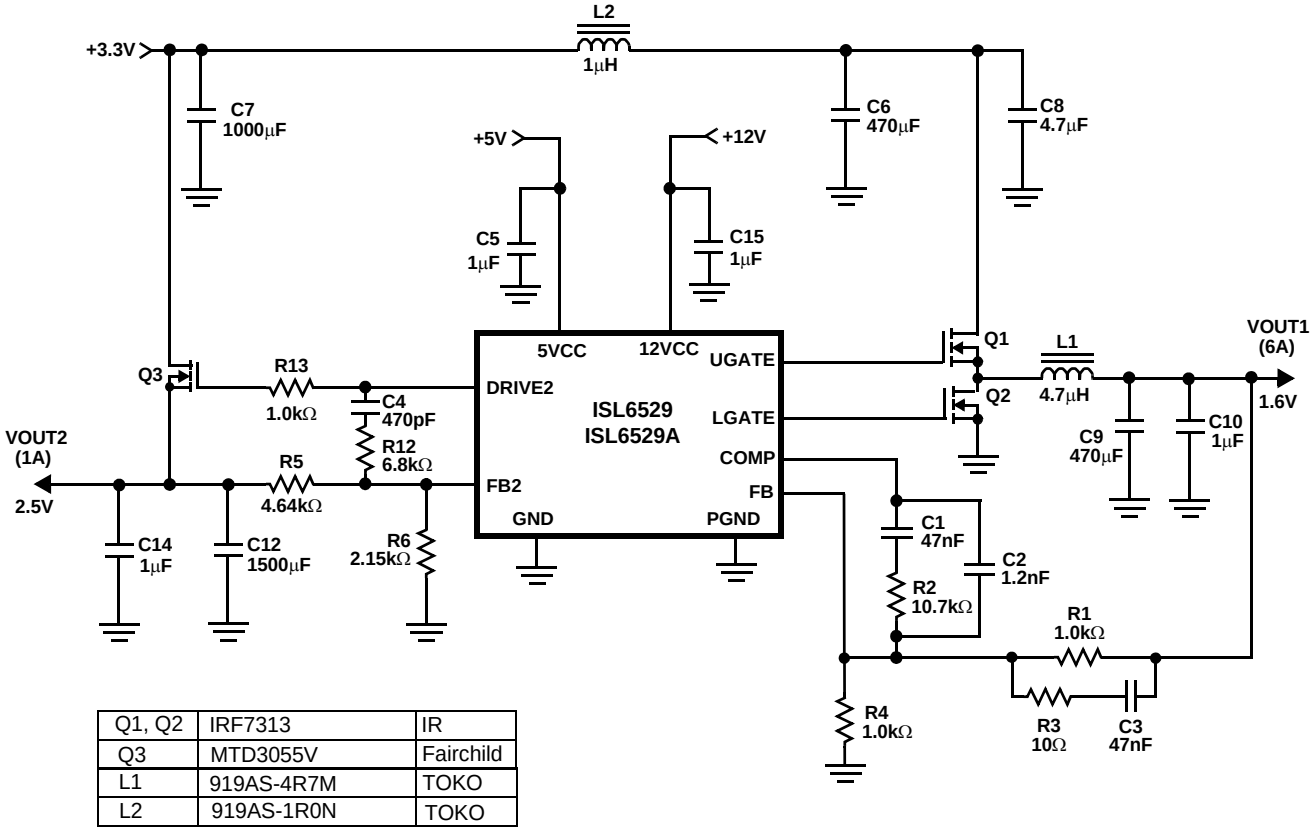
where I_O is the maximum output current and V_{OUT} is the nominal output voltage of the linear regulator.

References

Intersil documents are available on the web at http://www.intersil.com.

[1] Technical Brief, Intersil Corporation, TB417, http://www.intersil.com/data/tb/tb417.pdf

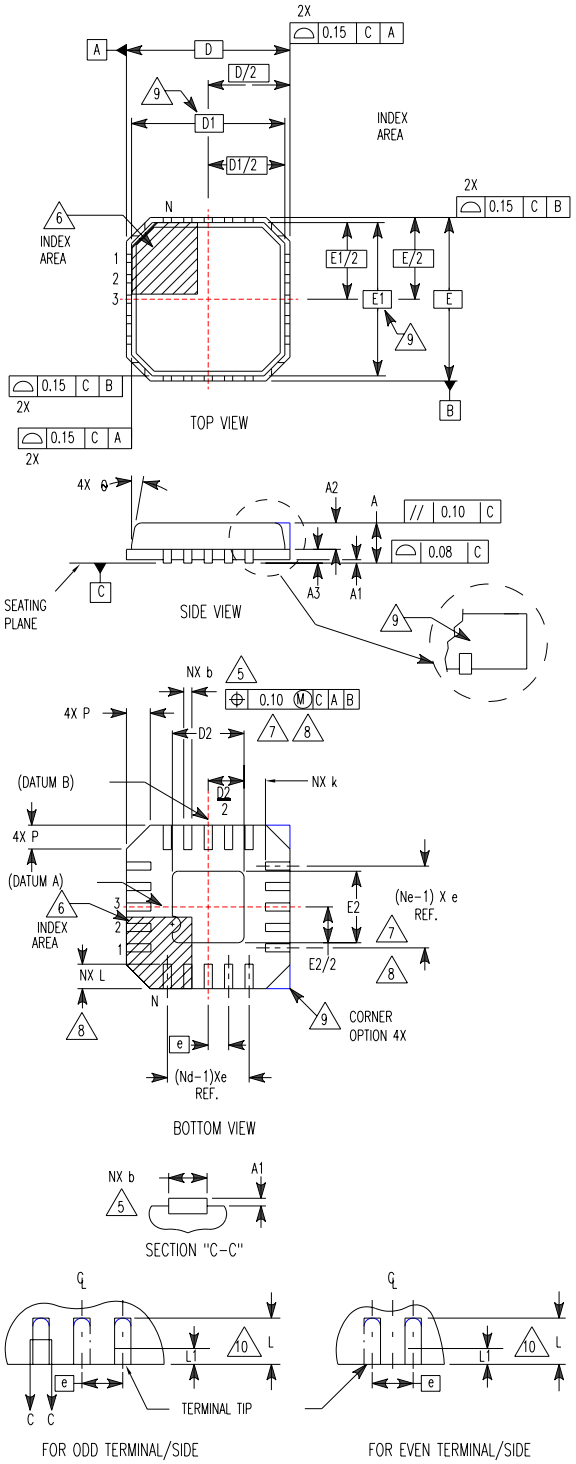
ISL6529 Converter Application Circuit



Q1, Q2	IRF7313	IR
Q3	MTD3055V	Fairchild
L1	919AS-4R7M	TOKO
L2	919AS-1R0N	TOKO

FIGURE 17. POWER SUPPLY APPLICATION CIRCUIT FOR A GRAPHICS CONTROLLER

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

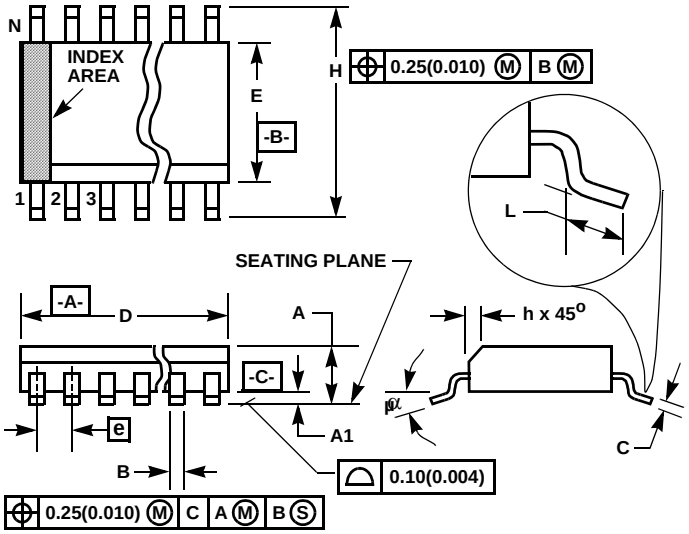
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

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