Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
V_{CC}, V_{DD} to GND .....-0.3V to +6V
SYSPOK, IMVPOK, $\overline{CLKEN}$ to GND .....-0.3V to +6V
$\overline{DPSLP}$, SUS, D0–D5 to GND .....-0.3V to +6V
REF, ILIM, CSP, CSN to GND.....-0.3V to (V_{CC} + 0.3V)
FB, POS, NEG, OAIN+, CC
OAIN- to GND.....-0.3V to (V_{CC} + 0.3V)
B0–B2, S0–S2, TON,
TIME to GND .....-0.3V to (V_{CC} + 0.3V)
DL, $\overline{DDO}$, to PGND.....-0.3V to (V_{DD} + 0.3V)
DH to LX.....-0.3V to (V_{BST} + 0.3V)
$\overline{SHDN}$ to GND.....-0.3 to +18V
BST to GND .....-0.3 to +36V
LX to BST.....-6V to +0.3V
GND to PGND .....-0.3V to +0.3V
REF Short-Circuit Duration .....Continuous
Continuous Power DIssipation
40-Pin 6mm × 6mm Thin QFN
(derate 26.3mW/°C above +70°C).....2105mW
Operating Temperature Range .....-40°C to +100°C
Junction Temperature.....+150°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0= S0 = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery Voltage, V+		2		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy		V+ = 4.5V to 28V, includes load regulation error	DAC codes from 1.276V to 1.708V	-0.75		+0.75	%
			DAC codes from 0.844V to 1.260V	-1.25		+1.25	
			DAC codes from 0.444V to 0.828V	-3.0		+3.0	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
Input Bias Current	I_{FB}	FB		-1		+1	µA
	I_{POS}, I_{NEG}	POS, NEG		-0.2		+0.2	
POS, NEG Common-Mode Range		$\overline{DPSLP}$ = GND		0		2	V
POS, NEG Differential Range		V_{POS} - V_{NEG}, $\overline{DPSLP}$ = GND		-200		+200	mV
POS, NEG Offset Gain	A_{OFF}	$\Delta V_{FB}/(V_{POS} - V_{NEG})$, ($V_{POS}$ - V_{NEG}) = 100mV, $\overline{DPSLP}$ = GND		0.95	1.00	1.05	mV/mV
POS, NEG Enable Time		Measured from the time $\overline{DPSLP}$ goes low to the time in which POS, NEG affect a change in the set point (V_{DAC})			0.1		µs
TIME Frequency Accuracy		640kHz nominal, R_{TIME} = 23.5kΩ		580	640	700	kHz
		320kHz nominal, R_{TIME} = 47kΩ		295	320	345	
		64kHz nominal, R_{TIME} = 235kΩ		58	64	70	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0= S0 = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time (Note 1)	t_{ON}	V+ = 5V, V_{FB} = 1.2V, TON = GND (1000kHz)		250	270	290	ns
		V+ = 12V, V_{FB} = 1.2V	TON = REF (550kHz)	165	190	215	
			TON = open (300kHz)	320	355	390	
			TON = V_{CC} = (200kHz)	465	515	565	
Minimum Off-Time (Note 1)	$t_{OFF(MIN)}$	TON = GND (1000kHz)			300	375	ns
		TON = V_{CC}, open or REF (200kHz, 300kHz, or 550kHz)			400	475	ns
$\overline{DDO}$ Delay Time	$t_{\overline{DDO}}$	Measured from the time FB reaches the voltage set by S0–S2, clock speed set by R_{TIME}			32		clks
SKIP Delay Time	t_{SKIP}	Measured from the time when $\overline{DDO}$ is asserted to the time in which the controller begins pulse-skipping operation			30		clks
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point			1.3	2.0	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation			0.1	5	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+			21	40	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			0.1	5	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND			0.1	5	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V			0.1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.990	2.000	2.010	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to 100µA		-10		+10	mV
FAULT PROTECTION							
Output Overvoltage Protection Threshold		Measured at FB with respect to unloaded output voltage, DAC code = 0.7V to 1.708V		13	16	19	%
Output Overvoltage Propagation Delay	t_{OVP}	FB forced 2% above trip threshold			10		µs
Output Undervoltage Protection Threshold		With respect to unloaded output voltage DAC Code = 0.7V to 1.708V		67	70	73	%
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 2% below trip threshold			10		µs
Output Fault Blanking Time	t_{BLANK}	The clock speed is set by R_{TIME} (Note 2)			32		clks

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0= S0 = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IMVPOK, $\overline{CLKEN}$ Threshold		SYSPOK = V_{CC}; measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-12	-10	-8	%
			Upper threshold (overvoltage)	8	10	12	
$\overline{CLKEN}$ Delay	$t_{\overline{CLKEN}}$	FB in regulation, measured from the rising edge of SYSPOK		30	50	90	µs
IMVPOK, $\overline{CLKEN}$ Transition Blanking Time		Measured from the time when FB reaches the voltage set by the DAC code, clock speed set by R_{TIME}			32		clks
IMVPOK Delay	t_{IMVPOK}	FB in regulation, measured from the falling edge of $\overline{CLKEN}$		3	5	7	ms
IMVPOK, $\overline{CLKEN}$, Output Low Voltage		I_{SINK} = 3mA				0.3	V
IMVPOK, $\overline{CLKEN}$, Leakage Current		High state, IMPOK, CLKEN forced to 5.5V				1	µA
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.0		4.4	V
Thermal Shutdown Threshold		Hysteresis = 10°C			160		°C
CURRENT LIMIT							
Current-Limit Threshold Voltage (Positive, Default)		CSP - CSN, ILIM = V_{CC}		47	50	53	mV
Current-Limit Threshold Voltage (Positive, Adjustable)		CSP - CSN	V_{ILIM} = 0.3V	27	30	33	mV
			V_{ILIM} = 1V	97	100	103	
Current-Limit Threshold Voltage (Negative)		CSP - CSN; ILIM = V_{CC}, SUS = GND and $\overline{DPSLP}$ = V_{CC}		-68	-63	-58	mV
Current-Limit Threshold Voltage (Zero Crossing)		GND - LX; SUS = V_{CC} or $\overline{DPSLP}$ = GND			4		mV
CSP, CSN Input Ranges				0		2	V
CSP, CSN Input Current		V_{CSP} = V_{CSN} = 0 to 5V		-1		+1	µA
ILIM Input Current		V_{ILIM} = 0 to 5V			0.01	200	nA
Current-Limit Default Switchover Threshold		ILIM		3	V_{CC} - 1	V_{CC} - 0.4	V
GATE DRIVERS							
DH Gate-Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V			1.2	4.0	Ω
DL Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			1.2	4.0	Ω
		Low state (pulldown)			0.5	1.5	
DH Gate-Driver Source/Sink Current		DH forced to 2.5V, BST - LX forced to 5V			1.6		A
DL Gate-Driver Sink Current		DL forced to 2.5V			4		A

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0= S0 = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DL Gate-Driver Source Current		DL forced to 2.5V			2		A
Dead Time		DL rising			35		ns
		DH rising			26		
VOLTAGE-POSITIONING AMPLIFIER							
Input Offset Voltage	V_{OS}	V_{CM} = 0		-1		+1	mV
Input Bias Current	I_{BIAS}	OAIN+, OAIN-			<0.1	200	nA
Op Amp Disable Threshold		OAIN-		3	V_{CC} - 1	V_{CC} - 0.4	V
Common-Mode Input Voltage Range	V_{CM}	Guaranteed by CMRR test		0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{OAIN+} = V_{OAIN-} = 0 to 2.5V		70	115		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V		75	100		dB
Large-Signal Voltage Gain	AOA	R_L = 1kΩ to V_{CC}/2		80	112		
Output Voltage Swing		$\lvert V_{OAIN+} - V_{OAIN-} \rvert \le$ 10mV, R_L = 1kΩ to V_{CC}/2	V_{CC} - V_{OH}		100	300	mV
			V_{OL}		70	200	
Input Capacitance					11		pF
Gain-Bandwidth Product					3		MHz
Slew Rate					0.3		V/µs
Capacitive-Load Stability		No sustained oscillations			400		pF
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK		2.4			V
Logic Input Low Voltage	V_{IL}	SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK				0.8	V
Logic Input Current		SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK		-1		+1	µA
$\overline{SHDN}$ No Fault Threshold		To enable No-Fault Mode		12		15	V
DAC Input High Voltage	$V_{VID(HIGH)}$	D0–D5		0.7			V
DAC Input Low Voltage	$V_{VID(LOW)}$	D0–D5				0.3	V
DAC Input Current		D0–D5		-1		+1	µA
Driver-Disable Output High Voltage		$\overline{DDO}$, I_{LOAD} = 1mA		2.4			V
Driver-Disable Output Low Voltage		$\overline{DDO}$, I_{LOAD} = 1mA				0.3	V
Four-Level Input Logic Levels		TON, S0–S2, B0–B2	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.5	
Four-Level Input Current		TON, S0–S2, B0–B2 forced to GND or V_{CC}		-3		+3	µA

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0 = SO = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = -40°C to +100°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		Battery voltage, V+		2		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy		V+ = 4.5V to 28V, includes load regulation error	DAC codes from 1.276V to 1.708V	-1.00		+1.00	%
			DAC codes from 0.844V to 1.260V	-1.5		+1.5	
			DAC codes from 0.444V to 0.828V	-3.5		+3.5	
POS, NEG Offset Gain	A_{OFF}	$\Delta V_{FB}/(V_{POS} - V_{NEG})$, ($V_{POS}$ - V_{NEG}) = 100mV, $\overline{DPSLP}$ = GND		0.95		1.05	mV/mV
TIME Frequency Accuracy		640kHz nominal, R_{TIME} = 23.5kΩ		580		700	kHz
		320kHz nominal, R_{TIME} = 47kΩ		295		305	
		64kHz nominal, R_{TIME} = 235kΩ		58		70	
On-Time (Note 1)	t_{ON}	V+ = 5V, V_{FB} = 1.2V, TON = GND (1000kHz)		250		290	ns
		V+ = 12V, V_{FB} = 1.2V	TON = REF (550kHz)	165		215	
			TON = open (300kHz)	320		390	
			TON = V_{CC} (200kHz)	465		565	
Minimum Off-Time (Note 1)	$t_{OFF(MIN)}$	TON = GND (1000kHz)				375	ns
		TON = V_{CC}, open, or REF (200kHz, 300kHz, or 550kHz)				475	ns
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point				2.0	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation				20	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+				40	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND				20	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND				20	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V				20	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0 = SO = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = -40°C to +100°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.985		2.015	V
FAULT PROTECTION							
Output Overvoltage Protection Threshold		Measured at FB with respect to unloaded output voltage		13		19	%
Output Undervoltage Protection Threshold		With respect to unloaded output voltage		67		73	%
IMVPOK, $\overline{CLKEN}$ Threshold		SYSPOK = V_{CC}; measured at FB with respect to unloaded output voltage	lower threshold (undervoltage)	-12		-8	%
			upper threshold (overvoltage)	+8		+12	%
$\overline{CLKEN}$ Delay	$t_{\overline{CLKEN}}$	FB in regulation, measured from the rising edge of SYSPOK		30			µs
IMVPOK Delay	t_{IMVPOK}	FB in regulation, measured from the falling edge of $\overline{CLKEN}$		3			ms
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 20mV, PWM disabled below this level		3.95		4.45	V
CURRENT LIMIT							
Current-Limit Threshold Voltage (Positive, Default)		CSP - CSN, ILIM = V_{CC}		45		55	mV
Current-Limit Threshold Voltage (Positive, Adjustable)		CSP - CSN	V_{ILIM} = 0.3V	25		35	mV
			V_{ILIM} = 2V (REF)	95		105	
Current-Limit Threshold Voltage (Negative)		CSP - CSN; ILIM = V_{CC}, SUS = GND and $\overline{DPSLP}$ = V_{CC}		-70		-56	mV
GATE DRIVERS							
DH Gate-Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V				4.5	Ω
DL Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				4.5	Ω
		Low state (pulldown)				2.0	
VOLTAGE-POSITIONING AMPLIFIER							
Input Offset Voltage	V_{OS}	V_{CM} = 0		-2		+2	mV
Output Voltage Swing		$\lvert V_{OAIN+} - V_{OAIN-} \rvert \le$ 10mV, R_L = 1kΩ to $V_{CC}/2$	$V_{CC} - V_{OH}$			300	mV
			V_{OL}			200	

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = V_{BI} = V_{OAIN-} = 5V, V_{FB} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, ILIM = V_{CC}, SUS = D5 = D1= D0 = SO = S1 = S2 = B0 = GND, V_{D4} = V_{D3} = V_{D2} = 1V, V_{B2} = 2V. **T_A = -40°C to +100°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Output Voltage Swing		$\|V_{OAIN+} - V_{OAIN-}\| \le 10mV$, R_L = 1kΩ to $V_{CC}/2$	$V_{CC} - V_{OH}$		300	
			V_{OL}		200	
LOGIC AND I/O						
DAC Input High Voltage	$V_{VID(HIGH)}$	D0–D5		0.7		V
DAC Input Low Voltage	$V_{VID(LOW)}$	D0–D5			0.3	V
Four-Level Input Logic Levels		TON, S0–S2, B0–B2	High	V_{CC} - 0.4		V
			Open	3.15	3.85	
			REF	1.65	2.35	
			Low		0.5	

Note 1: On-time specifications are measured from 50% to 50% at the DH pin, with LX forced to GND, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

Note 2: The output fault blanking time is measured from the time when FB reaches the regulation voltage set by the DAC code. During power-up, the regulation voltage is set by the boot DAC code (B0–B2). During normal operation (SUS = low), the regulation voltage is set by the VID DAC inputs (D0–D5). During suspend mode (SUS = high), the regulation voltage is set by the suspend DAC inputs (S0–S2).

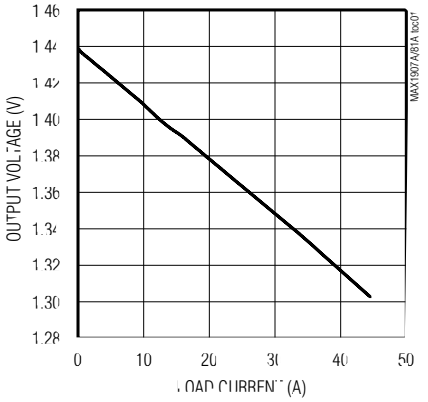
Note 3: Specifications to T_A = -40°C to +100°C are guaranteed by design and are not production tested.

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

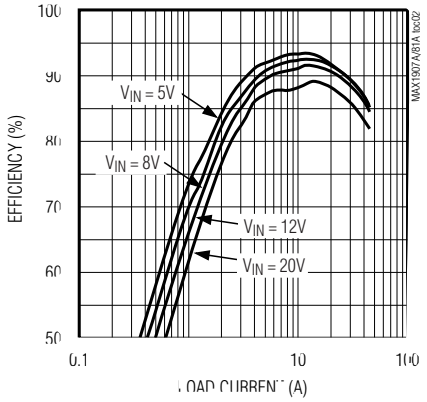
Typical Operating Characteristics

(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, B0–B2 set to 1.276V, S0–S2 set to 0.748V.)

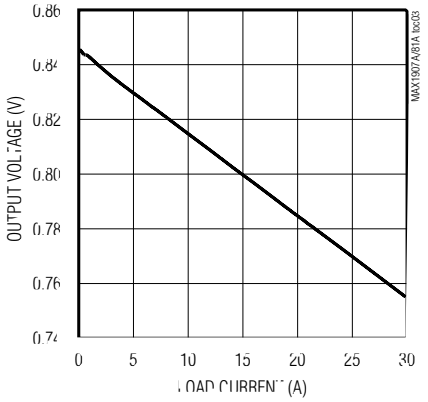
VOLTAGE-POSITIONED OUTPUT VS. LOAD CURRENT (V_{OUT} = 1.436V)



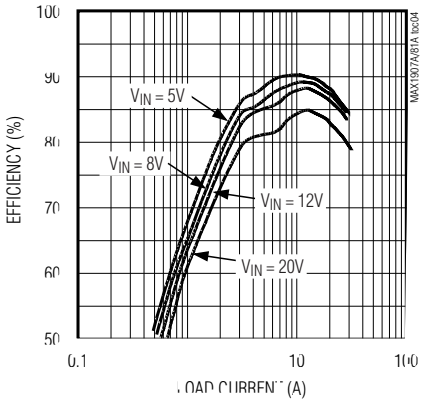
EFFICIENCY VS. LOAD CURRENT (V_{OUT} = 1.436V)



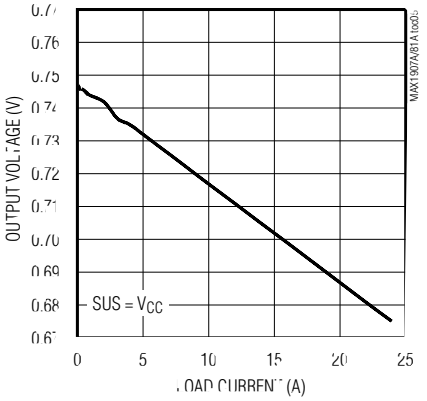
VOLTAGE-POSITIONED OUTPUT VS. LOAD CURRENT (V_{OUT} = 0.844V)



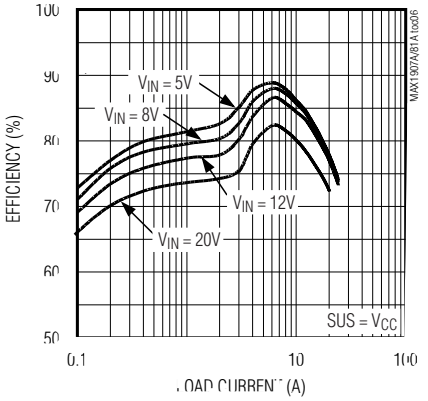
EFFICIENCY VS. LOAD CURRENT (V_{OUT} = 0.844V)



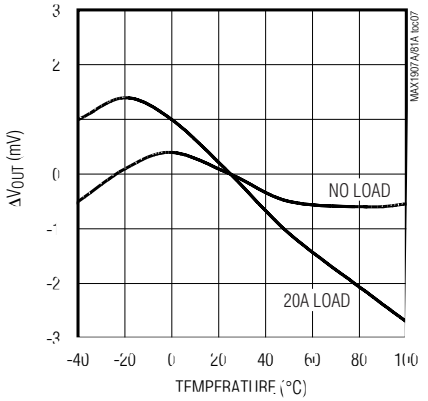
VOLTAGE-POSITIONED OUTPUT VS. LOAD CURRENT (V_{OUT} = 0.748V)



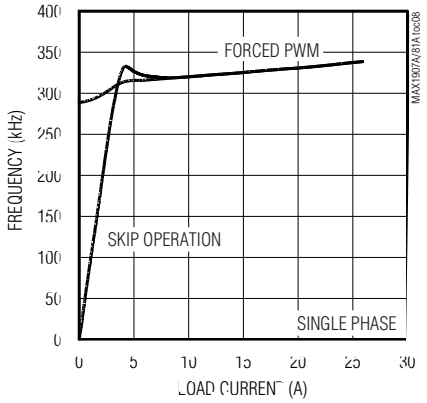
EFFICIENCY VS. LOAD CURRENT (V_{OUT} = 0.748V)



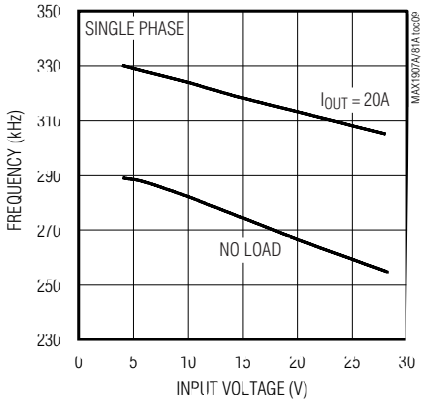
OUTPUT VOLTAGE SHIFT VS. TEMPERATURE



FREQUENCY VS. LOAD CURRENT



FREQUENCY VS. INPUT VOLTAGE

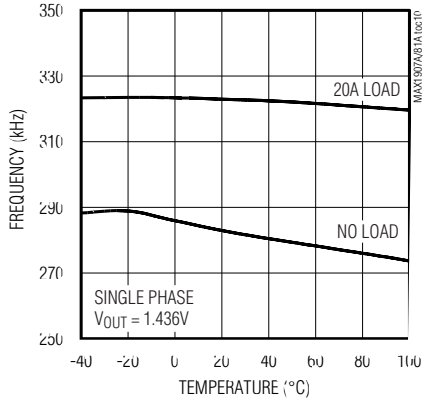


Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

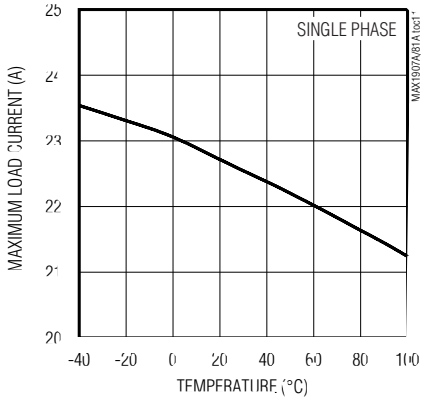
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, B0–B2 set to 1.276V, S0–S2 set to 0.748V.)

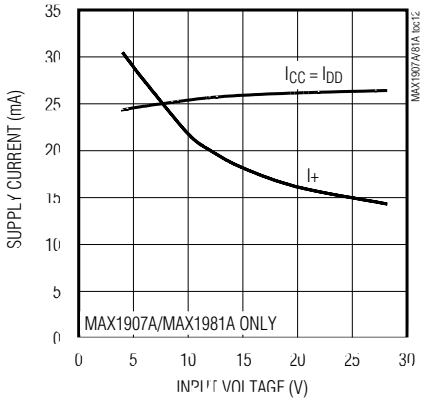
FREQUENCY vs. TEMPERATURE



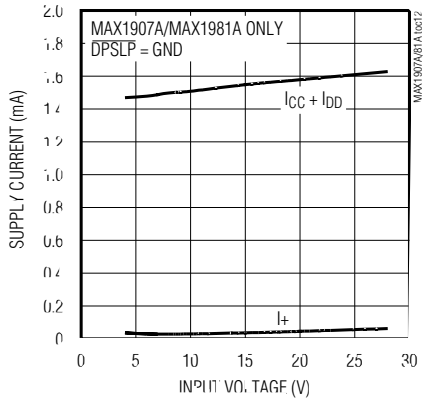
OUTPUT CURRENT AT CURRENT LIMIT vs. TEMPERATURE



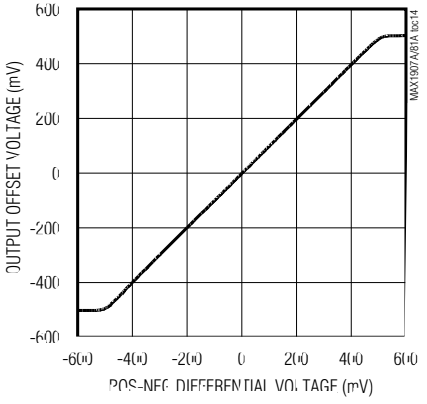
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM MODE)



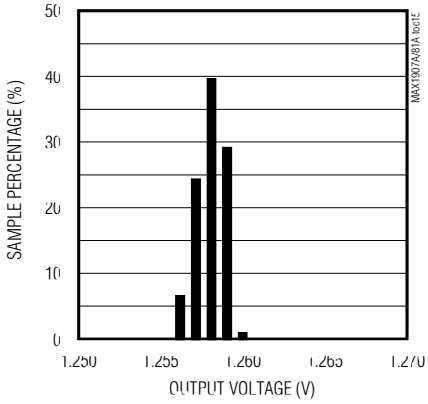
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PULSE SKIPPING)



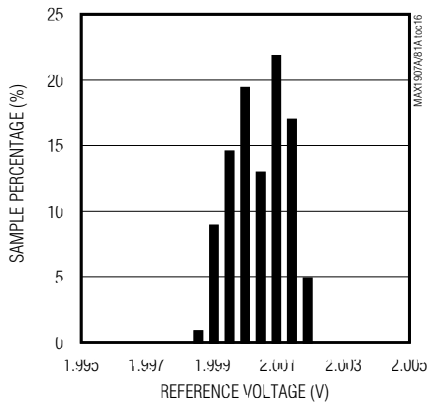
OUTPUT OFFSET VOLTAGE vs. POS-NEG DIFFERENTIAL VOLTAGE



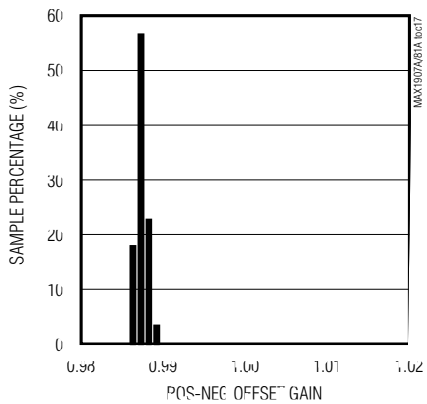
260V OUTPUT VOLTAGE DISTRIBUTION



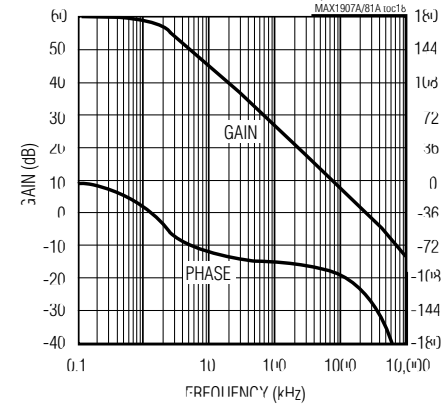
REFERENCE VOLTAGE DISTRIBUTION



POS-NEG OFFSET GAIN DISTRIBUTION



VOLTAGE-POSITIONING AMPLIFIER GAIN AND PHASE vs. FREQUENCY

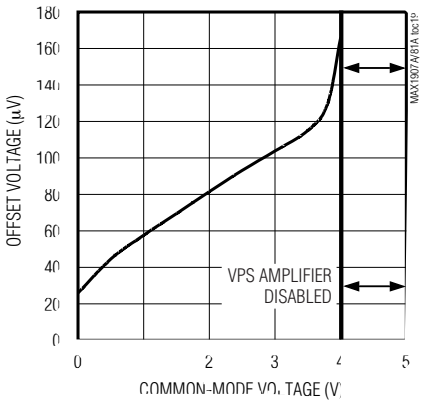


Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

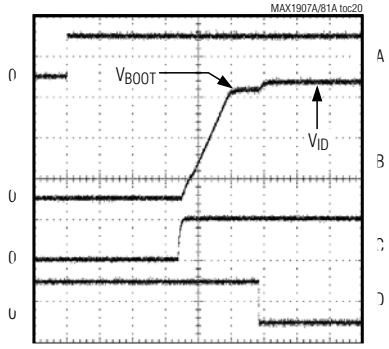
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, B0–B2 set to 1.276V, S0–S2 set to 0.748V.)

VPS AMPLIFIER OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



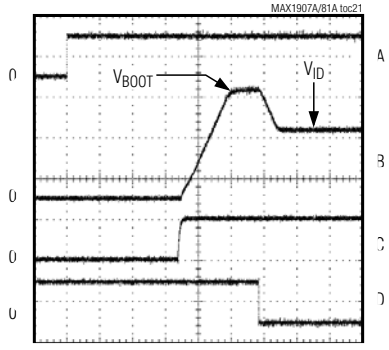
POWER-UP SEQUENCE (HIGHEST FREQUENCY)



100µs/div

A. $V_{\overline{SHDN}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 0 to 1.436V, 500mV/div
C. $\overline{DDO}$, 5V/div
D. $\overline{CLKEN}$, 5V/div
NO LOAD

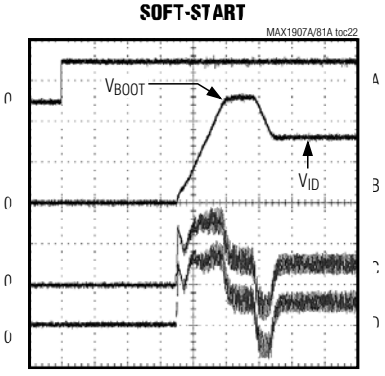
POWER-UP SEQUENCE (LOWEST FREQUENCY)



100µs/div

A. $V_{\overline{SHDN}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 0 to 0.844V, 500mV/div
C. $\overline{DDO}$, 5V/div
D. $\overline{CLKEN}$, 5V/div
NO LOAD

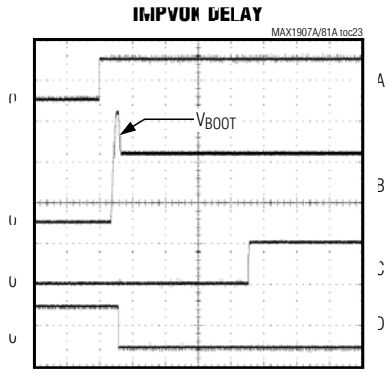
SOFT-START



100µs/div

A. $V_{\overline{SHDN}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 0 to 0.844V, 500mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div
30mΩ LOAD

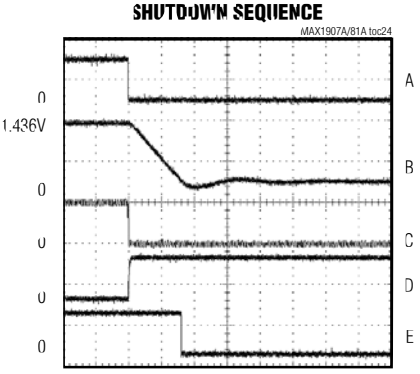
IMPVOK DELAY



1ms/div

A. $V_{\overline{SHDN}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 0 to 0.844V, 500mV/div
C. IMPVOK 5V/div
D. $\overline{CLKEN}$, 5V/div

SHUTDOWN SEQUENCE



100µs/div

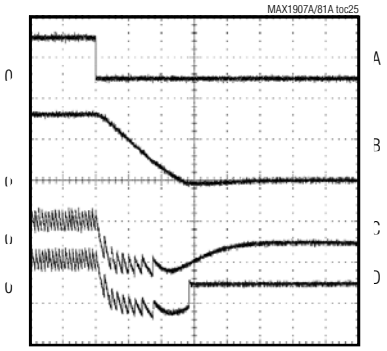
A. $V_{\overline{SHDN}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 1.436V to 0, 1V/div
C. IMPVOK 5V/div
D. $\overline{CLKEN}$, 5V/div
$\overline{DDO}$, 5V/div

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

Typical Operating Characteristics (continued)

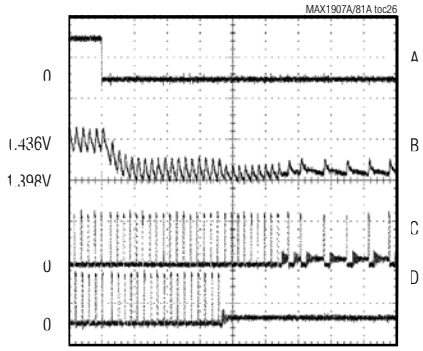
(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, B0–B2 set to 1.276V, S0–S2 set to 0.748V.)

SOFT SHUTDOWN



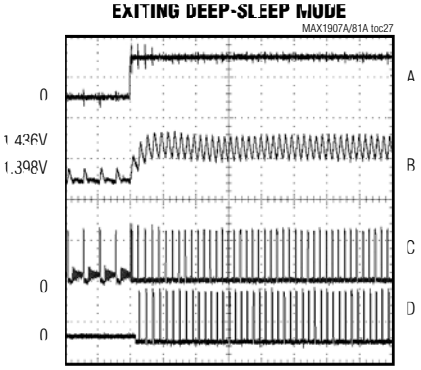
A. $V_{\overline{SHDN}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 0.844V to 0, 1V/div
C. I_{LM}, 10A/div
D. I_{LS},10A/div
8.0mΩ LOAD

ENTERING DEEP-SLEEP MODE



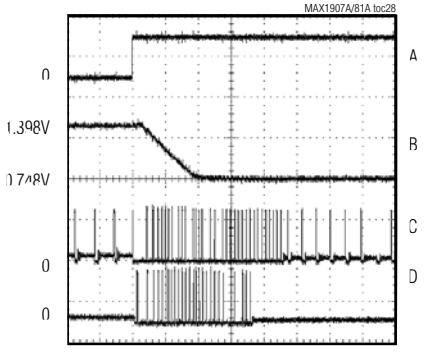
A. $V_{\overline{DPSLP}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 1.436V to 1.398V, 50mV/div
C. MAX1907A/MAX1981A LX, 10V/div
D. MAX1980 LX, 10V/div
SUS = GND, I_{OUT} = 1.0A

EXITING DEEP-SLEEP MODE



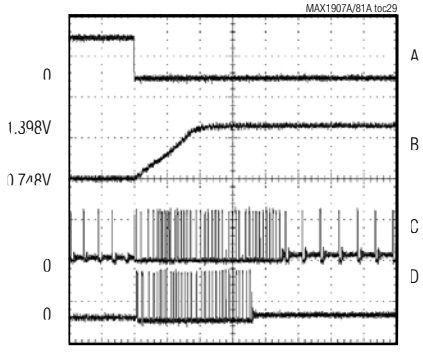
A. $V_{\overline{DPSLP}}$ = 0 to 5V, 5V/div
B. V_{OUT} = 1.398V to 1.436V, 50mV/div
C. MAX1907A/MAX1981A LX, 10V/div
D. MAX1980 LX, 10V/div
SUS = GND, I_{OUT} = 1.0A

ENTERING SUSPEND MODE



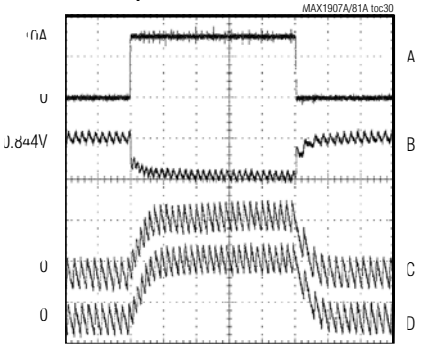
A. V_{SUS} = 0 to 5V, 5V/div
B. V_{OUT} = 1.398V to 0.748V, 500mV/div
C. MAX1907A/MAX1981A LX, 10V/div
D. MAX1980 LX, 10V/div
$\overline{DPSLP}$ = GND, I_{OUT} = 0.5A

EXITING SUSPEND MODE



A. V_{SUS} = 0 to 5V, 5V/div
B. V_{OUT} = 0.748V to 1.398V, 500mV/div
C. MAX1907A/MAX1981A LX, 10V/div
D. MAX1980 LX, 10V/div
$\overline{DPSLP}$ = GND, I_{OUT} = 0.5A

LOAD TRANSIENT (LOWEST FREQUENCY)

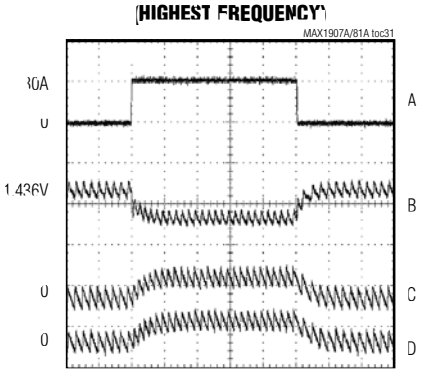


A. I_{OUT} = 0 to 10A, 10A/div
B. V_{OUT} = 0.844V (NO LOAD), 50mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

Typical Operating Characteristics (continued)

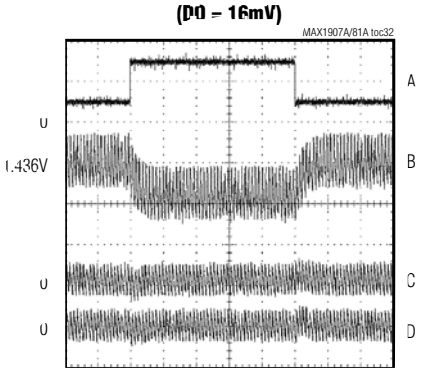
(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, B0–B2 set to 1.276V, S0–S2 set to 0.748V.)

LOAD TRANSIENT
(HIGHEST FREQUENCY)



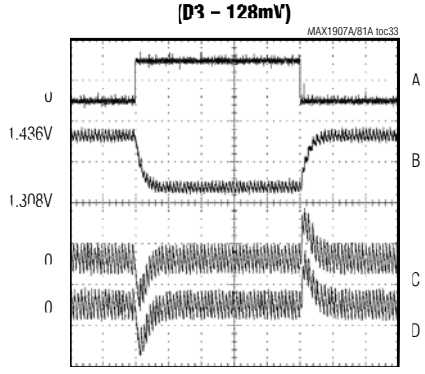
A. I_{OUT} = 0 to 30A, 20A/div
B. V_{OUT} = 1.436V (NO LOAD), 100mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

DYNAMIC VID TRANSITION
(D0 = 16mV)



A. V_{D0} = 0 to 1V, 1V/div
B. V_{OUT} = 1.436V to 1.420V, 20mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

DYNAMIC VID TRANSITION
(D3 = 128mV)



A. V_{D3} = 0 to 1V, 1V/div
B. V_{OUT} = 1.436V to 1.308V, 100mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	B0–B2	Boot-Mode Voltage Select Inputs. B0–B2 are four-level digital inputs that select the boot-mode VID code (Table 6) for the boot-mode multiplexer inputs. During power-up, the boot-mode VID code is delivered to the DAC (see the *Internal Multiplexers* section).
4, 5, 6	S0–S2	Suspend-Mode Voltage Select Inputs. S0–S2 are four-level digital inputs that select the suspend-mode VID code (Table 5) for the suspend-mode multiplexer inputs. If SUS is high, the suspend-mode VID code is delivered to the DAC (see the *Internal Multiplexers* section).
7	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 10µA (max) shutdown state. During the transition from normal operation to shutdown the output voltage is ramped down at the output voltage slew rate programmed by the TIME pin. In shutdown mode, DL is forced to V_{DD} to clamp the output to ground. Forcing $\overline{SHDN}$ to 12V~15V disables both overvoltage protection and undervoltage protection circuits, and clears the fault latch. Do not connect $\overline{SHDN}$ to >15V.
8	REF	2V Reference Output. Bypass to GND with 0.22µF or greater ceramic capacitor. The reference can source 50µA for external loads. Loading REF degrades output voltage accuracy according to the REF load regulation error.
9	ILIM	Current-Limit Adjustment. The current-limit threshold defaults to 50mV if ILIM is tied to V_{CC}. In adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM over a 100mV to 1.5V range. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V.
10	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) with a series 10Ω resistor. Bypass to GND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
11	GND	Analog Ground
12	CC	Integrator Capacitor Connection. Connect a 47pF to 1000pF (270pF typ) capacitor from CC to GND to set the integration time constant.
13	POS	Feedback Offset Adjust Positive Input. The output shifts by 100% (typ) of the differential input voltage appearing between POS and NEG when $\overline{DPSLP}$ is low. The common-mode range of POS and NEG is 0 to 2V. POS and NEG should be generated from resistor dividers from the output.
14	NEG	Feedback Offset Adjust Negative Input. The output shifts by 100% (typ) of differential input voltage appearing between POS and NEG when $\overline{DPSLP}$ is low. The common-mode range of POS and NEG is 0 to 2V. POS and NEG should be generated from resistor dividers from the output.
15	FB	Feedback Input. FB is internally connected to both the feedback input and the output of the voltage-positioning op amp (Figure 2). Connect a resistor between FB and OAIN- (Figure 1) to set the voltage-positioning gain (see the *Setting Voltage Positioning* section).
16	OAIN-	Dual-Mode Op Amp Inverting Input and Op Amp Disable Input. When using the internal op amp for additional voltage-positioning gain (Figure 1), connect to the negative terminal of current-sense resistor through a 1kΩ ±1% resistor as described in the *Setting Voltage Positioning* section. Connect OAIN- to V_{CC} to disable op amp. The logic threshold to disable the op amp is approximately V_{CC} - 1V.
17	OAIN+	Op Amp Noninverting Input. When using the internal op amp for additional voltage-positioning gain (Figure 1), connect to the positive terminal of current-sense resistor through a resistor as described in the *Setting Voltage Positioning* section.
18	CSP	Positive Current-Limit Input. Connect to the positive terminal of the current-sense resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
19	CSN	Negative Current-Limit Input. Connect to the negative terminal of the current-sense resistor.
20	$\overline{DPSLP}$	Deep-Sleep Control Input. When $\overline{DPSLP}$ is low the system enters the deep-sleep state and the regulator applies the appropriate deep-sleep offset. The MAX1907A/MAX1981A adds the offset measured at the POS and NEG pins to the output. 32 clock cycles after the deep-sleep transition is completed, $\overline{DDO}$ goes low (see the *Driver Disable and Low-Power Pulse Skipping* section). Another 32 clock cycles later, the MAX1907A/MAX1981A is allowed to enter pulse-skipping operation.
21–26	D5–D0	Low-Voltage VID DAC Code Inputs. D0 is the LSB, and D5 is the MSB of the internal 6-bit VID DAC (Table 4). The D0–D5 inputs do not have internal pullups. These 1V logic inputs are designed to interface directly with the CPU. In all normal active modes (modes other than suspend and boot), the output voltage is set by the VID code indicated by the D0–D5 logic-level voltages on D0–D5. In suspend mode (SUS = high), the decoded state of the four-level S0–S2 inputs sets the output voltage. In boot mode (see the *Power-Up Sequence* section), the decoded state of the four-level B0–B2 inputs set the output voltage.
27	$\overline{DDO}$	Driver-Disable Output. This TTL-logic output can be used to disable the driver outputs on slave-switching regulator controllers. This forces a high-impedance condition and makes it possible for the MAX1907A/MAX1981A master controller to operate in low current SKIP mode. $\overline{DDO}$ goes low 32 R_{TIME} clock cycles after the MAX1907A/MAX1981A completes a transition to the suspend mode or deep-sleep voltage (see the *Driver Disable and Low-Power Pulse Skipping* section). Another 30 clock cycles later, the MAX1907A/MAX1981A enters automatic pulse-skipping operation.
28	PGND	Power Ground. Ground connection for the DL gate driver.
29	DL	Low-Side Gate Driver Output. DL swings from PGND to V_{DD}. DL is forced high after the MAX1907A/MAX1981A powers down ($\overline{SHDN}$ = GND) or when the controller detects a fault. The MAX1981A does not include overvoltage protection.
30	V_{DD}	Supply Voltage Input for the DL Gate Driver. Connect to the system supply voltage (4.5V to 5.5V). Bypass to PGND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
31	BST	Boost Flying Capacitor Connection. An optional resistor in series with BST allows the DH pullup current to be adjusted.
32	LX	Inductor Connection. LX is the internal lower supply rail for the DH high-side gate driver. It connects to the skip-mode zero-crossing comparator.
33	DH	High-Side Gate Driver. Output swings LX to BST.
34	V+	Battery Voltage Sense Connection. Used only for PWM one-shot timing. DH on-time is inversely proportional to input voltage over a range of 2V to 28V.
35	SUS	Suspend-Mode Control Input. When SUS is high the regulator slews to the suspend voltage level. This level is set with four-level logic signals at the S0–S2 inputs. 32 clock cycles after the transition to the suspend-mode voltage is completed, $\overline{DDO}$ goes low (see the *Driver Disable and Low-Power Pulse Skipping* section). Another 32 clock cycles later, the MAX1907A/MAX1981A is allowed to enter pulse-skipping operation.
36	SYSPOK	System Power-Good Input. Primarily, SYSPOK serves as the wired NOR junction of the open-drain power-good signals for the V_{CCP} and V_{CCMCH} supplies. A falling edge on SYSPOK shuts down the MAX1907A/MAX1981A and sets the fault latch. Toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V to restart the controller.

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

Pin Description (continued)

PIN	NAME	FUNCTION
37	IMVPOK	Open-Drain Power Good Output. After output voltage transitions, except during power-up and power-down, if OUT is in regulation then IMVPOK is high impedance. IMVPOK is pulled high whenever the slew-rate control is active (output voltage transitions). IMVPOK is forced low in shutdown. A pullup resistor on IMVPOK will cause additional finite shutdown current. IMVPOK also reflects the state of SYSPOK and includes a 3ms (min) delay for power-up. IMVPOK is forced high during VID transitions.
38	$\overline{\text{CLKEN}}$	Clock Enable Logic Output. This inverted logic output indicates when SYSPOK is high and the output voltage sensed at FB is in regulation. $\overline{\text{CLKEN}}$ is forced low during VID transitions.
39	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 235kΩ to 23.5kΩ resistor sets the clock from 64kHz to 640kHz, f_{SLEW} = 320kHz × 47kΩ/R_{TIME}.
40	TON	On-Time Selection Control Input. This four-level input sets the K-factor value (Table 3) used to determine the DH on-time (see the *On-Time One-Shot* section). GND = 1000kHz, REF = 550kHz, OPEN = 300kHz, V_{CC} = 200kHz.

Table 1. Component Selection for Standard Multiphase Applications (Figure 1)

DESIGNATION	COMPONENT
Input Voltage Range*	8V to 24V
VID Output Voltage (D5–D0)	1.308V (D5–D0 = 011001)
Boot Voltage (B0–B2)	1.004V (B2 = OPEN, B1 = V_{CC}, B0 = GND)
Suspend Voltage (S0–S2)	0.748V (S2 = OPEN, S1 = V_{CC}, S0 = GND)
Deep-Sleep Offset Voltage (POS, NEG)	-50mV
Maximum Load Current	40A
Inductor (per phase)	0.6µH Sumida CDEP134H-0R6, Panasonic ETQP6F0R6BFA, or BI Technologies HM73-30R60
Switching Frequency	300kHz (TON = float)
High-Side MOSFET (N_H, per phase)	International Rectifier (2) IRF7811W or Siliconix (2) Si4892DY
Low-Side MOSFET (N_L, per phase)	International Rectifier (2) IRF7822, Fairchild (3) FDS7764A, or Siliconix (2) Si4860DY
Input Capacitor (C_{IN})	(6) 10µF 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Output Capacitor (C_{OUT})	(5) 330µF 2.5V Panasonic EEFUE0E331XR
Current-Sense Resistor (R_{SENSE}, per phase)	1.5mΩ Panasonic ERJM1WTJ1M5U
Schottky Diodes (D1, D2, D3)	Central Semiconductor CMPSH-3

**Input voltages less than 8V requires additional input capacitance.*

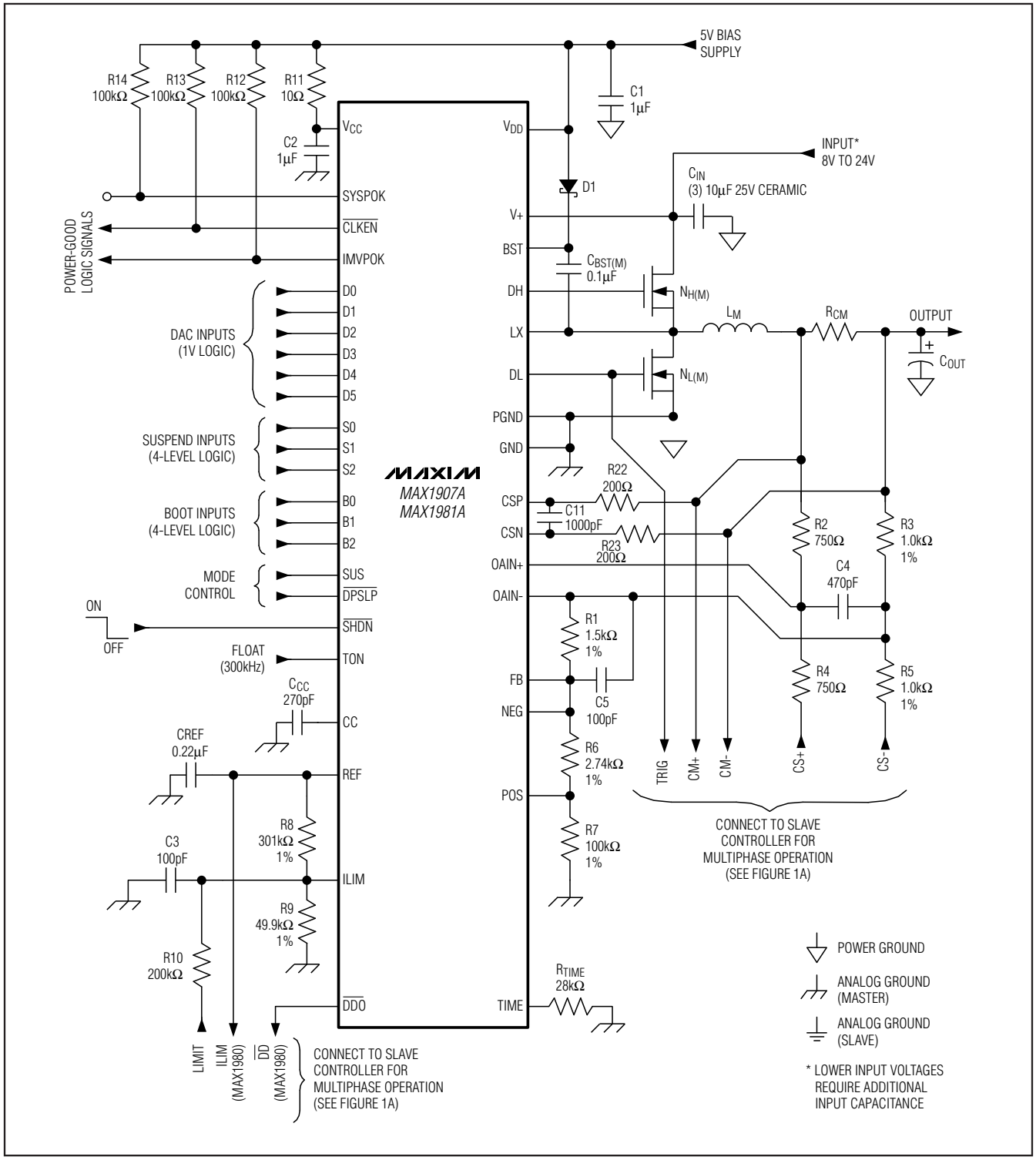


Figure 1. Standard Multiphase Application Circuit

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

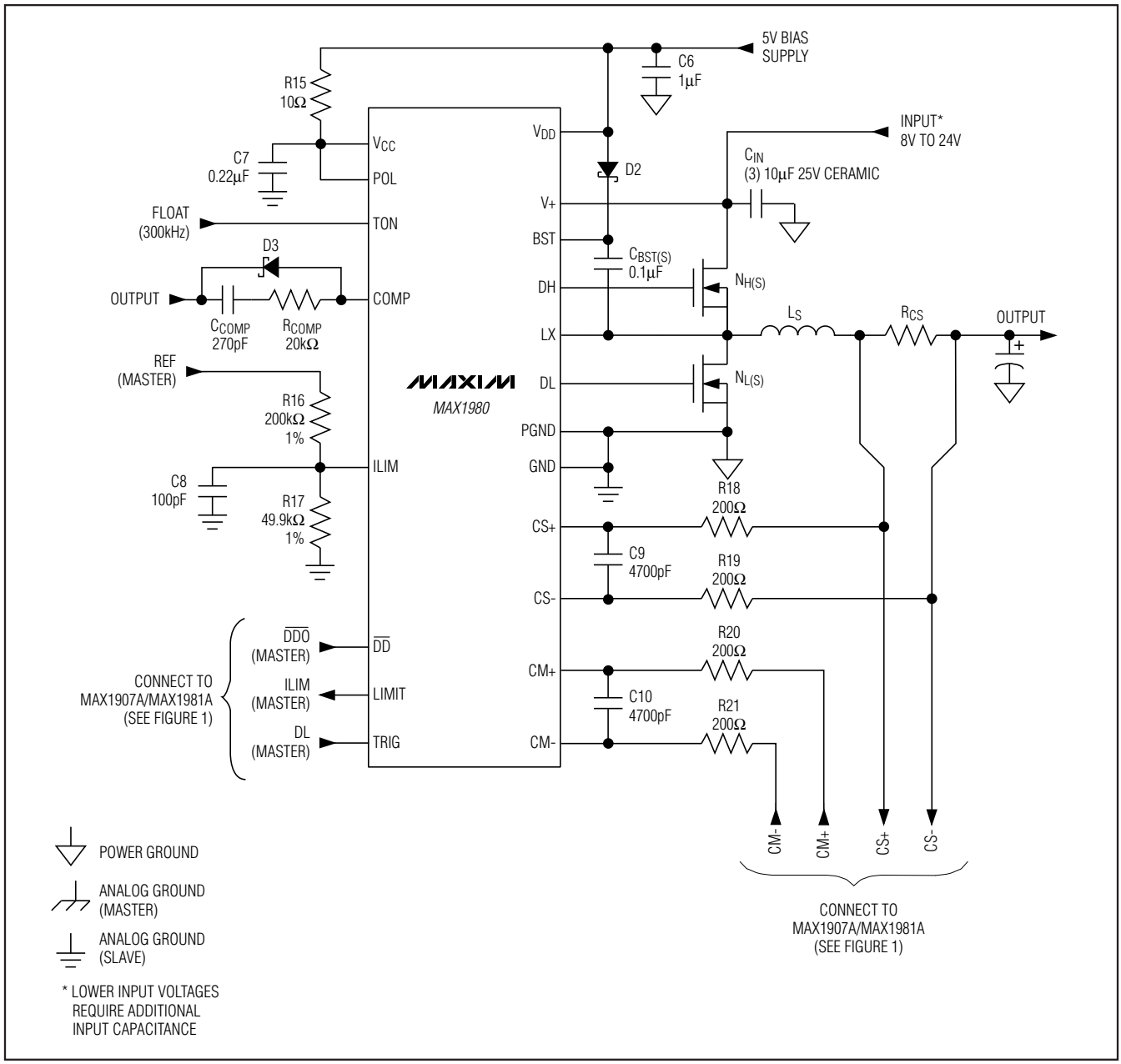


Figure 1A. Standard Multiphase Application Circuit (continued)

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
BI Technologies	714-447-2345 (USA)	www.bitechnologies.com
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	561-752-5000 (USA)	www.coiltronics.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	847-468-5624 (USA)	www.panasonic.com
Sanyo	408-749-9714 (USA) 65-281-3226 (Singapore)	www.secc.co.jp
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	408-573-4150 (USA) 03-3667-3408 (Japan)	www.t-yuden.com
TDK	847-803-6100 (USA) 81-3-5201-7241 (Japan)	www.component.tdk.com
Toko	858-675-8013 (USA)	www.tokoam.com

Detailed Description

5V Bias Supply (V_{CC} and V_{DD})

The MAX1907A/MAX1981A require an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator.

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 10mA \text{ to } 60mA \text{ (typ)}$$

where I_{CC} is 1.3mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total, gate-charge specification limits at V_{GS} = 5V.

V+ and V_{DD} can be tied together if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns, typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage:

$$t_{ON} = K(V_{FB} + 0.075V) / V_{IN}$$

where K is set by the TON pin-strap connection (Table 3) and 0.075V is an approximation to accommodate the

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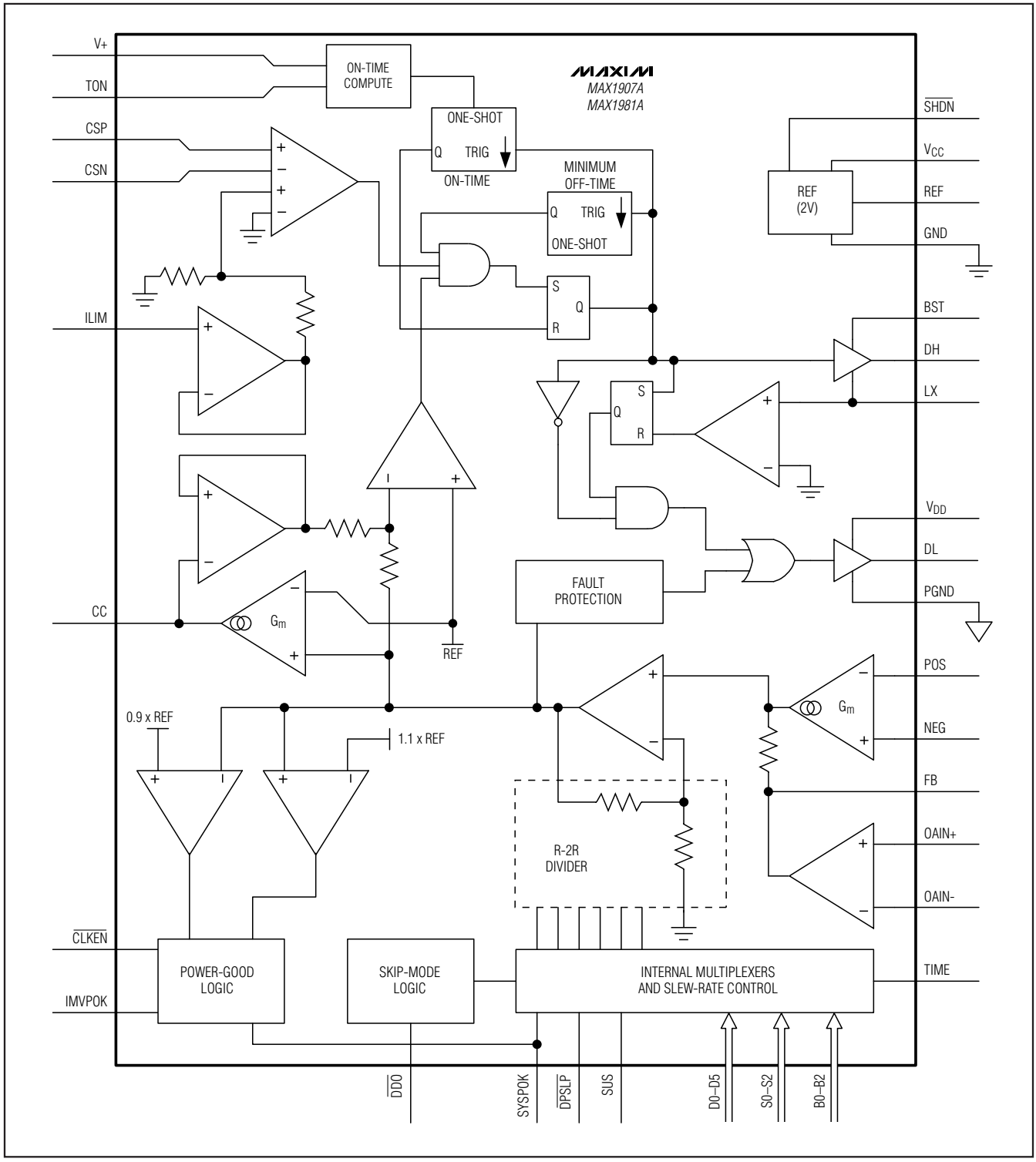

Figure 2. MAX1907A/MAX1981A Functional Diagram

expected drop across the low-side MOSFET switch. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: 1) the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; 2) the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* (±10% at 200kHz and 300kHz, ±12% at 550kHz and 1000kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wider range. For example, the 1000kHz setting will typically run about 10% slower with inputs much greater than 5V due to the very short on-times required.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode (SUS = low, $\overline{DPSLP}$ = low) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time.

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time calculated by the MAX1907A/MAX1981A.

Table 3. Approximate K-Factor Errors

TON CONNECTION	FREQUENCY SETTING (kHz)	K-FACTOR (µs)	MAX K-FACTOR ERROR (%)
V_{CC}	200	5	±10
Float	300	3.3	±10
REF	550	1.8	±12.5
GND	1000	1.0	±12.5

Integrator Amplifiers/ Output Voltage Offsets

Two transconductance amplifiers provide a fine adjustment to the output regulation point (Figure 2). One amplifier forces the DC average of the feedback voltage to equal the VID DAC setting. The second amplifier is used to create small positive or negative offsets to the feedback voltage, using the POS and NEG pins.

The feedback amplifier integrates the feedback voltage, allowing accurate DC output voltage regulation regardless of the output ripple voltage. The feedback amplifier has the ability to shift the output voltage by ±8%. The differential input voltage range is at least ±80mV total, including DC offset and AC ripple. The integration time constant can be set easily with one capacitor at the CC pin. Use a capacitor value of 47pF to 1000pF (270pF, typ).

The POS/NEG amplifier is used to add small offsets to the VID DAC setting in deep-sleep mode ($\overline{DPSLP}$ = low). The offset amplifier is summed directly with the feedback voltage, making the offset gain independent of the DAC code. This amplifier has the ability to offset the output by ±200mV. To create an output offset, bias POS and NEG to a voltage (typically V_{OUT} or REF) within their 0 to 2V common-mode range, and offset them from one another with a resistive divider (Figure 1). If V_{POS} is higher than V_{NEG}, then the output is shifted in the positive direction. If V_{NEG} is higher than V_{POS}, then the output is shifted in the negative direction. The output offset equals the voltage difference from POS to NEG.

Forced-PWM Operation (Normal Mode)

During normal mode, when the CPU is actively running (SUS = low and $\overline{DPSLP}$ = high), the MAX1907A/MAX1981A operates with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparator, forcing the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform. The benefit of forced-PWM mode is to keep the switching frequency fairly constant.

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Forced-PWM operation comes at a cost: the no-load 5V bias supply current remains between 10mA to 40mA, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light load conditions, the MAX1907A/MAX1981A automatically switches to the low-power pulse skipping control scheme after entering suspend or deep-sleep mode.

During all output voltage and mode transitions, the MAX1907A/MAX1981A uses forced-PWM operation in order to ensure fast, accurate transitions. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads, quickly discharging the output capacitors. The controller maintains forced-PWM operation for 30 clock cycles (set by R_{TIME}) after the controller sets the last DAC code value to guarantee the output voltage settles properly before entering pulse-skipping operation.

Low-Power Pulse Skipping

During deep-sleep mode ($\overline{DPSLP}$ = low) or low-power suspend (SUS = high), the MAX1907A/MAX1981A uses an automatic pulse-skipping control scheme.

For deep-sleep mode, when the CPU pulls $\overline{DPSLP}$ low, the MAX1907A/MAX1981A shifts the output voltage to incorporate the offset voltage set by the POS and NEG inputs. The controller pulls the driver-disable output ($\overline{DDO}$) low 32 R_{TIME} clock cycles after $\overline{DPSLP}$ goes low. Another 30 R_{TIME} clock cycles later, the MAX1907A/MAX1981A enters low-power operation, allowing automatic pulse skipping under light loads. When the CPU drives $\overline{DPSLP}$ high, the MAX1907A/MAX1981A immediately enters forced-PWM operation, forces $\overline{DDO}$ high, and eliminates the output offset, slewing the output to the operating voltage set by the D0–D5 inputs. When either $\overline{DPSLP}$ transition occurs, the MAX1907A/MAX1981A forces IMVPOK high and $\overline{CLKEN}$ low for 32 R_{TIME} clock cycles.

When entering suspend mode (SUS driven high), the MAX1907A/MAX1981A slews the output down to the suspend output voltage set by SO–S2 inputs. 32 R_{TIME} clock cycles after the slew-rate controller reaches the last DAC code (see the *Output Voltage Transition Timing* section), the driver-disable output ($\overline{DDO}$) is asserted low. After another 30 R_{TIME} clock cycles, the MAX1907A/MAX1981A enters low-power operation, allowing pulse skipping under light loads. When the CPU pulls SUS low, the MAX1907A/MAX1981A immediately enters forced-PWM operation, forces $\overline{DDO}$ high, and slews the output up to the operating voltage set by the D0–D5 inputs. When either SUS transition occurs, the MAX1907A/MAX1981A blanks IMVPOK and $\overline{CLKEN}$, preventing IMVPOK from going low and $\overline{CLKEN}$ from going high. The blanking remains until the slew-rate controller has reached the last DAC code and 32 RTIME clock pulses have passed.

In multiphase applications, the driver-disable signal is used to force one or more slave regulators into a high-impedance state. When the master's $\overline{DDO}$ output is driven low, the slave controller with driver disable (MAX1980) forces its DL (SLAVE) and DH (SLAVE) gate drivers low, effectively disabling the slave controller. Disabling the slave controller for single-phase operation allows the MAX1907A/MAX1981A to enter low-power pulse-skipping operation under low-power conditions, improving light-load efficiency. When $\overline{DDO}$ is driven high, the slave controller (MAX1980) enables the drivers, allowing normal forced-PWM operation.

Automatic Pulse-Skipping Switchover

In skip mode (SUS = high, or $\overline{DPSLP}$ = low), an inherent automatic switchover to PFM takes place at light loads (Figure 3). This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFET. Once V_{LX} - VP_{GND} drops below 4mV (typ), the comparator forces DL low (Figure 2). This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 4). For a battery range of 8V to 24V, this threshold is relatively constant, with only a minor dependence on battery voltage:

$$I_{LOAD(SKIP)} = \left(\frac{V_{OUT}K}{2L}\right)\left(\frac{V_{BATT} - V_{OUT}}{V_{BATT}}\right)$$

where K is the on-time scale factor (Table 3). For example, in the standard application circuit this becomes:

$$\left(\frac{1.3V \times 3.3\mu s}{2 \times 0.68\mu H}\right)\left(\frac{12.0V - 1.3V}{12.0V}\right) = 2.8A$$

The crossover point occurs at a lower value if a swinging (soft-saturation) inductor is used. The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader effi-

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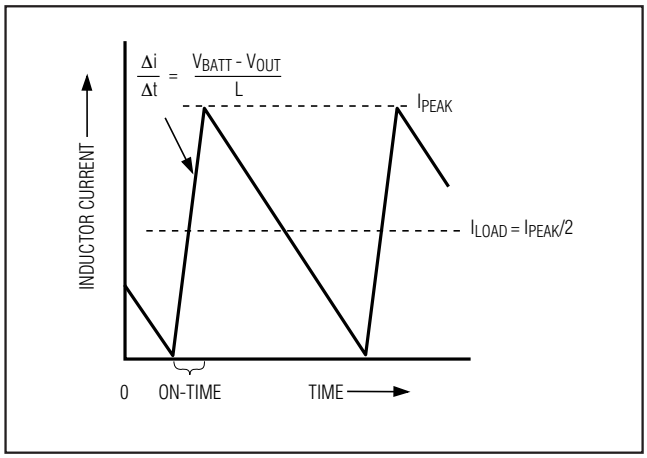

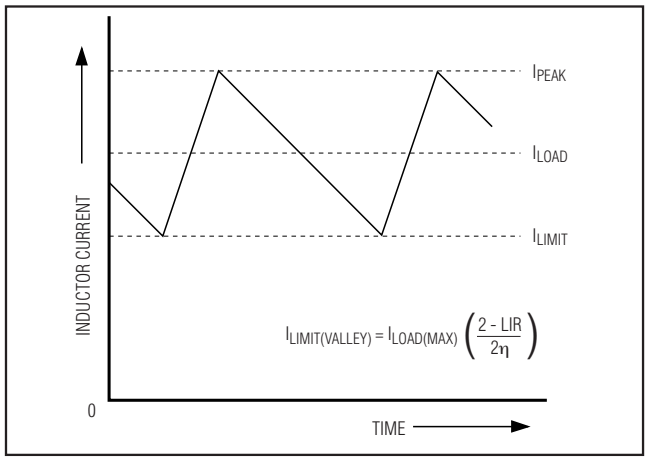

Figure 4. "Valley" Current-Limit Threshold Point

ciency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input voltage levels.

Current-Limit Circuit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses a current-sense resistor between CSP and CSN as the current-sensing element (Figure 1). If the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). Since only the "valley" current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM. The current-limit threshold voltage adjustment range is from 10mV to 150mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM. The threshold defaults to 50mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by LX and GND. Place the IC close to the low-side MOSFET with short, direct traces, making a Kelvin sense connection to the source and drain terminals.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderately sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1907A/MAX1981A will interpret the MOSFET gate as "off" while there is actually charge still left on the gate. Use very short, wide traces (50 to 100 mils wide if the MOSFET is 1in from the device). The dead time at the other edge (DH turning off) is determined by a fixed 35ns internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.5Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFET when LX switches from ground to V_{IN}. Applications with high input voltages and long inductive traces may require additional gate-to-source capacitance to ensure fast-rising LX edges do not pullup the DL gate driver, causing shoot-through currents. The capacitive cou-

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pling between LX and DL created by the MOSFETs' gate-to-drain capacitance (C_{RSS}), gate-to-source (C_{ISS}-C_{RSS}), and additional board parasitics should not exceed the following minimum threshold voltage:

$$V_{GS(TH)} < V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

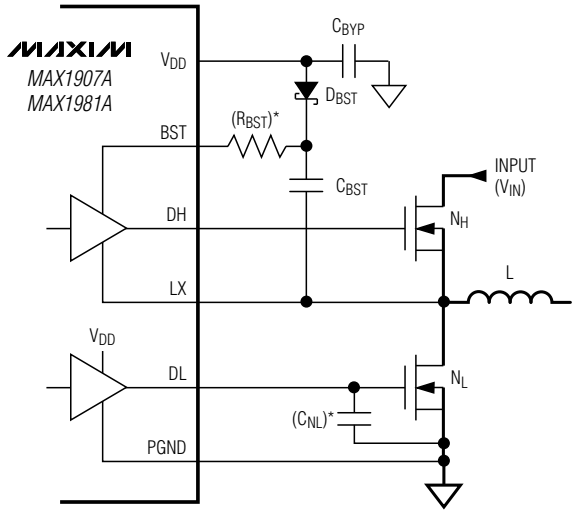
Lot-to-lot variation of the threshold voltage may cause problems in marginal designs. Typically, adding 4700pF between DL and power ground close to the low-side MOSFETs greatly reduces coupling. Due should not exceed 22nF of total gate capacitance to prevent excessive turn-off delays. Alternatively, adding a resistor less than 5Ω in series with BST may remedy the problem by increasing the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 5).

Voltage Positioning Amplifier

The MAX1907A/MAX1981A includes a dedicated operational amplifier for adding gain to the voltage positioning sense path. The voltage positioning gain allows the use of low-value, current-sense resistors in order to minimize power dissipation. This 3MHz gain-bandwidth amplifier was designed with low offset voltage (70µV, typ) to meet the IMVP-IV output accuracy requirements.

The inverting (OAIN-) and noninverting (OAIN+) inputs are used to differentially sense the voltage across the voltage-positioning sense resistor. The op amp's output is internally connected to the regulator's feedback input (FB). The op amp should be configured as a noninverting, differential amplifier as shown in Figure 1. The voltage positioning slope is set by properly selecting the feedback resistor connected from FB to OAIN- (see the *Setting Voltage Positioning* section). For applications using a slave controller, additional differential input resistors (summing configuration) should be connected to the slave's voltage-positioning sense resistor (Figure 1). Summing together both the master and slave current-sense signals ensures that the voltage-positioning slope will remain constant when the slave controller is disabled.

In applications that do not require voltage-positioning gain, the amplifier can be disabled by connecting the OAIN- pin directly to V_{CC}. The disabled amplifier's output becomes high-impedance, guaranteeing that the unused amplifier will not corrupt the FB input signal. The logic threshold to disable the op amp is approximately V_{CC} - 1V.



(RBST)* OPTIONAL—THE RESISTOR LOWERS EMI BY DECREASING THE SWITCHING NODE RISE TIME.
(CNL)* OPTIONAL—THE CAPACITOR REDUCES LX TO DL CAPACITIVE COUPLING THAT CAN CAUSE SHOOT-THROUGH CURRENTS.

Figure 5. High-Side Gate-Driver Boost Circuitry

Power-On Reset

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching, and forces the DL gate driver high (to enforce output overvoltage protection). When V_{CC} rises above 4.25V, the DAC inputs are sampled and the output voltage begins to slew to the boot voltage (Table 7).

For automatic startup, the battery voltage should be present before V_{CC}. If the MAX1907A/MAX1981A attempts to bring the output into regulation without the battery voltage present, the fault latch will trip. The $\overline{SHDN}$ pin can be toggled to reset the fault latch.

Input Undervoltage Lockout

During start-up, the V_{CC} UVLO circuitry forces the DL gate driver high and the DH gate driver low, inhibiting switching until an adequate supply voltage is reached. Once V_{CC} rises above 4.25V, valid transitions detected at the trigger input initiate a corresponding on-time pulse (see the *On-Time One-Shot* section).

If the V_{CC} voltage drops below 4.25V, it is assumed that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, DL is forced high in this mode to force the output to ground.

This results in large negative inductor current and possibly small negative output voltages. If V_{CC} is likely to drop in this fashion, the output can be clamped with a Schottky diode to PGND to reduce the negative excursion.

Shutdown

When $\overline{SHDN}$ or SYSPOK goes low, the MAX1907A/MAX1981A enters low-power shutdown mode. IMVPOK is pulled low and $\overline{CLKEN}$ is driven high immediately. The output voltage ramps down to 0 in 16mV steps at the clock rate set by R_{TIME}. When the DAC reaches the 0 setting, DL goes high, DH goes low, the reference is turned off, and the supply current drops to about 0.1µA. When SYSPOK activates the shutdown sequence, the controller also sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the MAX1907A/MAX1981A, toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V.

When $\overline{SHDN}$ goes high, the reference powers up, and after the reference UVLO is passed, the DAC target is evaluated and switching begins. The slew-rate controller ramps up from 0 in 16mV steps to the currently selected boot code value (see the *Power-Up Sequence* section). There is no traditional soft-start (variable current limit) circuitry, so full output current is available immediately. SYSPOK becomes high-impedance after the reference exceeds its UVLO threshold.

DAC Inputs (D0–D5)

During normal operation (SUS = low), the digital-to-analog converter (DAC) programs the output voltage using the D0–D5 inputs. D0–D5 are low-voltage (1V) logic inputs, designed to interface directly with the IMVP-IV CPU. Do not leave D0–D5 unconnected. D0–D5 can be changed while the MAX1907A/MAX1981A is active, initiating a transition to a new output voltage level. Change D0–D5 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages (Table 5) are compatible with IMVP-IV specification.

Four-Level Logic Inputs

TON, B0–B2, and S0–S2 are four-level logic inputs. These inputs help expand the functionality of the controller without adding an excessive number of pins. The four-level inputs are intended to be static inputs. When left open, an internal resistive divider sets the input voltage to approximately 3.5V. Therefore, connect the four-level logic inputs directly to V_{CC}, REF, or GND when selecting one of the other logic levels. See the *Electrical Characteristics* for exact logic-level voltages.

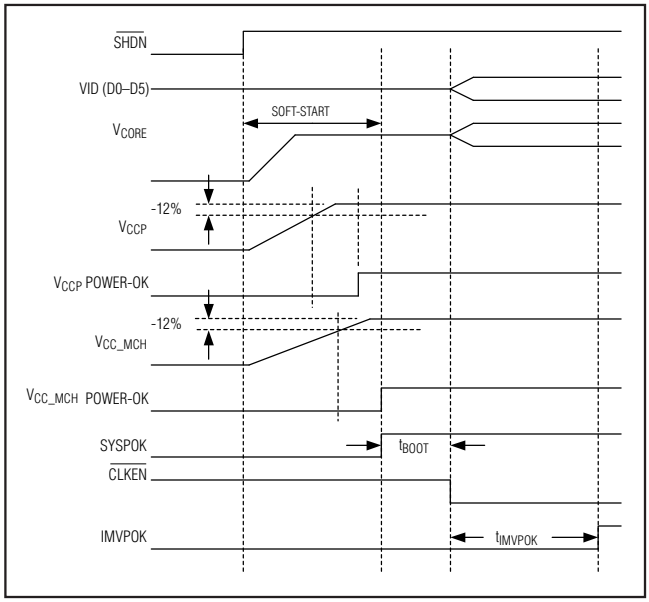


Figure 6. Power-Up Sequence Timing Diagram

Power-Up Sequence

The MAX1907A/MAX1981A is enabled when $\overline{SHDN}$ is driven high (Figure 6). First, the reference powers up. Once the reference exceeds its undervoltage lockout threshold, the PWM regulator becomes active. The slew-rate controller ramps up the output voltage in 16mV increments to the selected boot code value (B0–B2, Table 7). The ramp rate is set with the R_{TIME} resistor (see the *Output Voltage Transition Timing* section).

SYSPOK serves as the combined power-good input for V_{CCP} and V_{CC_MCH}. Once these supplies are within ±10% of their output voltage, their power good outputs become high-impedance, allowing SYSPOK to be pulled high. Approximately 50µs after the MAX1907A/MAX1981A detects a logic high voltage on SYSPOK and the FB voltage reaches the target voltage set by B0–B2, the controller pulls $\overline{CLKEN}$ low and slews the output to the proper operating voltage (see Table 4).

When $\overline{CLKEN}$ goes low, the MAX1907A/MAX1981A keeps IMVPOK low for an additional 3ms (min), guaranteeing that the CPU has time to start properly. If the MAX1907A/MAX1981A does not detect a fault, then IMVPOK will be pulled high once the 3ms timer expires.

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Table 4. Operating Mode Truth Table

$\overline{SHDN}$	SYSPOK	SUS	$\overline{DPSLP}$	$\overline{DDO}$	OUTPUT VOLTAGE	OPERATING MODE
0	x	x	x	0	GND	Low-Power Shutdown Mode. DL is forced high (V_{DD}), DH is forced low (LX), and the PWM controller is disabled. The supply current drops to 0.1µA (typ).
1	0	0	x	1	B0–B2 (No offset)	Power-Up Mode. When enabled, the MAX1907A/MAX1981A softly ramps up the output voltage to the selected boot voltage (B0–B2, Table 7). The controller remains at the boot voltage until SYSPOK is driven high (see the *Power-Up Sequence* section).
1	1	0	1	1	D0–D5 (No offset)	Normal Operation. The no-load output voltage is determined by the selected VID DAC code (D0–D5, Table 5).
1	1	0	0	0	D0–D5 (Plus offset)	Deep-Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D5, Table 5) plus the offset voltage set by POS and NEG. Operation with automatic PWM/PFM switchover for pulse skipping under light loads.
1	x	1	x	0	S0–S2 (No offset)	Suspend Mode. The no-load output voltage is determined by the selected suspend code (S0–S2, Table 6). Operation with automatic PWM/PFM switchover for pulse skipping under light loads.
1	0	x	x	0	GND	Fault Mode. The fault latch has been set by either UVP, OVP (MAX1907A only), thermal shutdown, or a falling edge on SYSPOK. The controller will remain in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

Table 5. Output Voltage VID DAC Codes (SUS = Low)

D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212

D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

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Table 6. Suspend Mode DAC Codes (SUS = High)

S2	S1	S0	OUTPUT VOLTAGE (V)
GND	GND	GND	1.452
GND	GND	REF	1.436
GND	GND	OPEN	1.420
GND	GND	V_{CC}	1.404
GND	REF	GND	1388
GND	REF	REF	1.372
GND	REF	OPEN	1.356
GND	REF	V_{CC}	1.340
GND	OPEN	GND	1.324
GND	OPEN	REF	1.308
GND	OPEN	OPEN	1.292
GND	OPEN	V_{CC}	1.276
GND	V_{CC}	GND	1.260
GND	V_{CC}	REF	1.244
GND	V_{CC}	OPEN	1.228
GND	V_{CC}	V_{CC}	1.212
REF	GND	GND	1.196
REF	GND	REF	1.180
REF	GND	OPEN	1.164
REF	GND	V_{CC}	1.148
REF	REF	GND	1.132
REF	REF	REF	1.116
REF	REF	OPEN	1.100
REF	REF	V_{CC}	1.084
REF	OPEN	GND	1.068
REF	OPEN	REF	1.052
REF	OPEN	OPEN	1.036
REF	OPEN	V_{CC}	1.020
REF	V_{CC}	GND	1.004
REF	V_{CC}	REF	0.988
REF	V_{CC}	OPEN	0.972
REF	V_{CC}	V_{CC}	0.956

S2	S1	S0	OUTPUT VOLTAGE (V)
OPEN	GND	GND	0.940
OPEN	GND	REF	0.924
OPEN	GND	OPEN	0.908
OPEN	GND	V_{CC}	0.892
OPEN	REF	GND	0.876
OPEN	REF	REF	0.860
OPEN	REF	OPEN	0.844
OPEN	REF	V_{CC}	0.828
OPEN	OPEN	GND	0.812
OPEN	OPEN	REF	0.796
OPEN	OPEN	OPEN	0.780
OPEN	OPEN	V_{CC}	0.764
OPEN	V_{CC}	GND	0.748
OPEN	V_{CC}	REF	0.732
OPEN	V_{CC}	OPEN	0.716
OPEN	V_{CC}	V_{CC}	0.700
V_{CC}	GND	GND	0.684
V_{CC}	GND	REF	0.668
V_{CC}	GND	OPEN	0.652
V_{CC}	GND	V_{CC}	0.636
V_{CC}	REF	GND	0.620
V_{CC}	REF	REF	0.604
V_{CC}	REF	OPEN	0.588
V_{CC}	REF	V_{CC}	0.572
V_{CC}	OPEN	GND	0.556
V_{CC}	OPEN	REF	0.540
V_{CC}	OPEN	OPEN	0.524
V_{CC}	OPEN	V_{CC}	0.508
V_{CC}	V_{CC}	GND	0.492
V_{CC}	V_{CC}	REF	0.476
V_{CC}	V_{CC}	OPEN	0.460
V_{CC}	V_{CC}	V_{CC}	0.444

Table 7. Boot-Mode DAC Codes (Power-Up)

B2	B1	B0	OUTPUT VOLTAGE (V)
GND	GND	GND	1.708
GND	GND	REF	1.692
GND	GND	OPEN	1.676
GND	GND	V_{CC}	1.660
GND	REF	GND	1.644
GND	REF	REF	1.628
GND	REF	OPEN	1.612
GND	REF	V_{CC}	1.596
GND	OPEN	GND	1.580
GND	OPEN	REF	1.564
GND	OPEN	OPEN	1.548
GND	OPEN	V_{CC}	1.532
GND	V_{CC}	GND	1.516
GND	V_{CC}	REF	1.500
GND	V_{CC}	OPEN	1.484
GND	V_{CC}	V_{CC}	1.468
REF	GND	GND	1.452
REF	GND	REF	1.436
REF	GND	OPEN	1.420
REF	GND	V_{CC}	1.404
REF	REF	GND	1.388
REF	REF	REF	1.372
REF	REF	OPEN	1.356
REF	REF	V_{CC}	1.340
REF	OPEN	GND	1.324
REF	OPEN	REF	1.308
REF	OPEN	OPEN	1.292
REF	OPEN	V_{CC}	1.276
REF	V_{CC}	GND	1.260
REF	V_{CC}	REF	1.244
REF	V_{CC}	OPEN	1.228
REF	V_{CC}	V_{CC}	1.212

B2	B1	B0	OUTPUT VOLTAGE (V)
OPEN	GND	GND	1.196
OPEN	GND	REF	1.180
OPEN	GND	OPEN	1.164
OPEN	GND	V_{CC}	1.148
OPEN	REF	GND	1.132
OPEN	REF	REF	1.116
OPEN	REF	OPEN	1.100
OPEN	REF	V_{CC}	1.084
OPEN	OPEN	GND	1.068
OPEN	OPEN	REF	1.052
OPEN	OPEN	OPEN	1.036
OPEN	OPEN	V_{CC}	1.020
OPEN	V_{CC}	GND	1.004
OPEN	V_{CC}	REF	0.988
OPEN	V_{CC}	OPEN	0.972
OPEN	V_{CC}	V_{CC}	0.956
V_{CC}	GND	GND	0.940
V_{CC}	GND	REF	0.924
V_{CC}	GND	OPEN	0.908
V_{CC}	GND	V_{CC}	0.892
V_{CC}	REF	GND	0.876
V_{CC}	REF	REF	0.860
V_{CC}	REF	OPEN	0.844
V_{CC}	REF	V_{CC}	0.828
V_{CC}	OPEN	GND	0.812
V_{CC}	OPEN	REF	0.796
V_{CC}	OPEN	OPEN	0.780
V_{CC}	OPEN	V_{CC}	0.764
V_{CC}	V_{CC}	GND	0.748
V_{CC}	V_{CC}	REF	0.732
V_{CC}	V_{CC}	OPEN	0.716
V_{CC}	V_{CC}	V_{CC}	0.700

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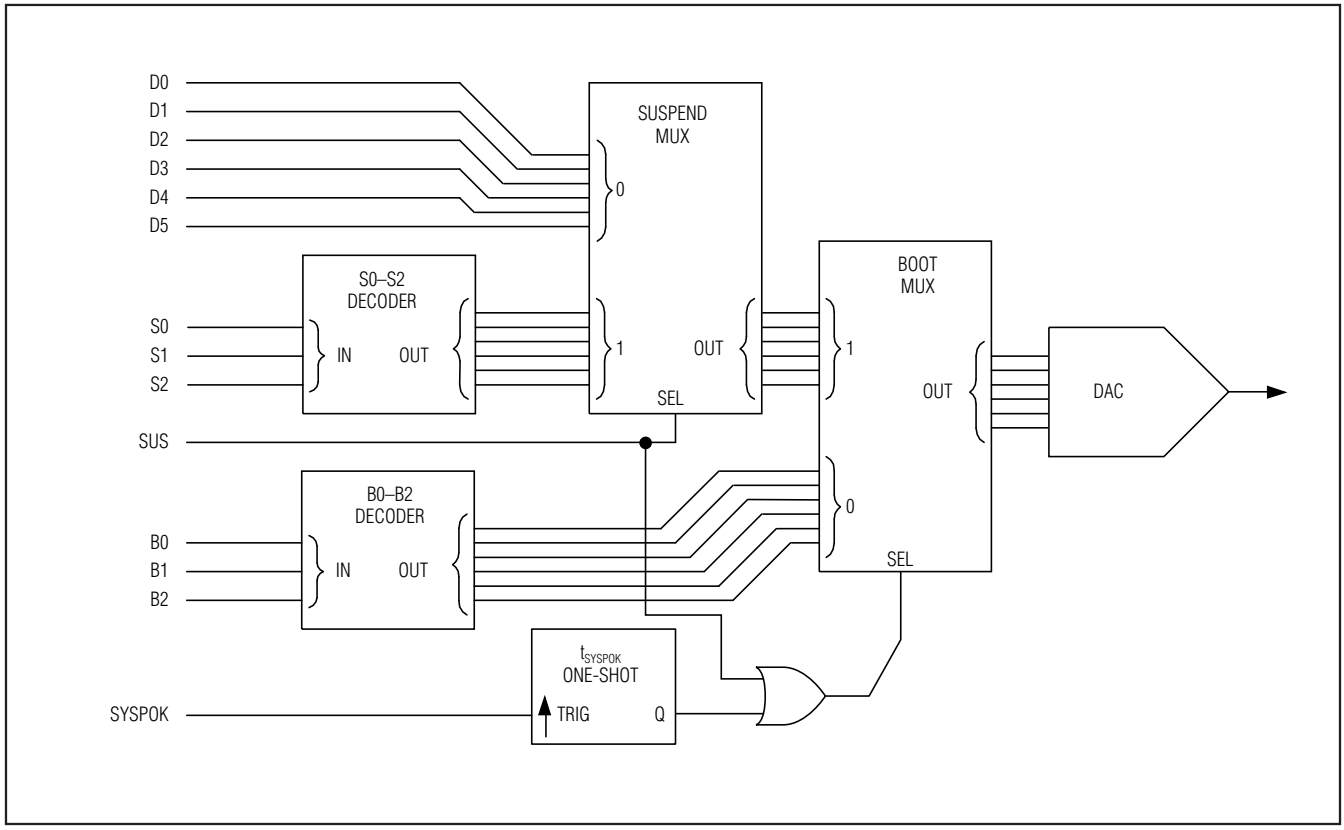

Figure 7. Internal Multiplexers Functional Diagram

Internal Multiplexers

The MAX1907A/MAX1981A has two unique internal DAC input multiplexers (muxes) that can select one of three different DAC code settings for different processor states. On startup, the controller selects the DAC code from the B0–B2 input decoder. Once SYSPOK goes high and the MAX1907A/MAX1981A properly regulates to the boot voltage, a second multiplexer selects the DAC code from either D0–D5 (SUS = low) or S0–S2 (SUS = high), depending on the SUS state (Figure 7).

Suspend Mode

When the processor enters low-power suspend mode, the system uses a lower supply voltage to reduce power consumption. The MAX1907A/MAX1981A include independent suspend-mode output voltage codes set by the four-level inputs S0–S2. When the CPU suspends operation, SUS is driven high, overriding the 6-bit VID DAC code set by D0–D5. The master controller slews the output to the selected suspend-mode voltage. During the transition, the MAX1907A/MAX1981A asserts forced-PWM operation until 62 R_{TIME} clock cycles after the slew-rate controller reaches the suspend-mode voltage.

When SUS is low, the output voltage is dynamically controlled by the 6-bit VID DAC inputs (D0–D5).

Output Voltage Transition Timing

The MAX1907A/MAX1981A is designed to perform mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance. This makes the IC ideal for IMVP-IV CPUs.

At the beginning of an output voltage transition, the MAX1907A/MAX1981A blanks the IMVPOK and $\overline{CLKEN}$ outputs, preventing them from changing states. IMVPOK and $\overline{CLKEN}$ remain blanked during the transition and is re-enabled 32 clock cycles after the slew-rate controller has set the final DAC code value. The slew-rate clock frequency (set by resistor R_{TIME}) must be set fast enough to ensure that the transition is completed within the maximum allotted time.

The slew-rate controller transitions the output voltage in 16mV increments during power-up, soft-shutdown, and suspend-mode transitions. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX1907A/MAX1981As' slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX1907A/MAX1981A automatically control the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less than the current limit set by ILIM. The transition time is given by:

$$t_{SLEW} \approx \frac{1}{f_{SLEW}} \left(\frac{V_{NEW} - V_{OLD}}{16mV} \right) \text{ for } V_{OUT} \text{ rising}$$

$$t_{SLEW} \approx \frac{1}{f_{SLEW}} \left[\left(\frac{V_{OLD} - V_{NEW}}{16mV} \right) + 2 \right] \text{ for } V_{OUT} \text{ falling}$$

where f_{SLEW} = 320kHz × 47kΩ / R_{TIME}, V_{OLD} is the original DAC setting, and V_{NEW} is the new DAC setting. The additional 2 clock cycles on the falling edge time are due to internal synchronization delays. See Time Frequency Accuracy in the *Electrical Characteristics* for f_{SLEW} accuracy.

The practical range of R_{TIME} is 23.5kΩ to 235kΩ corresponding to 1.6µs to 15.6µs per 16mV step. Although the DAC takes discrete 16mV steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times 16mV \times f_{SLEW}$$

Output Overvoltage Protection (MAX1907A Only)

The overvoltage protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The output voltage is continuously monitored for overvoltage. If the actual output voltage exceeds the set output voltage by more than 13% (min), OVP is triggered and the circuit shuts down. IMVPOK is pulled low and $\overline{CLKEN}$ is driven high immediately. The DL low-side gate-driver output is then latched high until $\overline{SHDN}$ is toggled or V_{CC} power is cycled below 1V. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow.

OVP can be defeated through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

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Output Undervoltage Shutdown

The output undervoltage protection (UVP) function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX1907A/MAX1981A output voltage is under 70% of the nominal value, the PWM is latched off and won't restart until $\overline{SHDN}$ is toggled or V_{CC} power is cycled below 1V. UVP is ignored during output voltage transitions and remains blanked for an additional 32 clock cycles after the controller reaches the final DAC code value.

UVP can be defeated through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

Thermal Fault Protection

The MAX1907A/MAX1981A features a thermal fault-protection circuit. When the junction temperature rises above 160°C, a thermal sensor activates the fault logic, forces the DL low-side gate-driver high, and pulls the DH high-side gate-driver low. This quickly discharges the output capacitors, tripping the master controller's UVLO protection. Toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V to reactivate the controller after the junction temperature cools by 15°C.

NO FAULT Test Mode

The OVP and UVP protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to disable the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. The NO FAULT test mode is entered by forcing 12V to 15V on $\overline{SHDN}$.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input Voltage Range. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high-AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery-selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Maximum Load Current. There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (ILOAD) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

For multi-phase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(SLAVE)} = I_{LOAD(MASTER)} = \frac{I_{LOAD}}{\eta}$$

where η is the number of phases.

Switching Frequency. This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

Setting Slave On-Time. The constant on-time control algorithm in the master results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. In the slave, the high-side switch on-time is inversely proportional to V+, and directly proportional to the compensation voltage (V_{COMP}):

$$t_{ON} = K\left(\frac{V_{COMP}}{V_{IN}}\right)$$

where K set by the TON pin-strap connection (Table 3).

Inductor Operating Point. This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

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Inductor Selection

The switching frequency and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)\eta}{V_{IN} f_{SW} I_{LOAD(MAX)} LIR}$$

where η is the number of phases. Example: η = 2, $I_{LOAD(MAX)}$ = 40A, V_{IN} = 12V, V_{OUT} = 1.3V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{1.3V \times \left(12V - 1.3V\right) \times 2}{12V \times 300kHz \times 40A \times 0.3} = 0.64\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(\frac{2 + LIR}{2\eta}\right)$$

where η is the number of phases.

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2\left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2\eta C_{OUT} V_{OUT}\left[\left(\frac{\left(V_{IN} - V_{OUT}\right)K}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*), η is the number of phases, and K is from Table 3.

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2\eta C_{OUT} V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at ILOAD(MAX) minus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > \left(\frac{I_{LOAD(MAX)}}{\eta}\right) - \left(\frac{I_{LOAD(MAX)} LIR}{2\eta}\right)$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the current-sense resistor (R_{SENSE}). For the 50mV default setting, the minimum current-limit threshold is 40mV.

Connect ILIM to V_{CC} for a default 50mV current-limit threshold. In adjustable mode, the current-limit threshold is precisely 1/10th the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to GND with ILIM connected to the center tap. The external 100mV to 2V adjustment range corresponds to a 10mV to 200mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and approximately 10µA divider current to prevent a significant increase of errors in the current-limit tolerance.

In multi-phase applications, set the slave's current-limit threshold above the MAX1907A/MAX1981As' current-limit threshold. This configuration ensures that the slave's current-limit circuitry will not disrupt the current balance required for stable multi-phase regulation. When the MAX1907A/MAX1981A limits the master inductor current, the slave's current-balance circuitry also limits the slave inductor current. However, if the current-balance circuitry fails, the slave controller's current limit provides back-up overcurrent protection.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

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In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For out-of-phase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\left(\frac{\eta}{L}\right)\left[\left(\frac{V_{IN} - \eta V_{OUT}}{f_{SW}}\right)\left(\frac{V_{OUT}}{V_{IN}}\right) - (\eta - 1)V_{OUT}t_{TRIG}\right]}$$

The previous equation can be rewritten as the single-phase ripple current minus a correction due to the additional phases:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\left[I_{LOAD(MAX)}LIR - \eta(\eta - 1)\left(\frac{V_{OUT}}{L}\right)(t_{ON} + t_{TRIG})\right]}$$

where t_{TRIG} is the propagation delay between the multiphase on-times, η is the number of phases, and K is from Table 3. When operating in-phase, the high-side MOSFETs turn on together, so the output capacitors must simultaneously support the combined inductor ripple currents of each phase. For in-phase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{I_{LOAD(MAX)}LIR}$$

$$R_{ESR} \le \frac{V_{RIPPLE}}{\left(\frac{\eta}{f_{SW}L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)(V_{IN} - V_{OUT})}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

$$\text{where } f_{ESR} = \frac{1}{2\pi R_{ESR}C_{OUT}}$$

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors, in widespread use at the time of publication, have typical ESR zero frequencies below 30kHz. In the standard application used for inductor selection, the ESR needed to support a 30mV$_{P-P}$ ripple is 30mV/(40A × 0.3) = 2.5mΩ. Five 330µF/2.5V Panasonic SP (type XR) capacitors in parallel provide 2mΩ (max) ESR. Their typical combined ESR results in a zero at 48kHz.

Do not put high-value ceramic capacitors directly across the output without taking precautions to ensure stability. Ceramic capacitors have a high-ESR zero frequency and can cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the junction of the inductor and FB pin.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The multi-phase slave controllers operate out-of-phase, staggering the turn-on times of each phase. This minimizes the input ripple current by dividing the load current among independent phases:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta}\right)\left(\frac{\sqrt{\eta V_{OUT}\left(V_{IN} - \eta V_{OUT}\right)}}{V_{IN}}\right)$$

for out-of-phase operation.

When operating the multiphase system in-phase, the high-side MOSFETs turn on simultaneously, so input capacitors must support the combined input ripple currents of each phase:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}\right)$$

for in-phase operation.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1907A/MAX1981A are operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK or D^2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(N_H\,Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta}\right)^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H\,Switching) = \frac{\left(V_{IN(MAX)}\right)^2 C_{RSS} f_{SW} I_{LOAD}}{I_{GATE}\eta}$$

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

where C_{RSS} is the reverse transfer capacitance of N_H and I_{GATE} is the peak gate-drive source/sink current (1A, typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied, due to the squared term in the $C \times V_{IN}^2 \times f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(N_L\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, it is possible to "over design" the circuit to tolerate:

$$I_{LOAD} = \eta I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum "valley" current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation. Choose a Schottky diode (D1) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to $1/(3\eta)$ of the load current. This diode is optional and can be removed if efficiency is not critical.

Setting Voltage Positioning

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the processor's power dissipation. When the output is loaded, an internal operational amplifier (Figures 2 and 8) increases the signal fed back to the master's feedback input. The additional gain provided by the op amp allows the use of low-value, current-sense resistors, significantly reducing the power dissipated in the current-sense resistors rather than connecting the feedback voltage directly to the current-sense resistor. The load-transient response of this control loop is extremely fast, yet well controlled, so the amount of voltage change can be accurately confined within the limits stipulated in the microprocessor power-supply guidelines. To understand the benefits of dynamically adjusting the output voltage, see the *Voltage Positioning and Effective Efficiency* section.

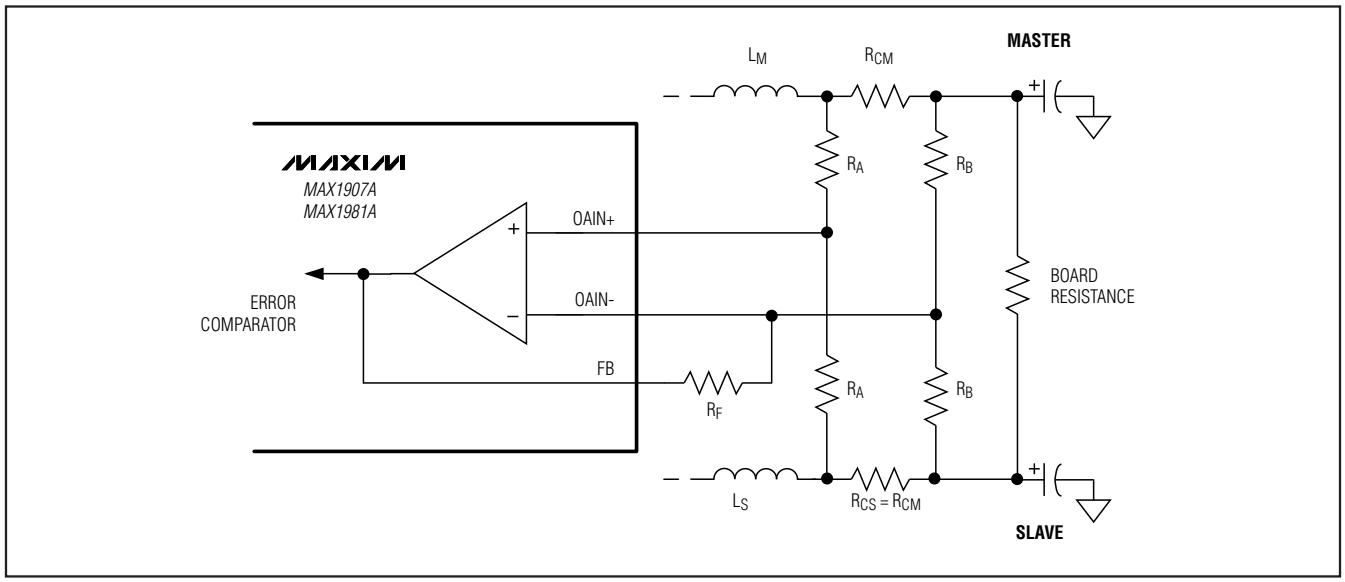

Figure 8. Voltage Positioning Gain

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The voltage-positioned circuit determines the load current from the voltage across the current-sense resistors ($R_{SENSE} = R_{CM} = R_{CS}$) connected between the inductors and output capacitors, as shown in Figure 8. The voltage drop may be determined by the following equation:

$$V_{VPS} = \left(1+\frac{\eta R_F}{R_B}\right)\left(\frac{I_{LOAD}}{\eta}\right) R_{SENSE}$$

$$V_{VPS} = \left(\frac{1}{\eta}+\frac{R_F}{R_B}\right) I_{LOAD} R_{SENSE}$$

where η is the number of phases summed together. When the slave controller is disabled, the current-sense summation maintains the proper voltage-positioned slope. Select the positive input-summing resistors using the following equation:

$$R_A = R_B \,||\, (\eta R_F)$$

Applications Information

Voltage Positioning and Effective Efficiency

Powering new mobile processors requires careful attention to detail to reduce cost, size, and power dissipation. As CPUs became more power hungry, it was recognized that even the fastest DC-DC converters were inadequate to handle the transient power requirements. After a load transient, the output instantly changes by $ESR_{COUT} \times \Delta I_{LOAD}$. Conventional DC-DC converters respond by regulating the output voltage back to its nominal state after the load transient occurs (Figure 9). However, the CPU only requires that the output voltage remain above a specified minimum value. Dynamically positioning the output voltage to this lower limit allows the use of fewer output capacitors and reduces power consumption under load.

For a conventional (non-voltage-positioned) circuit, the total voltage change is:

$$V_{P-P1} = 2 \times (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in Figure 10. Setting the converter to regulate at a lower voltage when under load allows a larger voltage step when the output current suddenly decreases (Figure 9). So the total voltage change for a voltage-positioned circuit is:

$$V_{P-P2} = 2 \times (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in the *Design Procedure* section. Since the amplitudes are the same for both circuits ($V_{P-P1} = V_{P-P2}$), the voltage-positioned circuit tolerates twice the ESR. Since the ESR specification is achieved by paralleling several capacitors, fewer units are needed for the voltage-positioned circuit.

An additional benefit of voltage positioning is reduced power consumption at high load currents. Since the output voltage is lower under load, the CPU draws less current. The result is lower power dissipation in the CPU, although some extra power is dissipated in R_{SENSE}. For a nominal 1.4V, 30A output (R_{LOAD} = 46.7mΩ), reducing the output voltage 7.1% gives an output voltage of 1.3V and an output current of 27.8A. Given these values, CPU power consumption is reduced from 42W to 36.1W. The additional power consumption of R_{SENSE} is:

$$1.5m\Omega \times (27.8A)^2 = 1.16W,$$

which results in an overall power savings of:

$$42W - (36.1W + 1.16W) = 4.7W.$$

In effect, 5.9W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial. Effective efficiency is defined as the efficiency required of a non-voltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

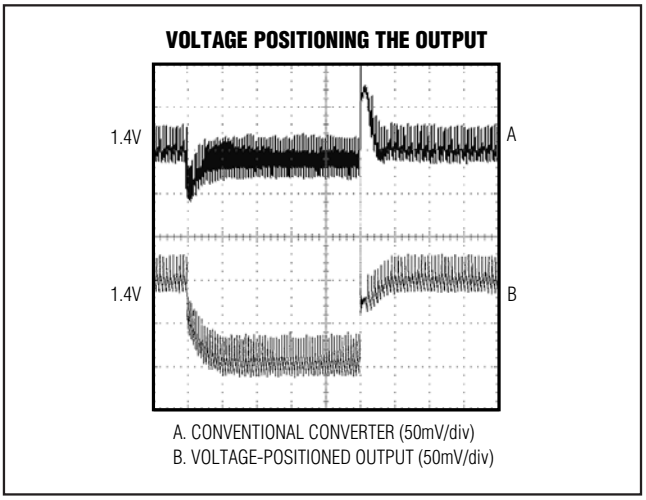

Figure 9. Voltage Positioning the Output

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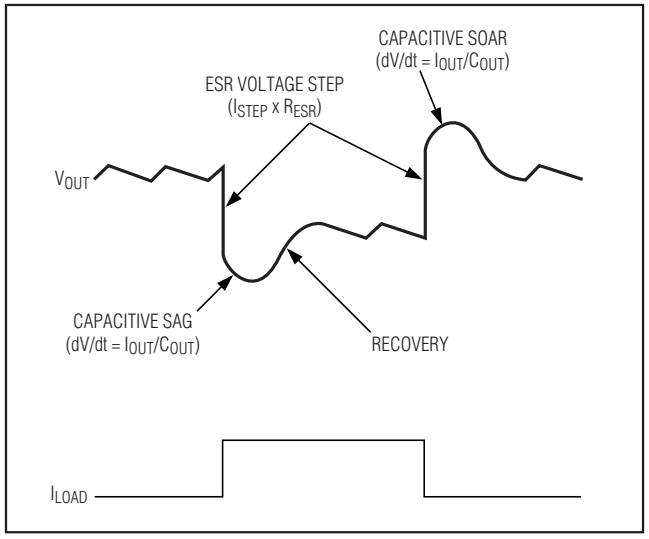


Figure 10. Transient Response Regions

Calculate effective efficiency as follows:

1) Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).
2) Model the load resistance for each data point:

$$R_{LOAD} = V_{OUT} / I_{OUT}$$

3) Calculate the output current that would exist for each R_{LOAD} data point in a non-positioned application:

$$I_{NP} = V_{NP} / R_{LOAD}$$

where V_{NP} = 1.6V (in this example).

4) Calculate effective efficiency as:

   Effective efficiency = ($V_{NP} \times I_{NP}$) / ($V_{IN} \times I_{IN}$) = calculated non-positioned power output divided by the measured voltage-positioned power input.

5) Plot the efficiency data point at the non-positioned current, I_{NP}.

   The effective efficiency of voltage-positioned circuits is shown in the *Typical Operating Characteristics*.

One-Stage (Battery Input) vs. Two-Stage (5V Input) Applications

The MAX1907A/MAX1981A can be used with a direct battery connection (one stage) or can obtain power from a regulated 5V supply (two stage). Each approach has advantages, and careful consideration should go into the selection of the final design.

The one-stage approach offers smaller total inductor size and fewer capacitors overall due to the reduced demands on the 5V supply. Due to the high input voltage, the one-stage approach requires lower DC input currents, reducing input connection/bus requirements and power dissipation due to input resistance. The transient response of the single stage is better due to the ability to ramp the inductor current faster. The total efficiency of a single stage is better than the two-stage approach.

The two-stage approach allows flexible placement due to smaller circuit size and reduced local power dissipation. The power supply can be placed closer to the CPU for better regulation and lower I^2R losses from PC board traces. Although the two-stage design has slower transient response than the single stage, this can be offset by the use of a voltage-positioned converter.

Ceramic Output Capacitor Applications

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR and are noncombustible, relatively small, and nonpolarized. However, they are also expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies. In addition, their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency), or there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored inductor energy. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The MAX1907A/MAX1981A can take full advantage of the small size and low ESR of ceramic output capacitors in a voltage-positioned circuit. The addition of the positioning resistor increases the ripple at FB, lowering the effective ESR zero frequency of the ceramic output capacitor.

Output overshoot (V_{SOAR}) determines the minimum output capacitance requirement (see the *Output Capacitor Selection* section). Often the switching frequency is increased to 550kHz, and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 550kHz is about 2% when compared to the 300kHz circuit, primarily due to the high-side MOSFET switching losses.

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 11). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the MAX1907A/MAX1981A. This includes the V_{CC} bypass capacitor, REF bypass capacitor, compensation (CC) capacitor, and the resistive-dividers connected to ILIM and POS/NEG.
3) The master controller should also have a separate analog ground. Return the appropriate noise sensitive components to this plane. Since the reference in the master is sometimes connected to the slave, it may be necessary to couple the analog ground in

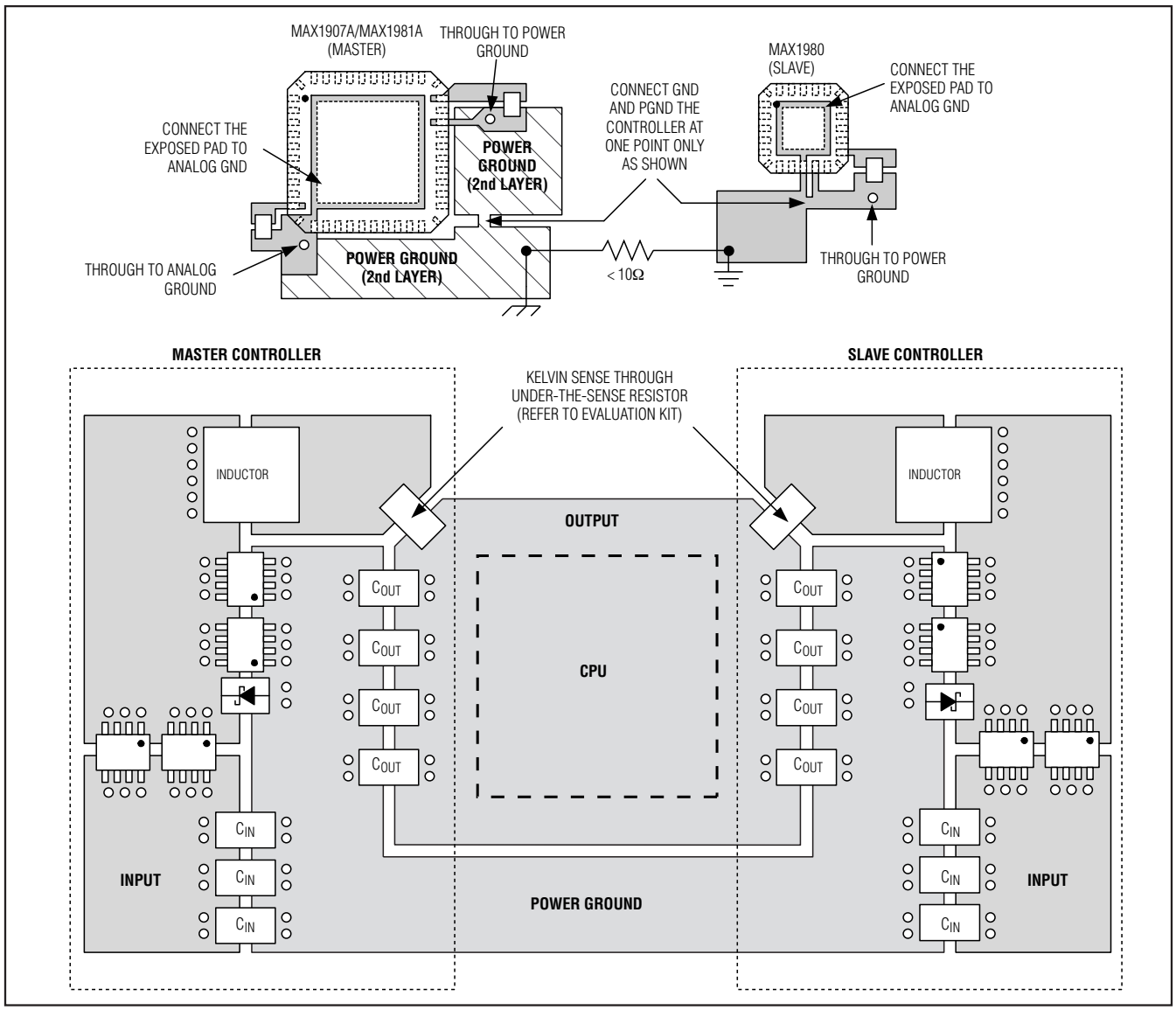


Figure 11. PC Board Layout Example

Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

the master to the analog ground in the slave to prevent ground offsets. A low value (≤10Ω) resistor is sufficient to link the two grounds.

4) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where 1mΩ of excess trace resistance causes a measurable efficiency penalty.
5) Keep the high-current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
6) CSP, CSN, OAIN+, and OAIN- connections for current limiting and voltage positioning must be made using Kelvin sense connections to guarantee the current-sense accuracy.
7) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
8) Route high-speed switching nodes away from sensitive analog areas (REF, COMP, ILIM, CSP, CSN, etc.). Make all pin-strap control input connections ($\overline{SHDN}$, ILIM, B0–B2, S0–S2, TON) to analog ground or V_{CC} rather than power ground or V_{DD}.

Layout Procedure

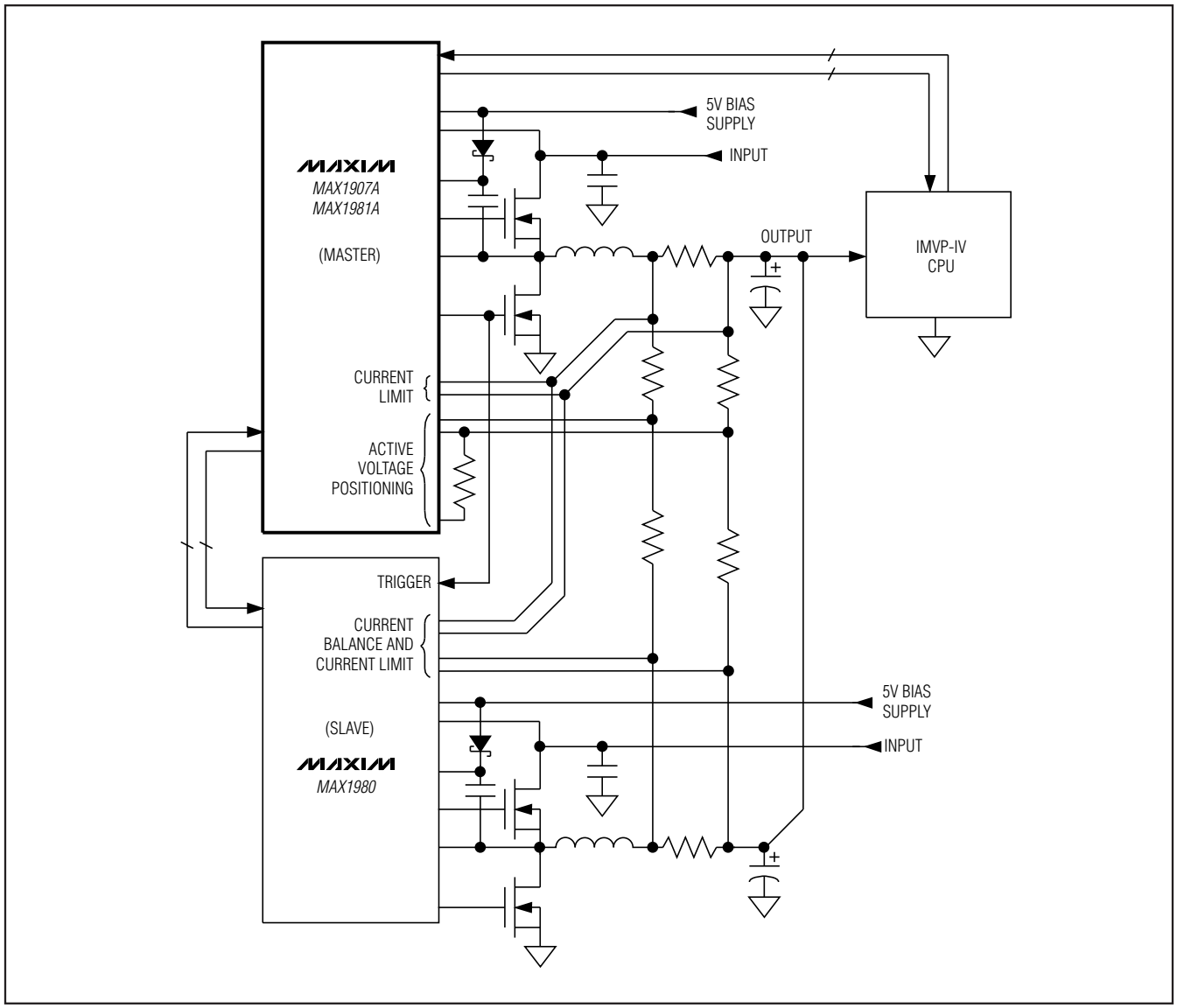
1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate trace must be short and wide (50mils to 100mils wide if the MOSFET is 1 inch from the controller IC).
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as having four separate ground planes: input/output ground (where all the high-power components go), the power ground plane (where the PGND pin and V_{DD} bypass capacitor go), the master's analog ground plane (where sensitive analog components such as the master's GND pin and V_{CC} bypass capacitor go), and the slave's analog ground plane (where the slave's GND pin and V_{CC} bypass capacitor go). The master's GND plane must meet the PGND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the PGND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

TRANSISTOR COUNT: 8713

PROCESS: BiCMOS

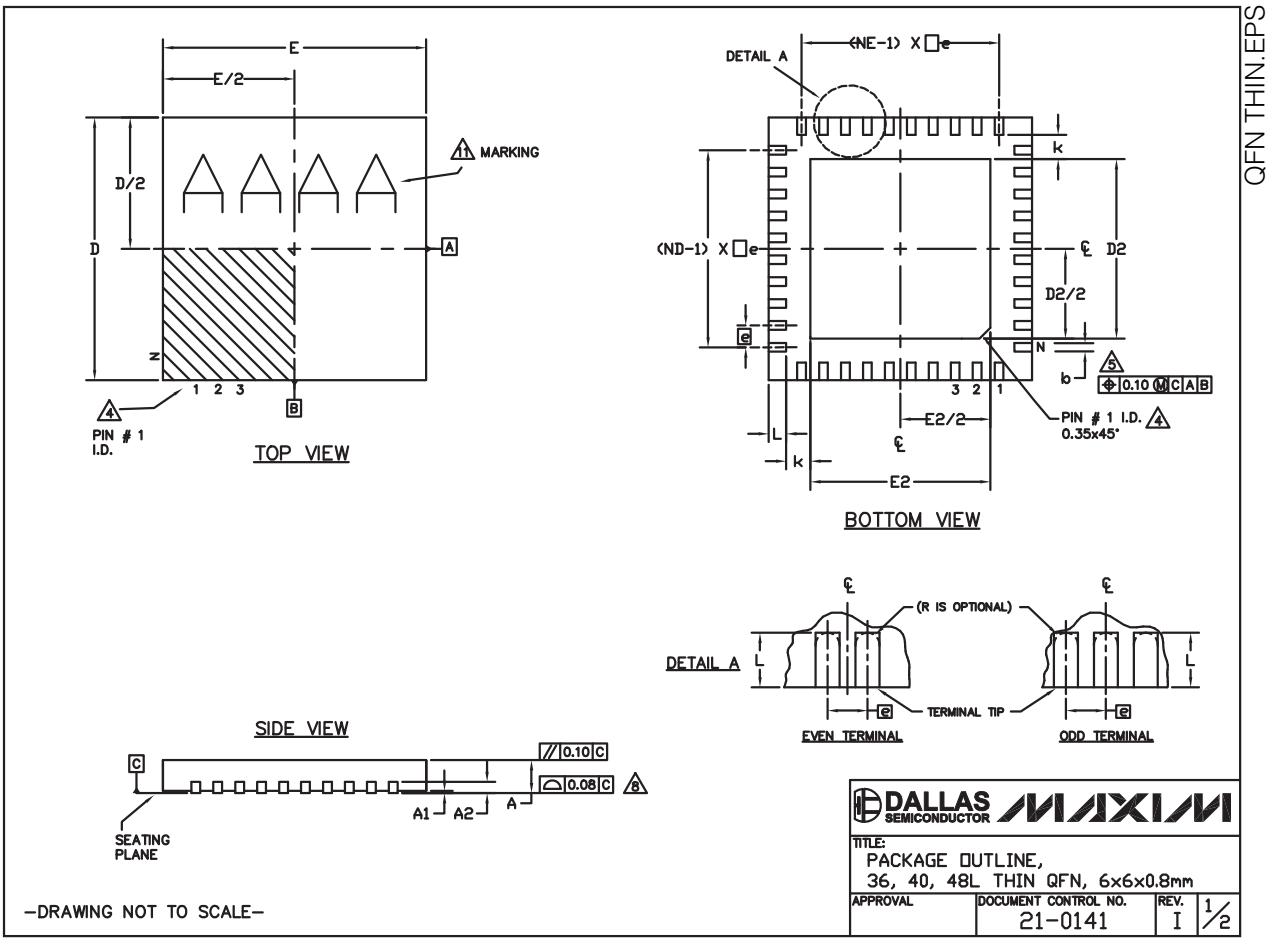
Typical Operating Circuit



Quick-PWM Master Controllers for Voltage-Positioned CPU Core Power Supplies (IMVP-IV)

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2		0.20 REF.			0.20 REF.			0.20 REF.	
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e		0.50 BSC.			0.50 BSC.			0.40 BSC.	
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N		36			40			48	
ND		9			10			12	
NE		9			10			12	
JEDEC		WJJD-1			WJJD-2			–	

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	I	2/2