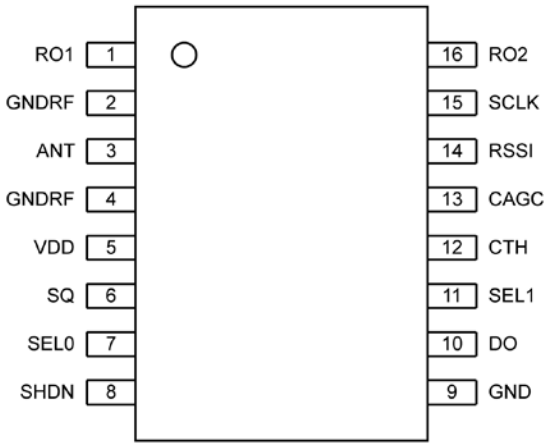
Ordering Information

Part Number	Temperature Range	Package
MICRF219AAYQS	–40°C to +105°C	16-Pin QSOP

Pin Configuration



MICRF219AAYQS

Pin Description

Pin Number	Pin Name	Pin Function
1	RO1	Reference resonator connection to the Pierce oscillator. May also be driven by external reference signal of 200mVp-p to 1.5V p-p amplitude maximum. Internal capacitance of 7pF to GND during normal operation.
2	GNDRF	Ground connection for ANT RF input. Connect to PCB ground plane.
3	ANT	Antenna Input: RF Signal Input from Antenna. Internally AC coupled. It is recommended to use a matching network with an inductor to RF ground to improve ESD protection.
4	GNDRF	Ground connection for ANT RF input. Connect to PCB ground plane.
5	VDD	Positive supply connection for all chip functions. Bypass with 0.1µF capacitor located as close to the VDD pin as possible.
6	SQ	Squelch Control Logic-Level Input. An internal pull-up (5µA typical) pulls the logic-input HIGH when the device is enabled. This feature is not recommended in MICRF219A and this pin should remain floating.
7	SEL0	Tie this pin to VDD to ensure robust register programming. Use register bits D[4:3] to set demodulation bandwidth.
8	SHDN	Shutdown Control Logic-Level Input. A logic-level LOW enables the device. A logic-level HIGH places the device in low-power shutdown mode. An internal pull-up (5µA typical) pulls the logic input HIGH. To ensure that the part starts up correctly, connect a 1µF capacitor from VDD to SHDN, and a 50kΩ resistor from SHDN pin to GND. After the supply voltage settles, apply a HIGH logic level voltage to SHDN to turn the part off, then a LOW logic level voltage to turn the part on before programming or operating the device.
9	GND	Ground connection for all chip functions except for RF input. Connect to PCB ground plane.
10	DO	Data Output. Demodulated data output. A current limited CMOS output during normal operation, 25kΩ pull-down is present when device is in shutdown.
11	SEL1	Tie this pin to VDD to ensure robust register programming. Use register bits D[4:3] to set demodulation bandwidth.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
12	CTH	Demodulation Threshold Voltage Integration Capacitor. Connect a 0.1µF capacitor from CTH pin to GND to provide a stable slicing threshold.
13	CAGC	AGC Filter Capacitor. Connect a capacitor from this pin to GND. Refer to the *AGC Loop and CAGC* section for information on the capacitor value.
14	RSSI	Received Signal Strength Indicator. The voltage on this pin is an inversed amplified version of the voltage on CAGC. Output is from a switched capacitor integrating op amp with 250Ω typical output impedance.
15	SCLK	Programming clock input.
16	RO2	Reference resonator connection to the Pierce oscillator. Internal capacitance of 7pF to GND during normal operation.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +5V
SQ, SEL0, SEL1, SCLK,
SHDN DC Voltage. ..... –0.3V to V_{DD} + 0.3V
ANT DC Voltage ..... -0.3V to +0.3V
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec.) ..... +300°C
Storage Temperature (T_S) ..... –65°C to +150°C
Maximum Receiver Input Power ..... +10dBm
ESD Rating[3] ..... 3kV HBM

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +105°C
Maximum Input RF Power 0dBm
Receive Modulation Duty Cycle ..... 20% to 80%
Frequency Range ..... 300MHz to 450MHz

Electrical Characteristics[4]

V_{DD} = 3.3V, V_{SHDN} = 0V, SQ = open, C_{CAGC} = 4.7µF, C_{CTH} = 0.1µF, unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ 105°C. "Bit rate" refers to the encoded bit rate throughout this datasheet (see Note 4).

Parameter	Condition	Min.	Typ.	Max.	Units
Operating Supply Current	Continuous Operation, f_{RF} = 315MHz		4.3		mA
	Continuous Operation, f_{RF} = 433.92MHz		6.0		
Sleep Current	Only sleep clock is on		13		µA
Shutdown Current	$V_{SHDN} = V_{DD}$		0.1		µA
Receiver					
Conducted Receiver Sensitivity @ 1kbps (Note 5)	433.92MHz, D[4:3] = 00, BER = 1%		–112.5		dBm
	433.92MHz, D[4:3] = 00, BER = 0.1%		–110		
	315MHz, D[4:3] = 01, BER = 1%		–112.5		
	315MHz, D[4:3] = 01, BER = 0.1%		–110		
Image Rejection	$f_{IMAGE} = f_{RF} – 2f_{IF}$		25		dB
IF Center Frequency (f_{IF})	f_{RF} = 315MHz		0.85		MHz
	f_{RF} = 433.92MHz		1.18		
–3dB IF Bandwidth	f_{RF} = 315MHz		235		kHz
	f_{RF} = 433.92MHz		330		
CAGC Voltage Range	–40dBm RF input level		1.15		V
	–100dBm RF input level		1.55		
Reference Oscillator					
Reference Oscillator Frequency	f_{RF} = 315MHz		9.81713		MHz
	f_{RF} = 433.92MHz		13.52313		
Reference Buffer Input Impedance	RO1 when driven externally		1.6		kΩ
Reference Oscillator Bias Voltage	RO2		1.15		V
Reference Oscillator Input Range	External input, AC couple to RO1	0.2		1.5	V_{P-P}
Reference Oscillator Source Current	V_{RO1} = 0V		300		µA

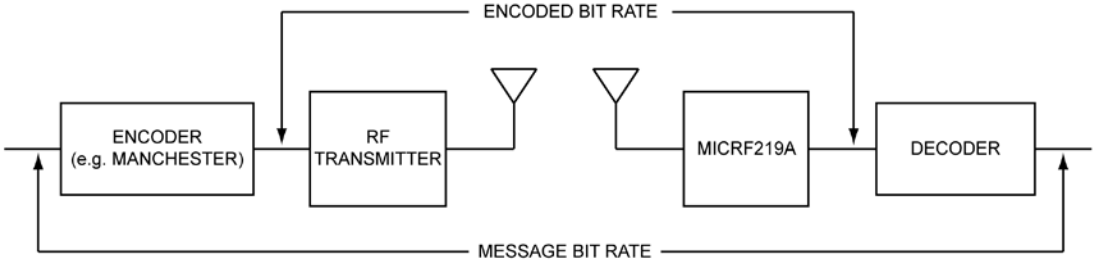
Electrical Characteristics[4] (Continued)

V_{DD} = 3.3V, V_{SHDN} = 0V, SQ = open, C_{CAGC} = 4.7µF, C_{CTH} = 0.1µF, unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ 105°C. "Bit rate" refers to the encoded bit rate throughout this datasheet (see Note 4).

Parameter	Condition	Min.	Typ.	Max.	Units
Demodulator					
CTH Source Impedance, Note 6	f_{REF} = 9.81713MHz		165		kΩ
	f_{REF} = 13.52313MHz		120		
CTH Leakage Current In CTH Hold Mode	T_A = +25ºC T_A = +105ºC		1 10		nA
Digital / Control Functions					
DO Pin Output Current	As output source @ 0.8V_{DD} As output sink @ 0.2V_{DD}		300 680		µA
Output Rise Time	15pF load on DO pin, transition time between 0.1V_{DD} and 0.9V_{DD}		600		ns
Output Fall Time			200		
Input High Voltage	SHDN, SQ	0.8V_{DD}			V
Input Low Voltage	SHDN, SQ			0.2V_{DD}	V
Output Voltage High	DO	0.8V_{DD}			V
Output Voltage Low	DO			0.2V_{DD}	V
RSSI					
RSSI DC Output Voltage Range	–110dBm RF input level		0.5		V
	–50dBm RF input level		2.0		
RSSI Output Current	5kΩ load to GND, –50dBm RF input level		400		µA
RSSI Output Impedance			250		Ω
RSSI Response Time	D[4:3] = 00, RF input power stepped from no input to –50dBm		10		ms

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside of its operating rating.
3. Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.
4. Encoded bit rate is 1/(shortest pulse duration) that appears at MICRF219A DO pin:

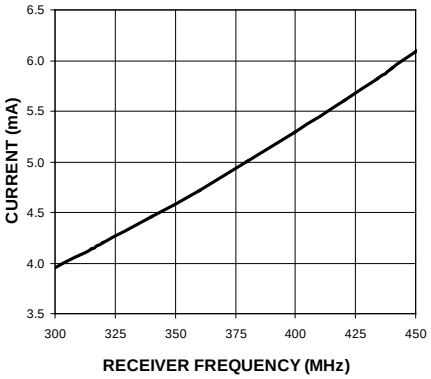


5. In an ON/OFF keyed (OOK) signal, the signal level goes between a "mark" level (when the RF signal is ON) and a "space" level (when the RF signal is OFF). Sensitivity is defined as the input signal level when "ON" necessary to achieve a specified BER (bit error rate). BER measured with the built-in BERT function in Agilent E4432B using PN9 sequence. Sensitivity measurement values are obtained using an input matching network corresponding to 315MHz or 433.92MHz.
6. CTH source impedance is inversely proportional to the reference frequency. In production test, the typical source impedance value is verified with 12MHz reference frequency.

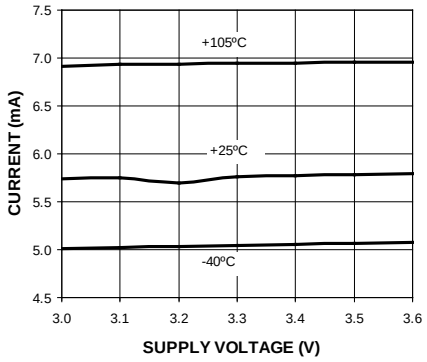
Typical Characteristics

V_{DD} = 3.3V, T_A = +25°C, BER measured with PN9 sequence, unless otherwise noted.

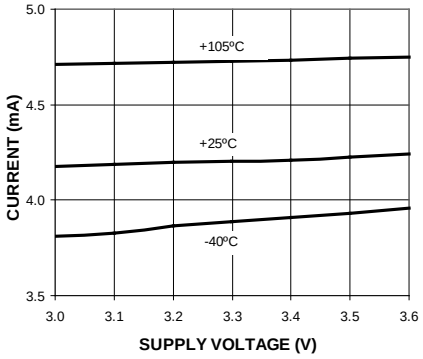
Current vs. Receiver Frequency



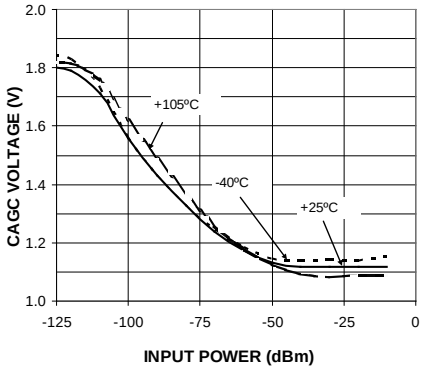
Current vs. Supply Voltage
f_{RF} = 433.92MHz



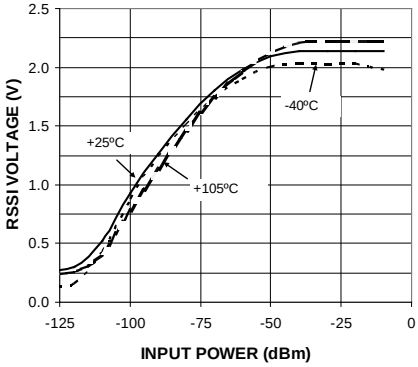
Current vs. Supply Voltage
f_{RF} = 315MHz



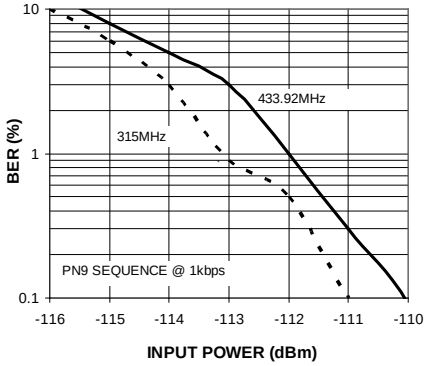
CAGC Voltage vs. Input Power



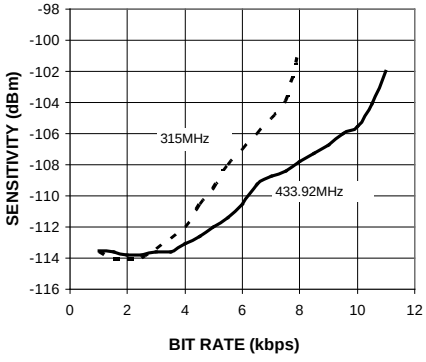
RSSI vs. Input Power



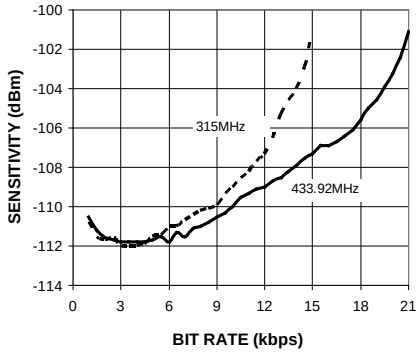
BER vs. Input Power
D[4:3] = 00



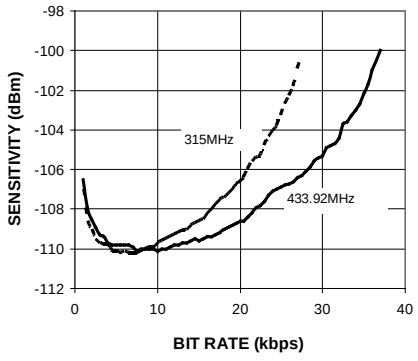
Sensitivity at 1% BER
D[4:3] = 00



Sensitivity at 1% BER
D[4:3] = 01



Sensitivity at 1% BER
D[4:3] = 10



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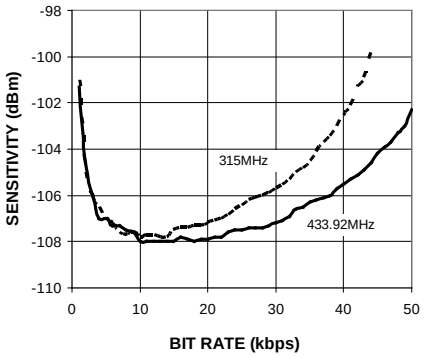
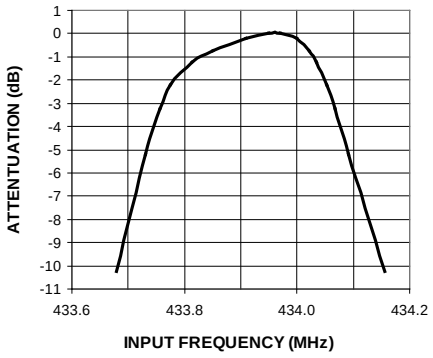
Typical Characteristics (Continued)

V_{DD} = 3.3V, T_A = +25°C, BER measured with PN9 sequence, unless otherwise noted.

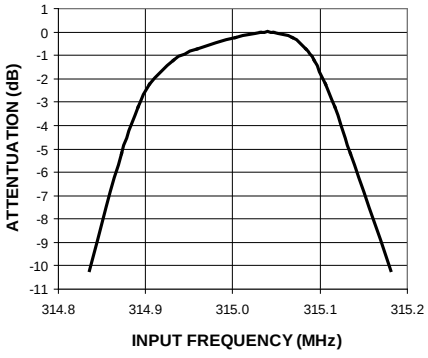
Sensitivity at 1% BER
D[4:3] = 11



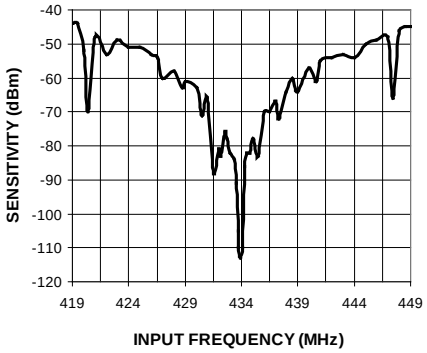
Bandpass Filter Attenuation
f_{XTAL} = 13.52313MHz



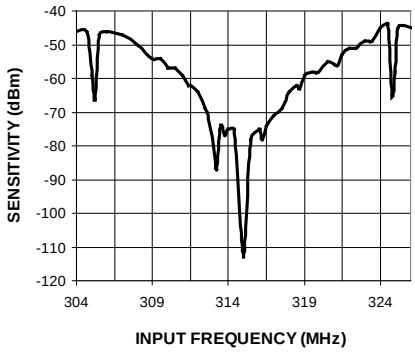
Bandpass Filter Attenuation
f_{XTAL} = 9.81713MHz



Sensitivity for 1% BER vs.
Frequency, f_{XTAL} = 13.52313MHz



Sensitivity for 1% BER vs.
Frequency, f_{XTAL} = 9.81713MHz



Functional Diagram

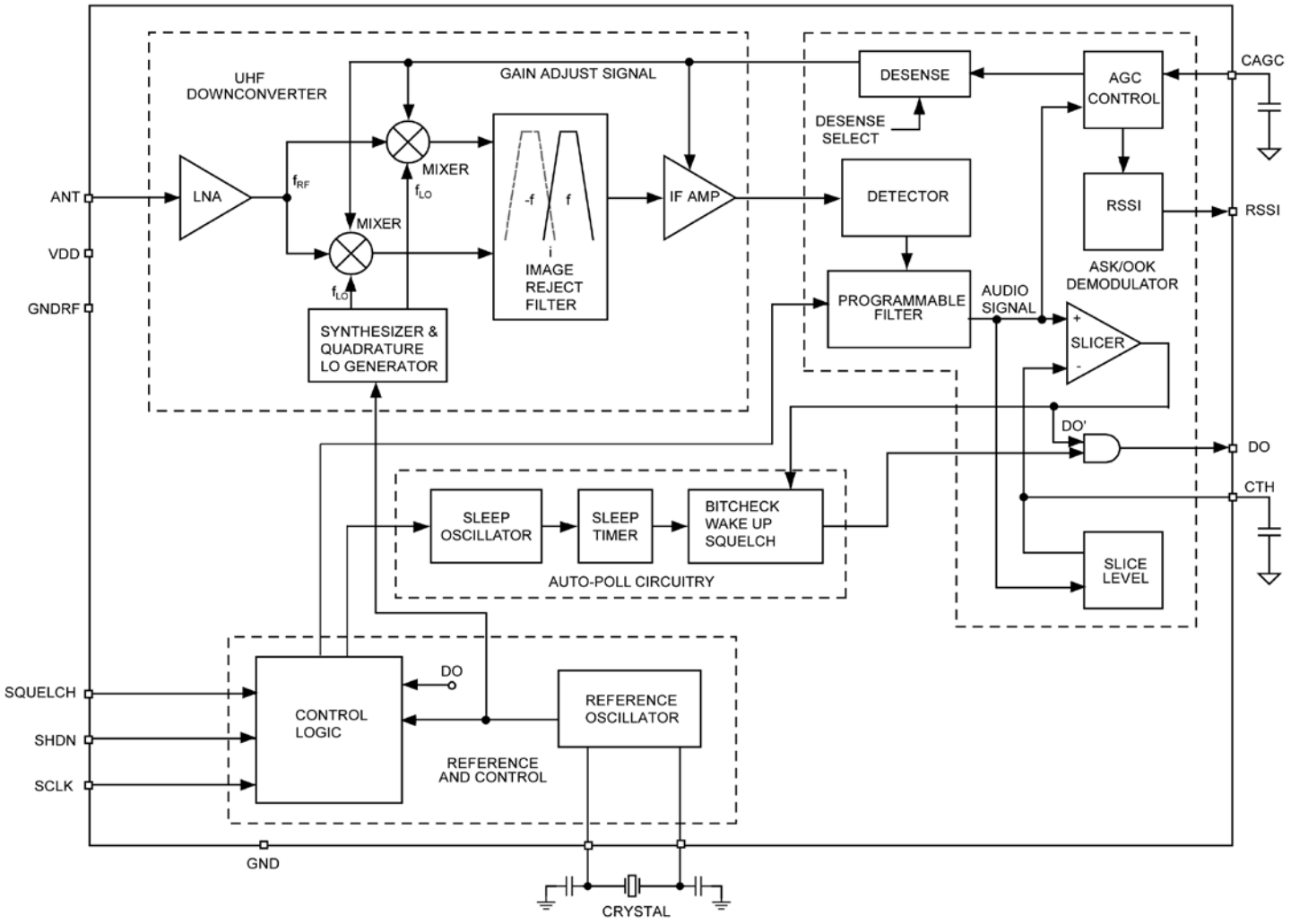


Figure 1. Simplified Block Diagram

Functional Description

The simplified block diagram (Figure 1) illustrates the basic structure of the MICRF219A receiver. It is made up of four sub-blocks:

- UHF Down-Converter
- ASK/OOK Demodulator
- Reference and Control logic
- Auto-poll circuitry

Outside the device, the MICRF219A receiver requires just a few components to operate: a capacitor from CAGC to GND, a capacitor from CTH to GND, a reference crystal resonator with associated loading capacitors, LNA input matching components, and a power-supply decoupling capacitor.

Receiver Operation

UHF Downconverter

The UHF down-converter has six sub-blocks: LNA, mixers, synthesizer, image reject filter, band pass filter and IF amplifier.

LNA

The RF input signal is AC-coupled into the gate of the LNA input device. The LNA configuration is a cascoded common source NMOS amplifier. The amplified RF signal is then fed to the RF ports of two double balanced mixers.

Mixers and Synthesizer

The LO ports of the mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal (Figure 2). The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will be demodulated by the detector of the device. The image reject mixer suppresses the image frequency which is below the wanted signal by 2x the IF frequency. The local oscillator frequency (f_{LO}) is set to 32x the crystal reference frequency (f_{REF}) via a phase-locked loop synthesizer with a fully-integrated loop filter:

$$f_{LO} = 32 \times f_{REF} \qquad \text{Eq. 1}$$

MICRF219A uses an IF frequency scheme that scales the IF frequency (f_{IF}) with f_{REF} according to:

$$f_{IF} = f_{REF} \times \frac{87}{1000} \qquad \text{Eq. 2}$$

Therefore, the reference frequency f_{REF} needed for a given desired RF frequency (f_{RF}) is approximately:

$$f_{REF} = f_{RF} / \left(32 + \frac{87}{1000}\right) \qquad \text{Eq. 3}$$

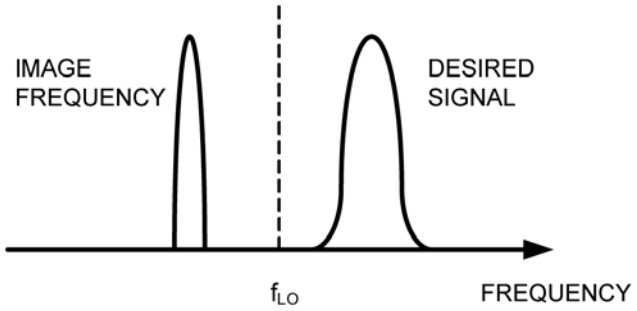


Figure 2. Low-Side Injection Local Oscillator

Image-Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature-down converted IF signals. These IF signals are low-pass filtered to remove higher frequency products prior to the image reject filter where they are combined to reject the image frequency. The IF signal then passes through a third order band pass filter. The IF bandwidth is 330kHz @ 433.92MHz, and will scale with RF operating frequency according to:

$$BW_{IF} = BW_{IF@433.92\ MHz} \times \left(\frac{\text{Operating Freq (MHz)}}{433.92}\right) \qquad \text{Eq. 4}$$

These filters are fully integrated inside the MICRF219A.

After filtering, four active gain controlled amplifier stages enhance the IF signal to its proper level for demodulation.

ASK/OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes baseband information. The low-pass filter further enhances the baseband signal. There are four selectable low-pass filter BW settings: 1625Hz, 3250Hz, 6500Hz, and 13000Hz for 433.92MHz operation. The low-pass filter BW is directly proportional to the crystal reference frequency, and hence RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. Equation 5 illustrates filter Demod BW calculation:

$$BW_{Operating\ Freq} = BW_{@433.92MHz} \times \left(\frac{Operating\ Freq\ (MHz)}{433.92} \right)$$

Eq. 5

It is very important to select a suitable low-pass filter BW setting for the required data rate to minimize bit error rate. Use the operating curves that show BER vs. bit rates for different D[4:3] settings as a guide.

This low-pass filter –3dB corner, or the demodulation BW, is set at 13000Hz @ 433.92MHz as default (assuming both SEL0 and SEL1 pins are connected to V_{DD}). The low-pass filter can be set by changing register bits D[4:3]. Table 2 demonstrates the scaling for 315MHz RF frequency:

D[4]	D[3]	Low-Pass Filter BW	Maximum Encoded Bit Rate
0	0	1625Hz	2.5kbps
0	1	3250Hz	5kbps
1	0	6500Hz	10kbps
1	1	13000Hz	20kbps

Table 1. Low-Pass Filter Selection @ 434MHz RF input

D[4]	D[3]	Low-Pass Filter BW	Maximum Encoded Bit Rate
0	0	1170Hz	1.8kbps
0	1	2350Hz	3.6kbps
1	0	4700Hz	7.2kbps
1	1	9400Hz	14.4kbps

Table 2. Low-Pass Filter Selection @ 315MHz RF input

Slicer and CTH

The signal prior to the slicer, labeled “Audio Signal” in Figure 1, is still baseband analog signal. The data slicer converts the analog signal into ones and zeros based on 50% of the slicing threshold voltage built up in the CTH capacitor. After the slicer, the signal is demodulated OOK digital data. When there is only thermal noise at ANT pin, the voltage level on CTH pin is about 650mV. This voltage starts to drop when there is RF signal present. When the RF signal level is greater than –100dBm, the voltage is about 400mV.

The value of the capacitor from CTH pin to GND is not critical to the sensitivity of MICRF219A, although it should be large enough to provide a stable slicing level for the comparator. The value used in the evaluation board of 0.1µF is good for all bit rates from 500bps to 20kbps.

CTH Hold Mode

If the internal demodulated signal (DO’ in Figure 1) is at logic LOW for more than about 4msec, the chip automatically enters CTH hold mode, which holds the voltage on CTH pin constant even without RF input signal. This is useful in a transmission gap, or “deadtime”, used in many encoding schemes. When the signal reappears, CTH voltage does not need to re-settle, improving the time to output with no pulse width distortion, or time to good data (TTGD).

AGC Loop and CAGC

The AGC comparator monitors the signal amplitude from the output of the programmable low-pass filter. The AGC loop in the chip regulates the signal at this point to be at a constant level when the input RF signal is within the AGC loop dynamic range (about –115dBm to –40dBm).

When the chip first turns on, the fast charge feature charges the CAGC node up with 120µA typical current. When the voltage on CAGC increases, the gains of the mixer and IF amplifier go up, increasing the amplitude of the audio signal (as labeled in Figure 1), even with only thermal noise at the LNA input. The fast-charge current is disabled when the audio signal crosses the slicing threshold, causing DO’ to go high, for the first time.

When an RF signal is applied, a fast attack period ensues, when 600µA current discharges the CAGC node to reduce the gain to a proper level. Once the loop reaches equilibrium, the fast attack current is disabled, leaving only 15µA to discharge CAGC or 1.5µA to charge CAGC. The fast attack current is enabled only when the RF signal increases faster than the ability of the AGC loop to track it.

The ability of the chip to track to a signal that DECREASED in strength is much slower, since only 1.5µA is available to charge CAGC to increase the gain. When designing a transmitter that communicates with the MICRF219A, ensure that the power level remains constant throughout the transmit burst.

The value of CAGC impacts the time to good data (TTGD), which is defined as the time when signal is first applied, to when the pulse width at DO is within 10% of the steady state value. The optimal value of CAGC depends on the setting of the D4 and D3 bits. A smaller CAGC value does NOT always result in a shorter TTGD. This is due to the loop dynamics, the fast discharge current being 600µA, and the charge current being only 1.5µA. For example, if D4 = D3 = 0, the low pass filter bandwidth is set to a minimum and CAGC capacitance is too small, TTGD will be longer than if CAGC capacitance is properly chosen. This is because when RF signal first appears, the fast discharge period will reduce V_{CAGC} very fast, lowering the gain of the mixer and IF amplifier. But since the low pass filter bandwidth is low, it takes too long for the AGC comparator to see a reduced level of the audio signal, so it can not stop the discharge current. This causes an undershoot in CAGC voltage and a corresponding overshoot in RSSI voltage. Once CAGC undershoots, it takes a long time for it to charge back up because the current available is only 1.5µA.

Table 3 lists the recommended minimum CAGC values for different D[4:3] settings to insure that the voltage on CAGC does not undershoot. The recommendation also takes into account the behavior in auto-polling. If CAGC is too small, the chip can have a tendency to false wake up (DO releases even when there is no input signal).

D4	D3	CAGC value
0	0	4.7µF
0	1	2.2µF
1	0	1µF
1	1	1µF

Table 3. Minimum Suggested CAGC Values

Figure 3 illustrates what occurs if CAGC capacitance is too small for a given D[4:3] setting. Here, D[4:3] = 01, the capacitance on CAGC pin is 0.47µF, and the RF input level is stepped from no signal to −100dBm. RSSI voltage is shown instead of CAGC voltage because RSSI is a buffered version of CAGC (with an inversion and amplification). Probing CAGC directly can affect the loop dynamics through resistive loading from a scope probe, especially in the state where only 1.5µA is available, whereas probing RSSI does not. When RF signal is first applied, RSSI voltage overshoots due to the fast discharge current on CAGC, and the loop is too slow to stop this fast discharge current in time. Since the voltage on CAGC is too low, the audio signal level is lower than the slicing threshold (voltage on CTH), and DO pin is low. Once the fast discharge current stops, only the small 1.5µA charge current is available in settling the AGC loop to the correct level, causing the recovery from CAGC undershoot/RSSI overshoot condition to be slow. As a result, TTGD is about 9.1ms.

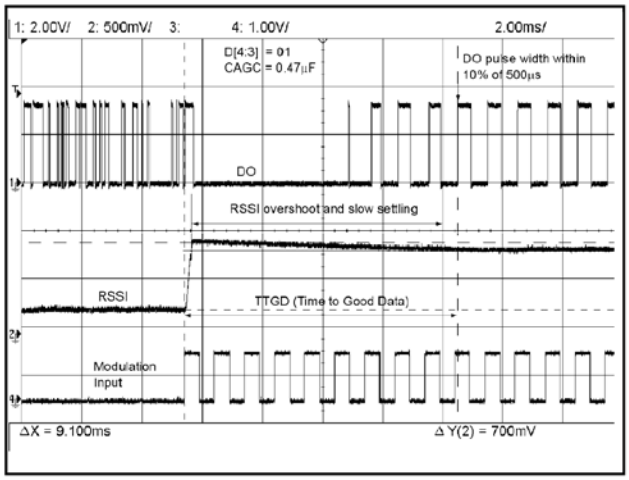


Figure 3. RSSI Overshoot and Slow TTGD (9.1ms)

Figure 4 shows the behavior with a larger capacitor on CAGC pin (2.2µF), D[4:3] = 01. In this case, V_{CAGC} does not undershoot (RSSI does not overshoot), and TTGD is relatively short at 1ms.

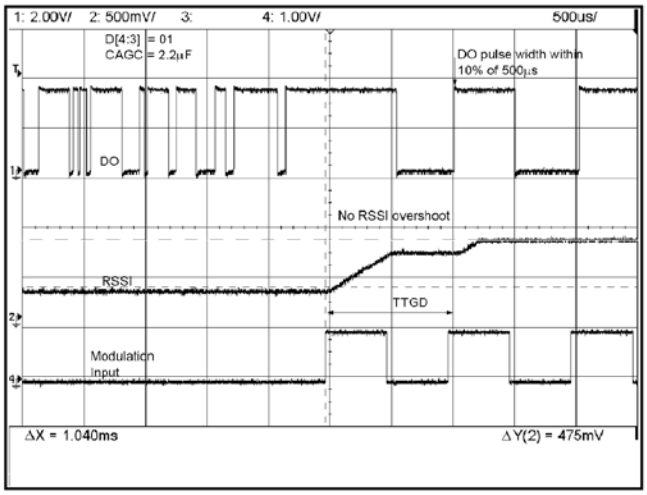


Figure 4. Proper TTGD (1ms) with Sufficient CAGC

Reference Oscillator

The reference oscillator in the MICRF219A (Figure 5) uses a basic Pierce crystal oscillator configuration with MOS transconductor. Though the MICRF219A has built-in load capacitors for the crystal oscillator, the external load capacitors are still required for tuning it to the right frequency. RO1 and RO2 are external pins of the MICRF219A to connect the crystal to the reference oscillator.

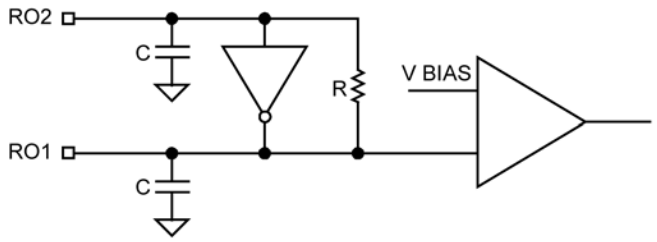


Figure 5. Reference Oscillator Circuit

Reference oscillator crystal frequency can be calculated using Equation 3. For example, if f_{RF} = 433.92MHz, f_{REF} = 13.52313MHz. Table 4 lists the values of reference frequencies at different popular RF frequencies. To operate the MICRF219A with minimum offset, use proper loading capacitance recommended by the crystal manufacturer.

RF Input Frequency (MHz)	Reference Frequency (MHz)
315.0	9.81713*
390.0	12.15446
418.0	13.02708
433.92	13.52313*

*Empirically derived, slightly different from Equation 3.

Table 4. Reference Frequency Examples

Auto-Polling

The MICRF219A can be programmed into an auto-polling mode by setting register bit D[15] to 1, where it monitors if there is a valid incoming RF signal while holding DO low. In this mode, the chip goes between sleep state and polling state. In sleep state, only a low power sleep clock is on, resulting in very low current consumption of 13µA typical. The sleep time is programmable from 10ms to 1.28s. In a polling state, every block in the MICRF219A is on, and the chip looks for signal with bit durations greater than a user-programmed value. This operation is subsequently called “bit checking” in this datasheet. A “valid bit” is a mark or space with duration that is longer than the bit check window. A “bad bit” is a mark or space with duration that is shorter than the bit check window. The user can set different bit check window time to suit a particular signal by programming register bits D[11:9] as listed in the register programming section. The number of consecutive valid bits before releasing DO and exiting polling mode can also be set by register bits D[8:7].

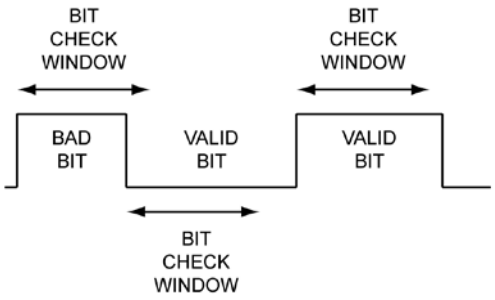


Figure 6. One Bad Bit Followed by Two Valid Bits

During the bit checking operation, DO is held low while the bit checker examines the pulse widths at the node labeled DO’ in Figure 1. If there is no signal present and DO’ randomly chatters, the MICRF219A returns to sleep after seeing 4 consecutive bad bits.

Note that since DO’ randomly chatters with no signal present, the amount of time it takes for 4 consecutive bad bits to happen is random. Therefore, the duration of polling time is random without signal.

If enough consecutive valid bits are found, DO is released and the MICRF219A stays on in the continuous receive mode. Once the chip is in continuous receive mode, it will not go back to sleep automatically when RF signal is removed. The register bits must be programmed again to put the MICRF219A back into auto-polling mode.

Serial Interface Register Programming

There are twenty register bits in MICRF219A. The functions are described in the following tables.

D19	Always set this bit to 0

D18	Always set this bit to 1

SQ Pin	D17	
0	0	Not recommended
0	1	Squelch Circuit Disabled
1	0	Squelch Circuit Disabled (default)
1	1	Not recommended

D16	Always set this bit to 0

D15	Auto-Poll Enable
0	Awake – does not poll - default
1	Auto-polls with sleep periods

D14	D13	D12	Set Sleep Time
0	0	0	10ms
0	0	1	20ms
0	1	0	40ms Default
0	1	1	80ms
1	0	0	160ms
1	0	1	320ms
1	1	0	640ms
1	1	1	1280ms

D11	D10	D9	Set Bit-Check Window Time (315 MHz, time in µs)			
			D4=1 D3=1	D4=1 D3=0	D4=0 D3=1	D4=0 D3=0
0	0	0	98	196	393	785
0	0	1	92	183	367	733
0	1	0	85	170	341	681
0	1	1	79	157	314	629
1	0	0	72	144	288	577
1	0	1	66	131	262	525
1	1	0	59	118	236	473
1	1	1	53	105	210	420

D11	D10	D9	Set Bit-Check Window Time (433.92 MHz, time in µs)			
			D4=1 D3=1	D4=1 D3=0	D4=0 D3=1	D4=0 D3=0
0	0	0	71	143	285	570
0	0	1	67	133	266	532
0	1	0	62	124	247	494
0	1	1	57	114	228	457
1	0	0	52	105	209	419
1	0	1	48	95	190	381
1	1	0	43	86	172	343
1	1	1	38	76	152	305

Default value of D[11:9] = 111.

D8	D7	Set number of consecutive valid bits before releasing DO
0	0	0 bit - default
0	1	4
1	0	8
1	1	16

D6	D5	Set slice level
0	1	Slice Level 30%
1	0	Slice Level 40%
1	1	Slice Level 50% - default
0	0	Slice Level 60%

D4	D3	Demod Bandwidth (at 433.92MHz)
0	0	1625Hz
0	1	3250Hz
1	0	6500Hz
1	1	13000Hz - default

D0	D1	D2	
0	X	X	default
1	0	0	Not recomended
1	1	0	Not recomended
1	0	1	Not recomended
1	1	1	Not recomended

Programming the device is accomplished by the use of pins DO and SCLK. Normally, DO (Pin 10) is outputting data and needs to switch to an input pin made by the start sequence, as shown at Figure 7.

High at the SCLK pin tri-states the DO pin, enabling the external drive into the DO pin with an initial low level. The start sequence is completed by taking SCLK low, then high while DO is low, followed by taking DO high, then low while SCLK is high. The serial interface is initialized and ready to receive the programming data.

SCLK frequency should be greater than 5kHz to avoid automatic reset from internal circuitry.

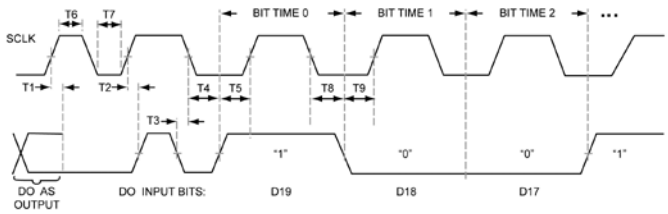


Figure 7. Serial Interface Start Sequence

Bits are serially programmed starting with the most significant bit (MSB = D19) if all bits are being programmed until the least significant bit (LSB =D0) For instance, if only the bits D0, D1, and D2 are being programmed, then these are the only bits that need to be programmed with the start sequence, D2, D1, D0, plus the stop sequence. Or, if only the bit D17 is needed, then the sequence must be from start sequence, D17 through D0 plus the stop sequence, making sure the other bits (besides D17) are programmed as needed. It is recommended that all parallel input pins (SEL0, SEL1, and SQ) be kept high when using the serial interface. After the programming bits are finished, a stop sequence (as shown in Figure 8) is required to end the mode and re-establish the DO pin as an output again. To do so, the SCLK pin is kept high while the DO pin changes from low to high, then low again, followed by the SCLK pin made low. Timing of the programming bits are not critical, but should be kept as shown below:

T1 < 0.1 us, Time from SCLK to convert DO to input pin

T6 > 0.1 us, SCLK high time

T7 > 0.1 us, SCLK low time

T2, T3, T4, T5, T8, T9, T10 > 0.1 us

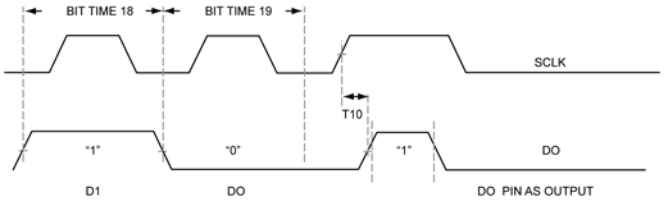


Figure 8. Serial Interface Stop Sequence

Serial Interface Register Loading Examples

See Figures 9 to 11. (Channel 1 is the DO pin, and channel 2 is the SCLK pin).

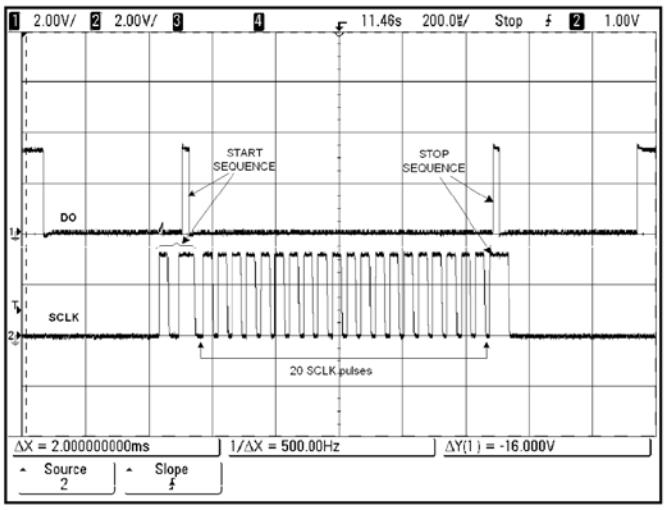


Figure 9. All Bits D19 through D0 = 0

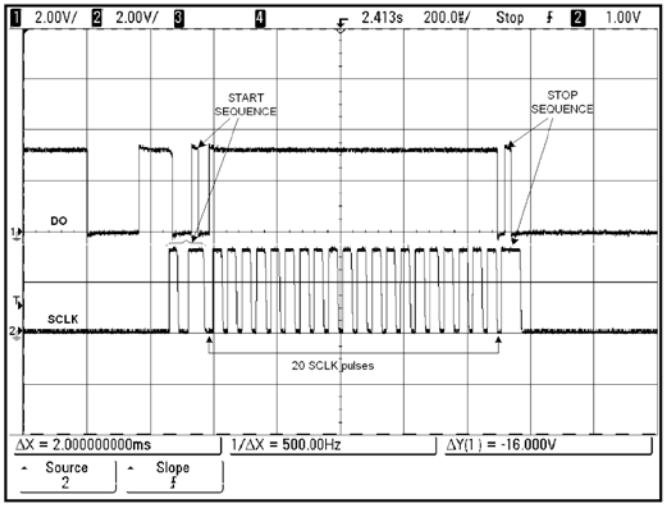


Figure 10. All Bits D19 through D0 = 1

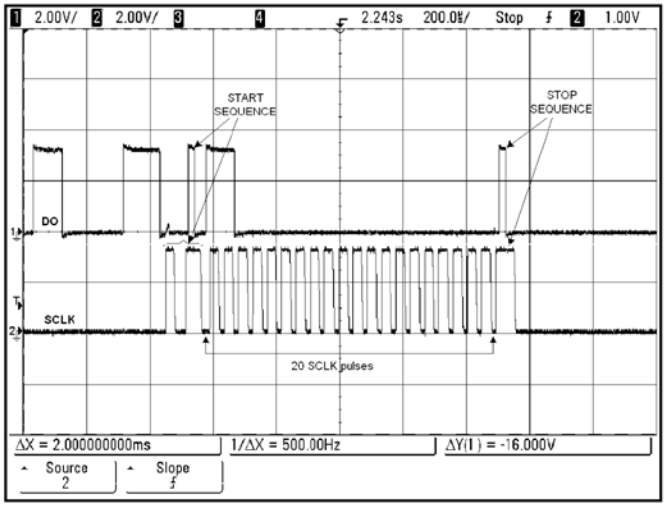


Figure 11. D[19:18] = 11, D[17:0] = All 0s

Auto-Poll Programming Example

RF frequency 433.92MHz, bit rate 1kbps, bit width 1ms.

D[19] = 0, AGC fast attack enabled

D[18] = 1, watchdog timer is OFF

D[17] = 0,

D[16] = 0

D[15] = 1, device is placed in autopoll

D[14:12] = 100, sleep time 160ms

D[11:9] = 011, bit check window time 457µs with D[4:3] = 00

D[8:7] = 10, number of consecutive valid bits is 8

D[6:5] = 11, slice level 50%

D[4:3] = 00, demodulator bandwidth = 1.625kHz

D[2:0] = 000

From MSB to LSB, see Table 5:

D19	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**
0	1	0	0	1	1	0	0
D11	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	
0	1	1	1	0	1	1	
D4	**D3**	**D2**	**D1**	**D0**			
0	0	0	0	0			

Table 5. Auto-Poll example bit sequence.

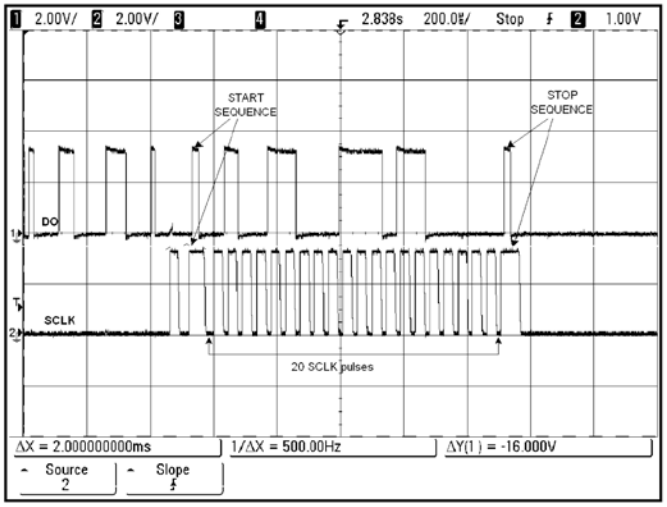


Figure 12. Auto-Poll Example

As noted in the Absolute Maximum Ratings section, the voltage on SCLK can go up to V_{DD} + 0.3V without causing damage. But applying V_{DD} + 0.3V to SCLK can put the part in an unknown test mode. If this accidently happens, cycle the power supply to restore the part to normal operation.

Application Information

Initial Startup

When supply voltage is initially applied, it should rise monotonically from 0V to 3.3V to ensure proper startup of the crystal oscillator and the PLL. It should not have multiple bounces across 2.6V, which is the threshold of the undervoltage lockout (UVLO) circuit inside MICRF219A. The SHDN pin needs to have 50kΩ resistor to GND and a coupling capacitor to VDD as shown in the evaluation board schematic to ensure that the part starts up in shutdown mode first. Then the micro controller can bring the SHDN pin voltage down to turn the part on.

Length of Preamble

When using MICRF219A in auto-polling mode, the preamble of the corresponding transmitter should be long enough to guarantee that the MICRF219A becomes fully awake during the preamble portion of the burst. This way the entire data portion will be received. A good rule of thumb to use is:

Preamble length = 1.2 x sleep time + length of valid bits sequence

The factor of 1.2 is to accommodate sleep time variation due to process shift.

Figure 13 shows an example of insufficient length preamble. MICRF219A starts checking bits during the data portion of the burst, so by the time it becomes fully awake and releases DO, part of the data portion is lost. In Figure 14, the preamble length is sufficient. The chip wakes up during the preamble and is ready for the data portion.

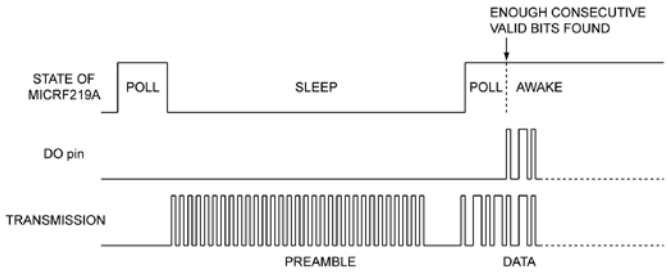


Figure 13. Preamble Length Too Short

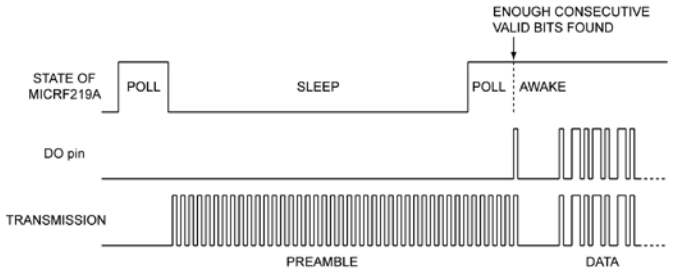


Figure 14. Sufficient Preamble Length

Antenna and RF Port Connections

The evaluation board offers two options of injecting the RF input signal: through a PCB antenna or through a 50Ω SMA connector. The SMA connection allows for conductive testing, or an external antenna.

Low-Noise Amplifier Input Matching

Capacitor C3 and inductor L2 form the “L” shape input matching network to the SMA connector. The capacitor cancels out the inductive portion of the net impedance after the shunt inductor, and provides additional attenuation for low-frequency outside band noise. The inductor is chosen to over resonate the net capacitance at the pin, leaving a net-positive reactance and increasing the real part of the impedance. It also provides additional ESD protection for the antenna pin. The input impedance of the device is listed in Table 6 to aid calculation of matching values. Note that the net impedance at the pin is easily affected by component pads parasitic due to the high input impedance of the device. The numbers in Table 6 does NOT include trace and component pad parasitic capacitance, which total about 0.75pF on the evaluation board.

The matching components to the PCB antenna (L3 and C9) were empirically derived for best over-the-air reception range.

Frequency (MHz)	Z Device (Ω)
315	23 – j290
390	14 – j230
418	17 – j216
433.92	12 – j209

Table 6. Input Impedance for the Most Used frequencies

Crystal Selection

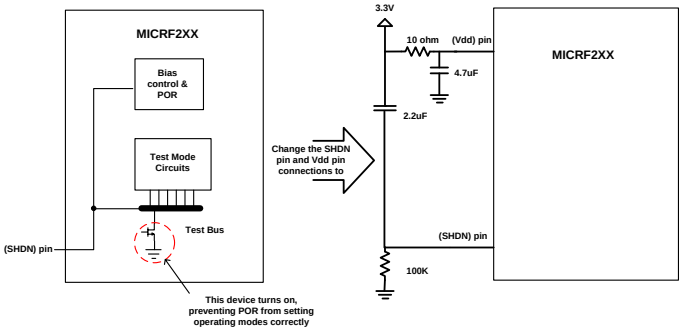
The crystal resonator provides a reference clock for all the device internal circuits. Crystal tolerance needs to be chosen such that the down-converted signal is always inside the IF bandwidth of MICRF219A. From this consideration, the tolerance should be ±50ppm on both the transmitter and the MICRF219A side. The ESR should be less than 300Ω, and the temperature range of the crystal should match the range required by the application. With the Abracon crystal listed in the Bill of Materials, a typical MICRF219A crystal oscillator still starts up at +105ºC with additional 400Ω series resistance.

The oscillator of the MICRF219A is a Pierce-type oscillator. Good care must be taken when laying out the printed circuit board. Avoid long traces and place the ground plane on the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and the crystals used are not verified, the oscillator may not start or takes longer to start. Time-to-good-data will be longer as well.

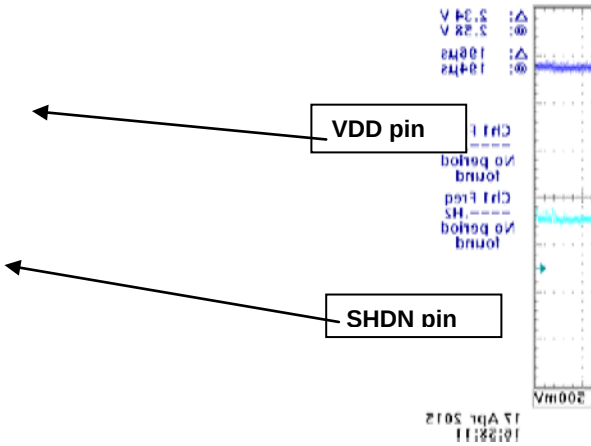
Important Note

A few customers have reported that some MICRF219A receiver do not start up correctly. When the issue occurs, DO either chatters or stays at low voltage level. An unusual operating current is observed and the part cannot receive or demodulate data even when a strong OOK signal is present.

Micrel has confirmed that this is the symptom of incorrect power on reset (POR) of internal register bits. The MICRF219A is designed to start up in shutdown mode (SHDN pin must be in logic high during Vdd ramp up). When the SHDN pin is tied to GND, and if the supply is ramped up slowly, a “test bus pull down” circuit may be activated. Once the chip enters this mode, the POR does not have the chance to set register bits (and hence operating modes) correctly. The test bus pull down acts on the SHDN pin, and can be illustrated in the following diagram.



To prevent the erroneous startup, a simple RC network is recommended. The 10Ω resistor and the 4.7µF capacitor provide a delay of about 200µs between the VDD and SHDN during the power up, thus ensuring the part to enter to shutdown stage before the part is actually turned on. The 2.2µF capacitor bootstraps the voltage on SHDN, ensuring that SHDN voltage leads the supply voltage on VDD during the power up. This gives the POR circuit time to set internal register bits. The SHDN pin can be brought low to turn the chip on once the initialization is completed. The 2.2µF and 100kΩ network form a RC delay of about 200ms before the SHDN pin is brought to low again. The 100kΩ resistor discharges the SHDN pin to turn the chip on.

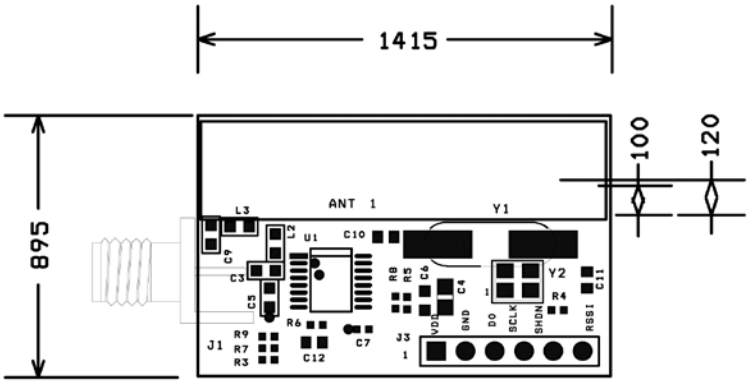


The suggestion provided above will generally serve to prevent the startup issue from happening to the MICRF219A series ASK receiver. However, exact values of the RC network depend on the ramp rate of the supply voltage, and should be determined on a case-by-case basis.

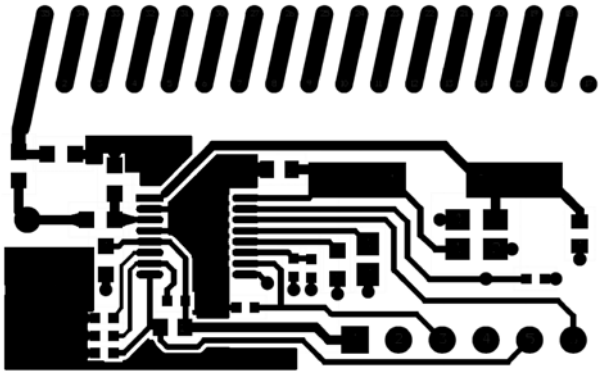
PCB Considerations and Layout

The MICRF219A evaluation board is a good starting point for prototyping of most applications. The Gerber files are downloadable from the Micrel website and contain the remaining layers needed to fabricate this board. When copying or making one's own boards, make the traces as short as possible. Long traces alter the matching network and the values suggested are no longer valid. Suggested matching values may vary due to PCB variations. A PCB trace 100 mils (2.5mm) long has about 1.1nH inductance. Optimization should always be done with range tests. Make sure the individual ground connection has a dedicated via rather then sharing a few of ground points by a single via. Sharing ground via will increase the ground path inductance. Ground plane should be solid and with no sudden interruptions. Avoid using ground plane on top layer next to the matching elements. It normally adds additional stray capacitance which changes the matching. Do not use Phenolic materials as they are conductive above 200MHz. Typically, FR4 or better materials are recommended. The RF path should be as straight as possible to avoid loops and unnecessary turns. Separate ground and V_{DD} lines from other digital or switching power circuits (such microcontroller, etc). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid unnecessary wide traces which would add more distribution capacitance (between top trace to bottom GND plane) and alter the RF parameters.

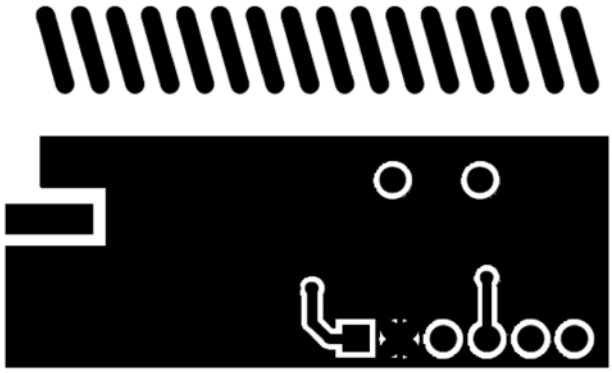
PCB Recommended Layout Considerations



MICRF219A Evaluation Board Assembly

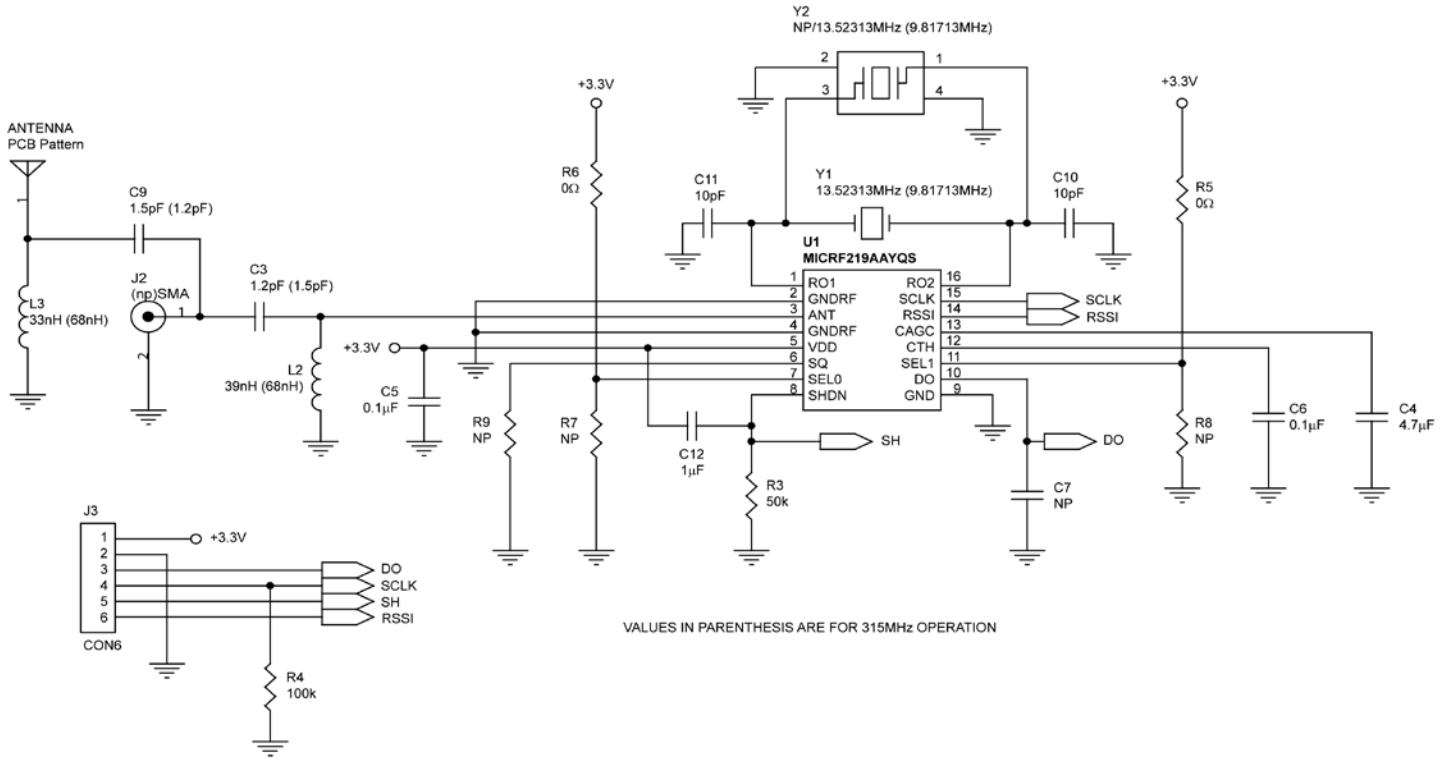


MICRF219A Evaluation Board Top Layer



MICRF219A Evaluation Board Bottom Layer

MICRF219A Evaluation Board Schematic



Bill of Materials – MICRF219A Evaluation Board: 433.92MHz

Item	Part Number	Manufacturer	Description	Qty.
C3	GQM1885C2A1R2C	Murata[1]	1.2pF ±0.25pF, 0603 capacitor	1
C4	GRM219R60J475K	Murata[1]	4.7µF ±10%, 0805 capacitor	1
C5, C6	GRM188R71E104K	Murata[1]	0.1µF ±10%, 0603 capacitor	2
C7			NP	0
C9	GQM1885C2A1R5C	Murata[1]	1.5pF ±0.25pF, 0603 capacitor	1
C10, C11	GRM1885C1H100J	Murata[1]	10pF ±5%, 0603 capacitor	2
C12	GRM188R61A105K	Murata[1]	1µF ±10%, 0603 capacitor	1
J2			NP, SMA, Edge Conn.	0
J3	571-41031480	Mouser[2]	AMPMODU Breakaway Headers 40 P(6pos) R/A HEADER GOLD	1
L2	LQG18HN39NJ00	Murata[1]	39nH ±5%, 0603 multi layer ceramic inductor	1
L3	LQG18HN33NJ00	Murata[1]	33nH ±5%, 0603 multi layer ceramic inductor	1
R3	CRCW040250KFKEA	Vishay[3]	50kΩ ±5%, 0402 resistor	1
R4	CRCW0402100KFKEA	Vishay[3]	100kΩ ±5%, 0402 resistor	1
R5, R6	CRCW04020000Z	Vishay[3]	0Ω ±5%,, 0402 resistor	2
R7, R8, R9			NP	0
Y1	ABLS-13.52313MHz-10J4Y	Abracon[4]	13.52313MHz, HC49/US	1
Y2	DSX321GK-13.52313MHz	KDS[5]	NP, (13.52313MHz, –40°C to +105°C), DSX321GK	0
U1	**MICRF219AAYQS**	**Micrel, Inc.[6]**	**300MHz to 450MHz ASK/OOK Receiver with Auto-Poll, and RSSI**	**1**

Notes:

1. Murata: www.murata.com.
2. Mouser: www.mouser.com.
3. Vishay Tel: www.vishay.com.
4. Abracon: www.abracon.com.
5. KDS: www.kds.info/index_en.htm.
6. **Micrel, Inc.:** www.micrel.com.

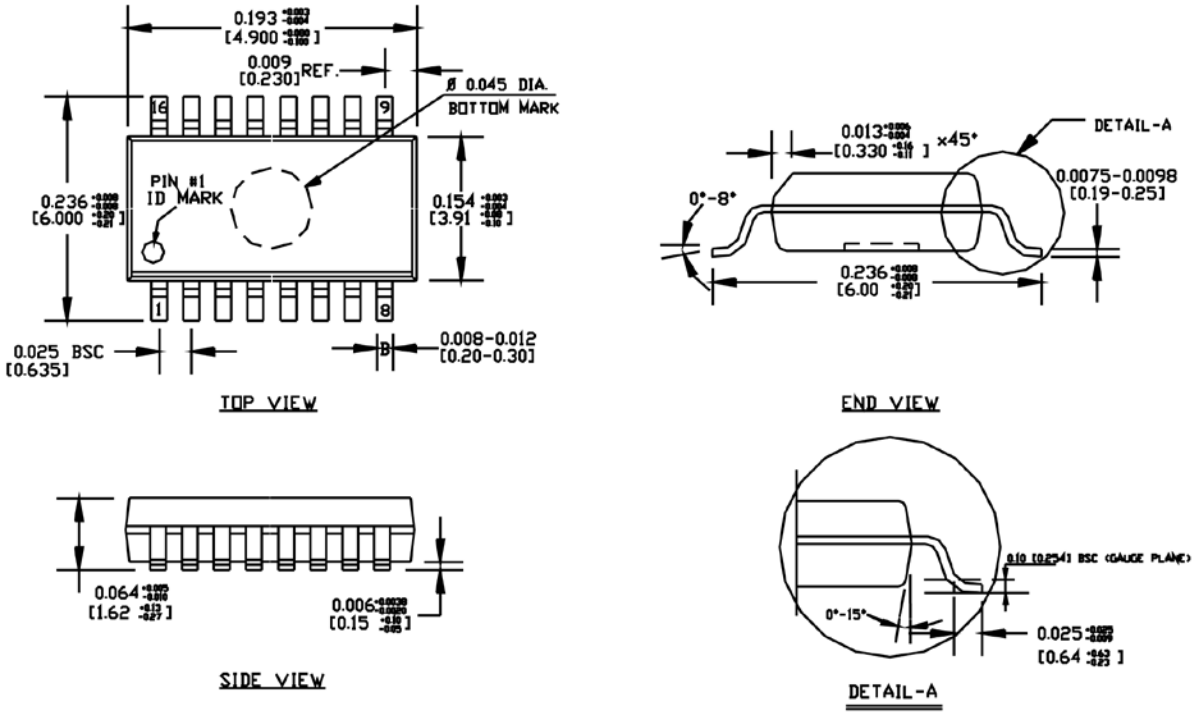
Bill of Materials – MICRF219A Evaluation Board: 315MHz

Item	Part Number	Manufacturer	Description	Qty.
C3	GQM1885C2A1R5C	Murata[7]	1.5pF ±0.25pF, 0603 Capacitor	1
C4	GRM21BR60J475K	Murata[7]	4.7µF ±10%, 0805 Capacitor	1
C5, C6	GRM188R71E104K	Murata[7]	0.1µF ±10%, 0603 Capacitor	2
C7			NP	0
C9	GQM1885C2A1R2C	Murata[7]	1.2pF ±0.25pF, 0603 Capacitor	1
C10, C11	GRM1885C1H100J	Murata[7]	10pF ±5%, 0603 Capacitor	2
C12	GRM188R61A105K	Murata[7]	1µF ±10%, 0603 Capacitor	1
J2			NP, SMA, Edge Conn.	0
J3	571-41031480	Mouser[8]	AMPMODU Breakaway Headers 40 P(6pos) R/A HEADER GOLD	1
L2, L3	LQG18HN68NJ00	Murata[7]	68nH ±5%, 0603 Multi Layer Ceramic Inductor	2
R3	CRCW040250KFKEA	Vishay[9]	50kΩ ±5%, 0402 Resistor	1
R4	CRCW0402100KFKEA	Vishay[9]	100kΩ ±5%, 0402 Resistor	1
R5, R6	CRCW04020000Z	Vishay[9]	0Ω ±5%,, 0402 Resistor	2
R7, R8, R9			NP	0
Y1	ABLS-9.81713MHz-10J4Y	Abracon[10]	9.81713MHz, HC49/US	1
Y2	DSX321GK-9.81713MHz	KDS[11]	NP, (9.81713MHz, –40°C to +105°C), DSX321GK	0
U1	**MICRF219AAYQS**	**Micrel, Inc.[12]**	**300MHz to 450MHz ASK/OOK Receiver with Auto-Poll, and RSSI**	**1**

Notes:

7. Murata: www.murata.com.
8. Mouser: www.mouser.com.
9. Vishay Tel: www.vishay.com.
10. Abracon: www.abracon.com.
11. KDS: www.kds.info/index_en.htm.
12. **Micrel, Inc.:** www.micrel.com.

Package Information and Recommended Land Pattern[13]



NOTE:
1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0076 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

QSOP16 Package (AQS16)

Note:
13. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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Micrel, Inc. is a leading global manufacturer of IC solutions for the worldwide high performance linear and power, LAN, and timing & communications markets. The Company's products include advanced mixed-signal, analog & power semiconductors; high-performance communication, clock management, MEMs-based clock oscillators & crystal-less clock generators, Ethernet switches, and physical layer transceiver ICs. Company customers include leading manufacturers of enterprise, consumer, industrial, mobile, telecommunications, automotive, and computer products. Corporation headquarters and state-of-the-art wafer fabrication facilities are located in San Jose, CA, with regional sales and support offices and advanced technology design centers situated throughout the Americas, Europe, and Asia. Additionally, the Company maintains an extensive network of distributors and reps worldwide.

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