Absolute Maximum Ratings(Note 1)

 $\begin{array}{lll} \mbox{Voltage at Any Pin} & -0.3\mbox{V to V}_{\mbox{CC}} + 0.3\mbox{V} \\ \mbox{Operating Temperature Range} & -55\mbox{^{\circ}C to +125\mbox{^{\circ}C}} \\ \mbox{Storage Temperature Range} & -65\mbox{^{\circ}C to +150\mbox{^{\circ}C}} \end{array}$

Power Dissipation

 $\begin{array}{cc} \text{Dual-In-Line} & 700 \text{ mW} \\ \text{Small Outline} & 500 \text{ mW} \\ \text{Operating V}_{\text{CC}} \text{ Range} & 4.5 \text{V to } 15 \text{V} \\ \end{array}$

Absolute Maximum V_{CC} 18V

 $R_{EXT} \ge 80 V_{CC} (\Omega)$

Lead Temperature

(Soldering, 10 seconds)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions

for actual device operation.

DC Electrical Characteristics

Max/min limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS to 0	CMOS	•				
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	3.5			V
		$V_{CC} = 10V$	8.0			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
		$V_{CC} = 10V$			2.0	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_{O} = -10 \mu A$	4.5			V
		$V_{CC} = 10V$, $I_{O} = -10 \mu A$	9.0			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5V, I_{O} = +10 \mu A$			0.5	V
. ,		$V_{CC} = 10V$, $I_{O} = +10 \mu A$			1	
N(1)	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ
N(0)	Logical "0" Input Current	V _{CC} = 15V, V _{IN} = 0V	-1.0	-0.005		μΑ
I _{cc}	Supply Current (Standby)	V _{CC} = 15V, R _{EXT} = ∞,		0.05	300	μΑ
		Q1, Q2 = Logic "0" (Note 2)				
lcc	Supply Current	V _{CC} = 15V, Q1 = Logic "1",		15		mA
	(During Output Pulse)	Q2 = Logic "0" (Figure 4)				
		V _{CC} = 5V, Q1 = Logic "1",		2		mA
		Q2 = Logic "0" (Figure 4)				
	Leakage Current at R/C _{EXT} Pin	V _{CC} = 15V, V _{CEXT} = 5V		0.01	3.0	μА
MOS/LP	TTL Interface	•		L		
¹ IN(1)	Logical "1" Input Voltage	V _{CC} = 4.75V	V _{CC} - 1.5			V
IN(0)	Logical "0" Input Voltage	V _{CC} = 4.75V			8.0	V
/ _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_{O} = -360 \mu A$	2.4			V
OUT(0)	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{O} = 360 \mu A$			0.4	V
Output Dri	ve (See Family Characteristics Data	Sheet) (Short Circuit Current)		L		
I _{SOURCE}	Output Source Current	V _{CC} = 5V	-1.75			mA
	(P-Channel)	T _A = 25°C, V _{OUT} = 0V				
I _{SOURCE}	Output Source Current	V _{CC} = 10V	-8			mA
	(P-Channel)	T _A = 25°C, V _{OUT} = 0V				
SINK	Output Sink Current	V _{CC} = 5V	1.75			mA
	(N-Channel)	$T_A = 25^{\circ}C$, $V_{OUT} = V_{CC}$				
I _{SINK}	Output Sink Current	V _{CC} = 10V	8			mA
	(N-Channel)	T _A = 25°C, V _{OUT} = V _{CC}				

260°C

Note 2: In Standby (Q = Logic "0") the power dissipated equals the leakage current plus V_{CC}/R_{EXT} .

AC Electrical Characteristics (Note 3) $T_A = 25^{\circ}C$, $C_1 = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd A, B}	Propagation Delay from Trigger	V _{CC} = 5V		250	500	ns
	Input (A, B) to Output Q, Q	V _{CC} = 10V		120	250	
t _{pd CL}	Propagation Delay from Clear	V _{CC} = 5V		250	500	ns
	Input (CL) to Output Q, Q	V _{CC} = 10V		120	250	
t _S	Time Prior to Trigger Input (A, B)	V _{CC} = 5V	150	50		ns
	that Clear must be Set	V _{CC} = 10V	60	20		
t _{W(A, B)}	Trigger Input (A, B) Pulse Width	V _{CC} = 5V	150	50		T
		V _{CC} = 10V	70	30		ns
t _{W(CL)}	Clear Input (CL) Pulse Width	V _{CC} = 5V	150	50		
		V _{CC} = 10V	70	30		ns
t _{W(OUT)}	Q or Q Output Pulse Width	V _{CC} = 5V, R _{EXT} = 10k,		900		ns
	· ·	C _{EXT} = 0 pF				
		$V_{CC} = 10V, R_{EXT} = 10k,$		350		ns
		C _{EXT} = 0 pF				
		V _{CC} = 15V, R _{EXT} = 10k,		320		ns
		C _{EXT} = 0 pF				
		$V_{CC} = 5V, R_{EXT} = 10k,$	9.0	10.6	12.2	μs
		C _{EXT} = 1000 pF (Figure 1)				
		V _{CC} = 10V, R _{EXT} = 10k,	9.0	10	11	μs
		C _{EXT} = 1000 pF (Figure 1)				
		V _{CC} = 15V, R _{EXT} = 10k,	8.9	9.8	10.8	μs
		C _{EXT} = 1000 pF (Figure 1)				•
		V _{CC} = 5V, R _{EXT} = 10k,	900	1020	1200	μs
		$C_{EXT} = 0.1 \mu\text{F} \text{ (Figure 3)}$				
		V _{CC} = 10V, R _{EXT} = 10k,	900	1000	1100	μs
		$C_{EXT} = 0.1 \mu F$ (Figure 3)				
		V _{CC} = 15V, R _{EXT} = 10k,	900	990	1100	μs
		C _{EXT} = 0.1 μF (Figure 3)				
R _{ON}	ON Resistance of Transistor	V _{CC} = 5V (Note 4)		50	150	
	between R/C EXT to CEXT	V _{CC} = 10V (Note 4)		25	65	Ω
		V _{CC} = 15V (Note 4)		16.7	45	
	Output Duty Cycle	R = 10k, C = 1000 pF			90	0/
		$R = 10k, C = 0.1 \mu F$			90	%
		(Note 5)				
C _{IN}	Input Capacitance	R/C _{EXT} Input (Note 6)		15	25	
		Any Other Input (Note 6)		5		pF

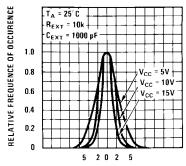
Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: See AN-138 for detailed explanation $\ensuremath{\text{R}_{\text{ON}}}.$

Note 5: Maximum output duty cycle = $R_{EXT}/R_{EXT} + 1000$.

Note 6: Capacitance is guaranteed by periodic testing.

Typical Performance Characteristics



OUTPUT PULSE WIDTH (Tw., %)

0% Point pulse width:

At $V_{CC} = 5V$, $T_W = 10.6 \,\mu s$

At $V_{CC} = 10 \text{V}, T_W = 10~\mu\text{s}$

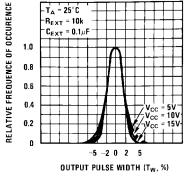
At $V_{CC} = 15 V$, $T_W = 9.8~\mu s$

Percentage of units within +4%:

At $V_{CC} = 5V,90\%$ of units

At $V_{CC} = 10V,95\%$ of units At $V_{CC} = 15V,98\%$ of units

FIGURE 1. Typical Distribution of Units for Output



0% Point pulse width:

At $V_{CC} = 5V$, $T_W = 1020 \ \mu s$

At $V_{CC}=10 V, T_W=1000~\mu s$

At V_{CC} = 15V, T_W = 982 μs

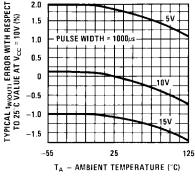
Percentage of units within +4%:

At $V_{CC} = 5V,95\%$ of units

At $V_{CC} = 10V,97\%$ of units

At V_{CC} = 15V,98% of units

FIGURE 3. Typical Distribution of Units for Output Pulse Width



Pulse Width

FIGURE 2. Typical Variation in Output Pulse Width vs
Temperature

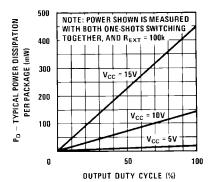
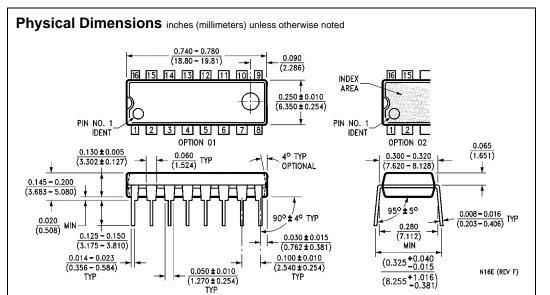


FIGURE 4. Typical Power Dissipation per Package



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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