

**Table 3. ESD Protection Characteristics**

| Test Methodology                      | Class         |
|---------------------------------------|---------------|
| Human Body Model (per JESD22-A114)    | 1B (Minimum)  |
| Machine Model (per EIA/JESD22-A115)   | A (Minimum)   |
| Charge Device Model (per JESD22-C101) | III (Minimum) |

**Table 4. Moisture Sensitivity Level**

| Test Methodology                     | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3      | 260                      | °C   |

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

**Off Characteristics**

|   |           |   |   |    |                 |
|---|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current<br>( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) | $I_{DSS}$ | — | — | 10 | $\mu\text{Adc}$ |
| Zero Gate Voltage Drain Leakage Current<br>( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) | $I_{DSS}$ | — | — | 1  | $\mu\text{Adc}$ |
| Gate-Source Leakage Current<br>( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )              | $I_{GSS}$ | — | — | 1  | $\mu\text{Adc}$ |

**On Characteristics (DC)**

|   |              |     |     |     |     |
|---|--------------|-----|-----|-----|-----|
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 200\ \mu\text{Adc}$ )                           | $V_{GS(th)}$ | 1.5 | 2.2 | 2.5 | Vdc |
| Gate Quiescent Voltage<br>( $V_{DD} = 28\text{ Vdc}$ , $I_D = 610\text{ mAdc}$ , Measured in Functional Test) | $V_{GS(Q)}$  | 2   | 2.8 | 4   | Vdc |
| Drain-Source On-Voltage<br>( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ )                              | $V_{DS(on)}$ | —   | 0.3 | —   | Vdc |

**Dynamic Characteristics <sup>(1)</sup>**

|   |           |   |     |   |    |
|---|-----------|---|-----|---|----|
| Reverse Transfer Capacitance<br>( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ ) | $C_{rss}$ | — | 1.5 | — | pF |
|---|-----------|---|-----|---|----|

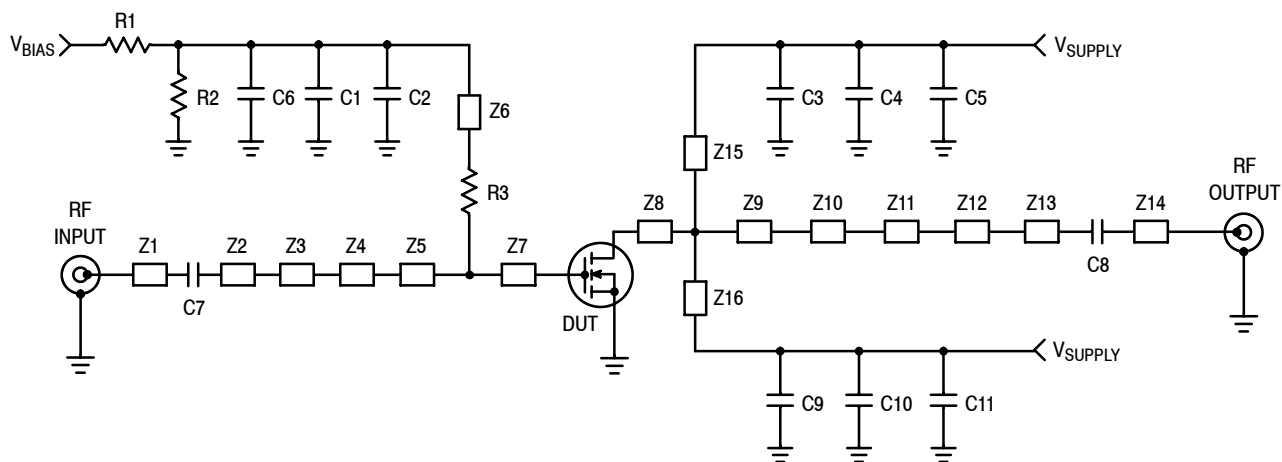
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 610\text{ mA}$ ,  $P_{out} = 14\text{ W Avg.}$ ,  $f_1 = 2115.5\text{ MHz}$ ,  $f_2 = 2122.5\text{ MHz}$ , 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset. IM3 measured in 3.84 MHz Bandwidth @  $\pm 10\text{ MHz}$  Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

|                              |          |      |      |      |     |
|------------------------------|----------|------|------|------|-----|
| Power Gain                   | $G_{ps}$ | 13.5 | 15.5 | 16.5 | dB  |
| Drain Efficiency             | $\eta_D$ | 24.5 | 26   | —    | %   |
| Intermodulation Distortion   | IM3      | —    | -37  | -35  | dBc |
| Adjacent Channel Power Ratio | ACPR     | —    | -40  | -38  | dBc |
| Input Return Loss            | IRL      | —    | -14  | -10  | dB  |

1. Part is internally matched both on input and output.

LIFETIME BUY

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|    |                            |     |  |
|----|----------------------------|-----|--|
| Z1 | 0.250" x 0.080" Microstrip | Z10 | 0.270" x 0.300" Microstrip                                 |
| Z2 | 0.860" x 0.080" Microstrip | Z11 | 0.230" x 0.080" Microstrip                                 |
| Z3 | 0.300" x 0.405" Microstrip | Z12 | 0.310" x 0.300" Microstrip                                 |
| Z4 | 0.350" x 0.080" Microstrip | Z13 | 0.830" x 0.080" Microstrip                                 |
| Z5 | 0.350" x 0.755" Microstrip | Z14 | 0.200" x 0.080" Microstrip                                 |
| Z6 | 0.680" x 0.080" Microstrip | Z15 | 1.000" x 0.080" Microstrip                                 |
| Z7 | 0.115" x 0.755" Microstrip | Z16 | 1.100" x 0.070" Microstrip                                 |
| Z8 | 0.115" x 1.000" Microstrip | PCB | Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$ |
| Z9 | 0.240" x 1.000" Microstrip |     |  |

Figure 1. MRF6S21060NR1(NBR1) Test Circuit Schematic

Table 6. MRF6S21060NR1(NBR1) Test Circuit Component Designations and Values

| Part                 | Description                         | Part Number        | Manufacturer |
|----------------------|-------------------------------------|--------------------|--------------|
| C1                   | 100 nF Chip Capacitor               | CDR33BX104AKYS     | Kemet        |
| C2, C7               | 4.7 pF Chip Capacitors              | ATC100B4R7BT500XT  | ATC          |
| C3, C8, C9           | 6.8 pF Chip Capacitors              | ATC100B6R8BT500XT  | ATC          |
| C4, C5, C6, C10, C11 | 10 $\mu$ F, 35 V Chip Capacitors    | GRM55DR61H106KA88L | Murata       |
| R1                   | 1 k $\Omega$ , 1/4 W Chip Resistor  | CRCW12061001FKEA   | Vishay       |
| R2                   | 10 k $\Omega$ , 1/4 W Chip Resistor | CRCW12061002FKEA   | Vishay       |
| R3                   | 10 $\Omega$ , 1/4 W Chip Resistor   | CRCW120610R0FKEA   | Vishay       |

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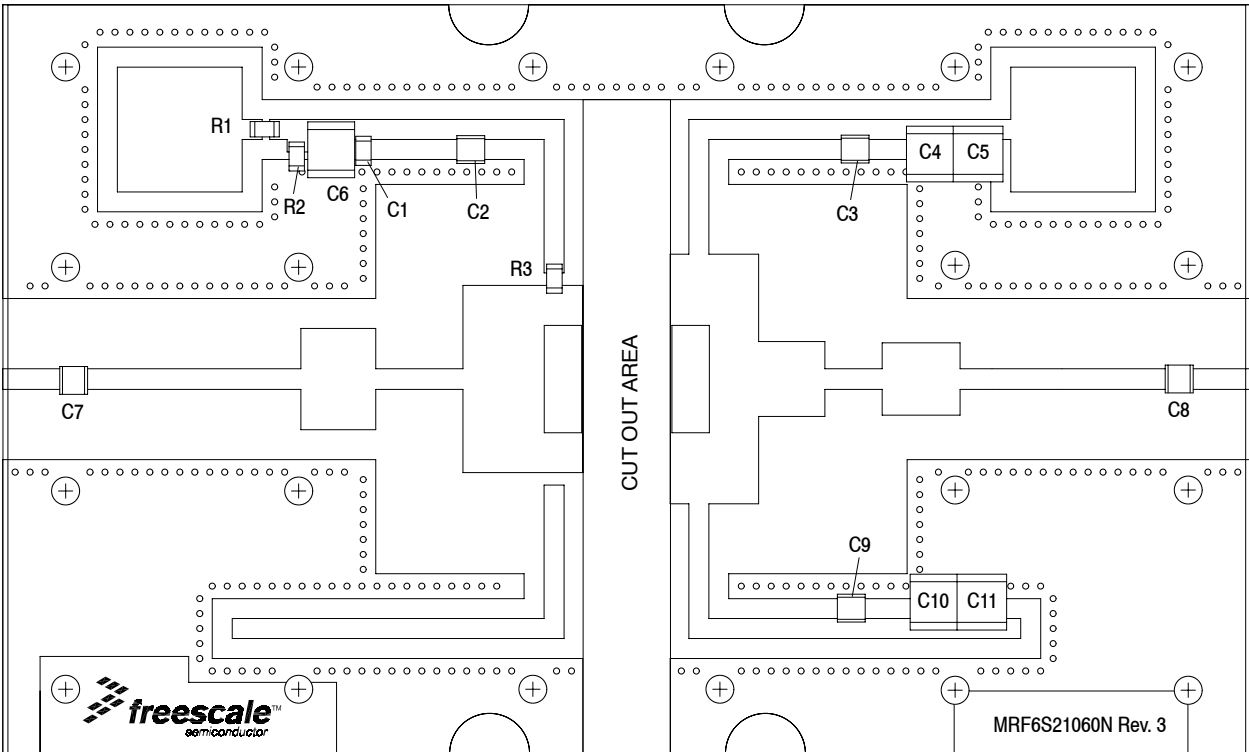


Figure 2. MRF6S21060NR1(NBR1) Test Circuit Component Layout

### TYPICAL CHARACTERISTICS

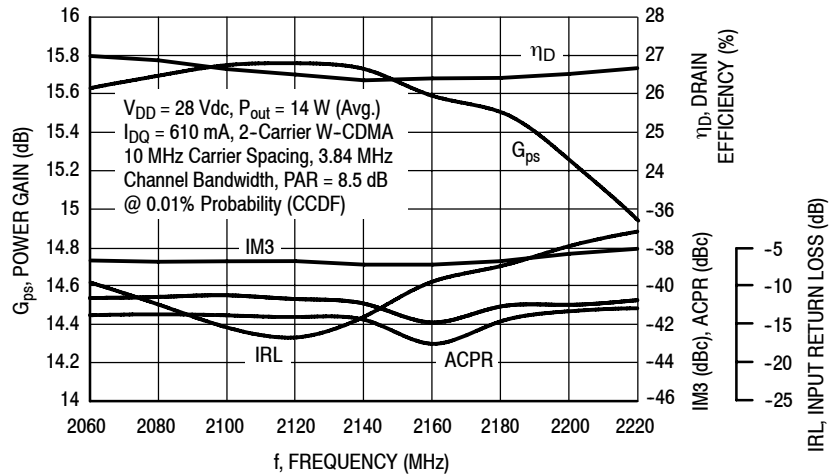


Figure 3. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 14$  Watts Avg.

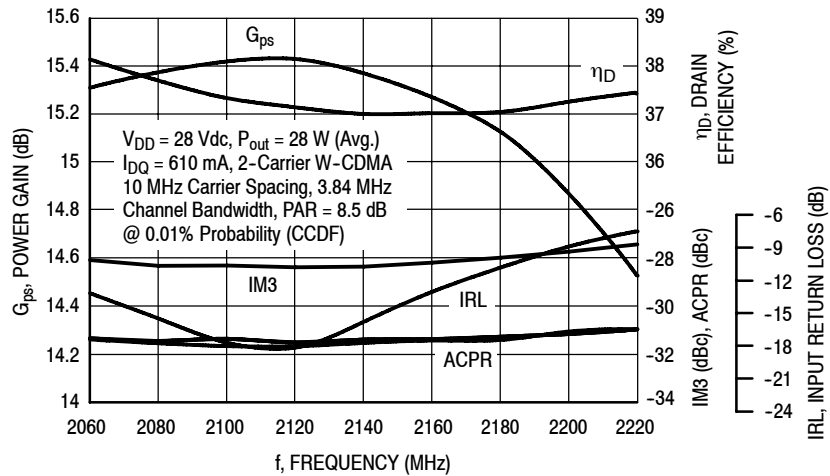


Figure 4. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 28$  Watts Avg.

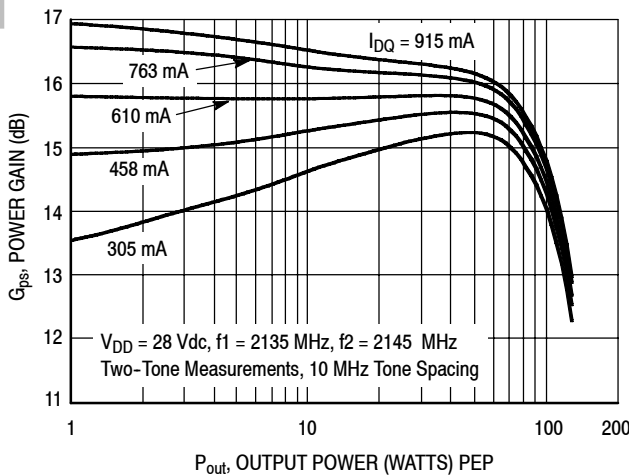


Figure 5. Two-Tone Power Gain versus Output Power

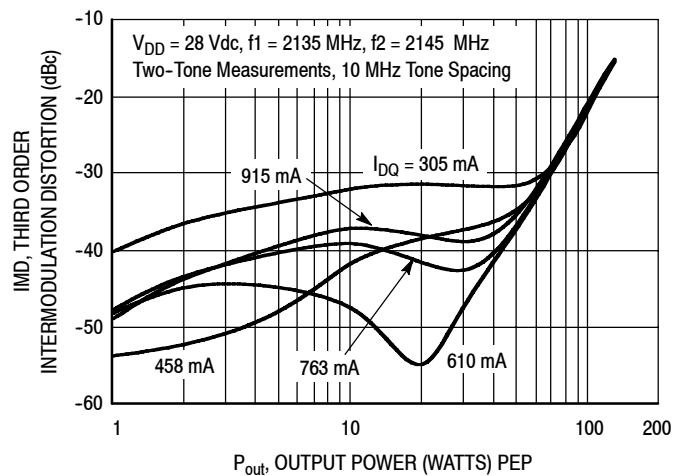
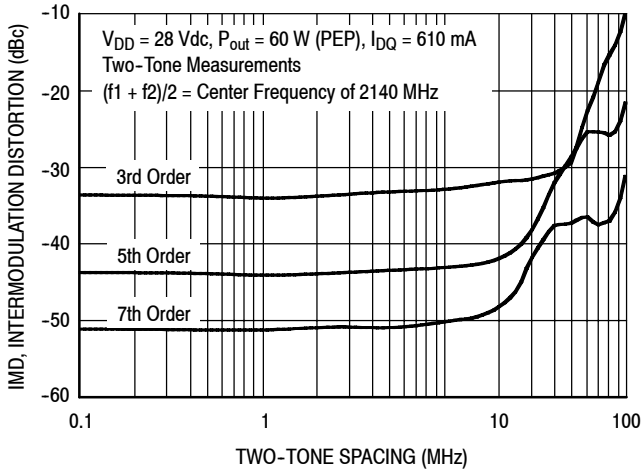
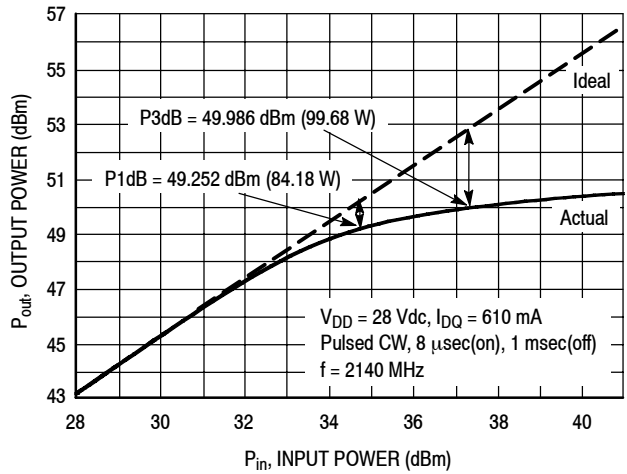


Figure 6. Third Order Intermodulation Distortion versus Output Power

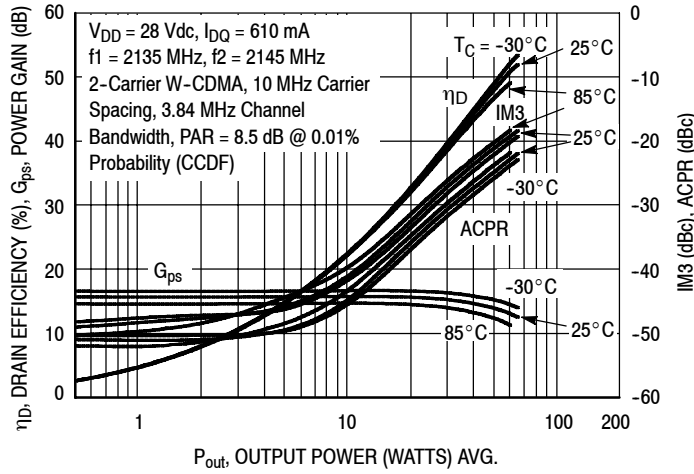
### TYPICAL CHARACTERISTICS



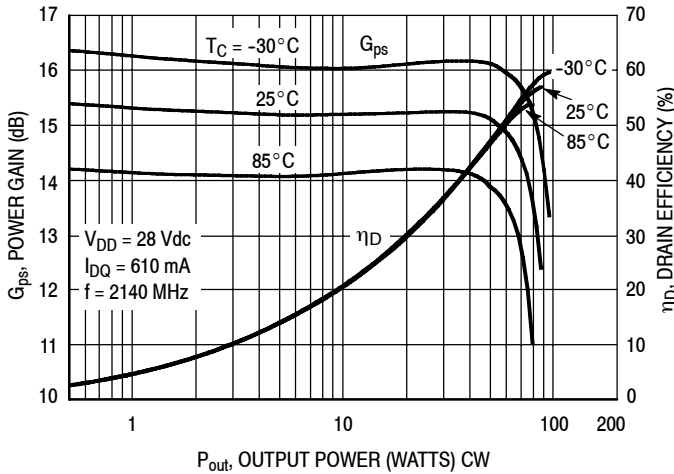
**Figure 7. Intermodulation Distortion Products versus Tone Spacing**



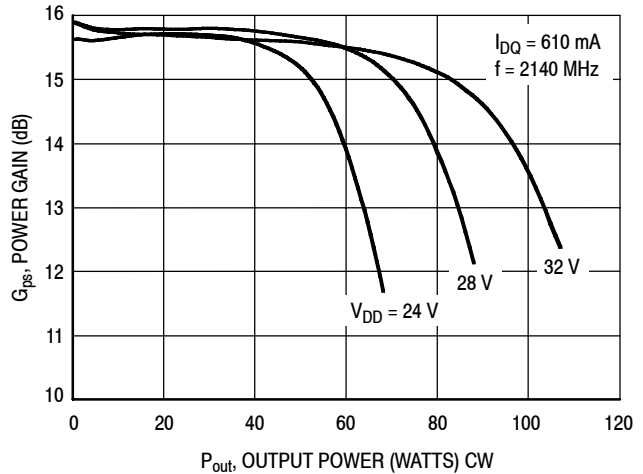
**Figure 8. Pulsed CW Output Power versus Input Power**



**Figure 9. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**



**Figure 10. Power Gain and Drain Efficiency versus CW Output Power**

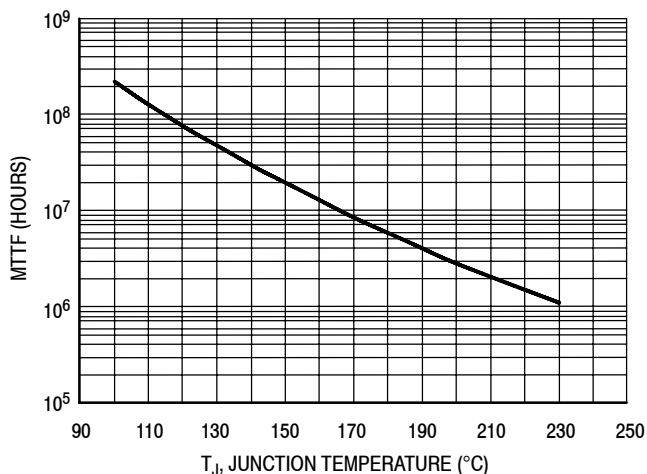


**Figure 11. Power Gain versus Output Power**

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### TYPICAL CHARACTERISTICS



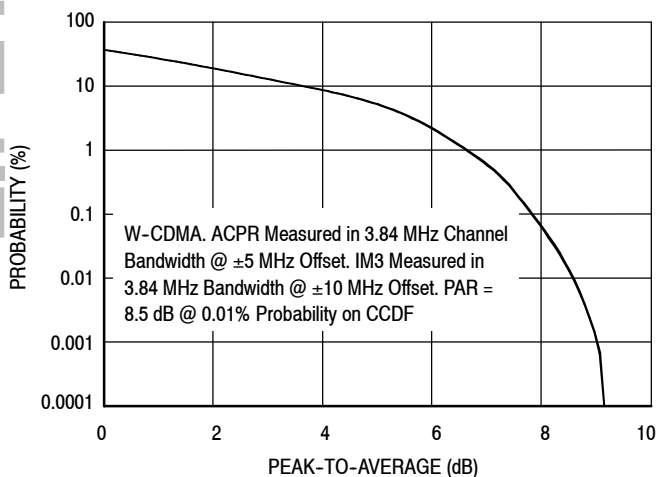
This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 14$  W Avg., and  $\eta_D = 26\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

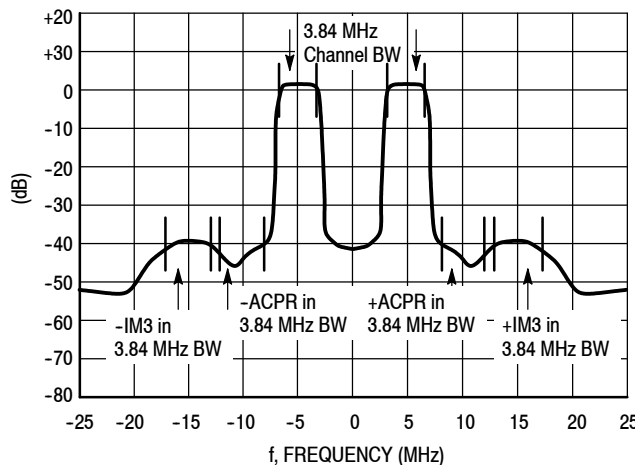
**Figure 12. MTTF Factor versus Junction Temperature**

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### W-CDMA TEST SIGNAL

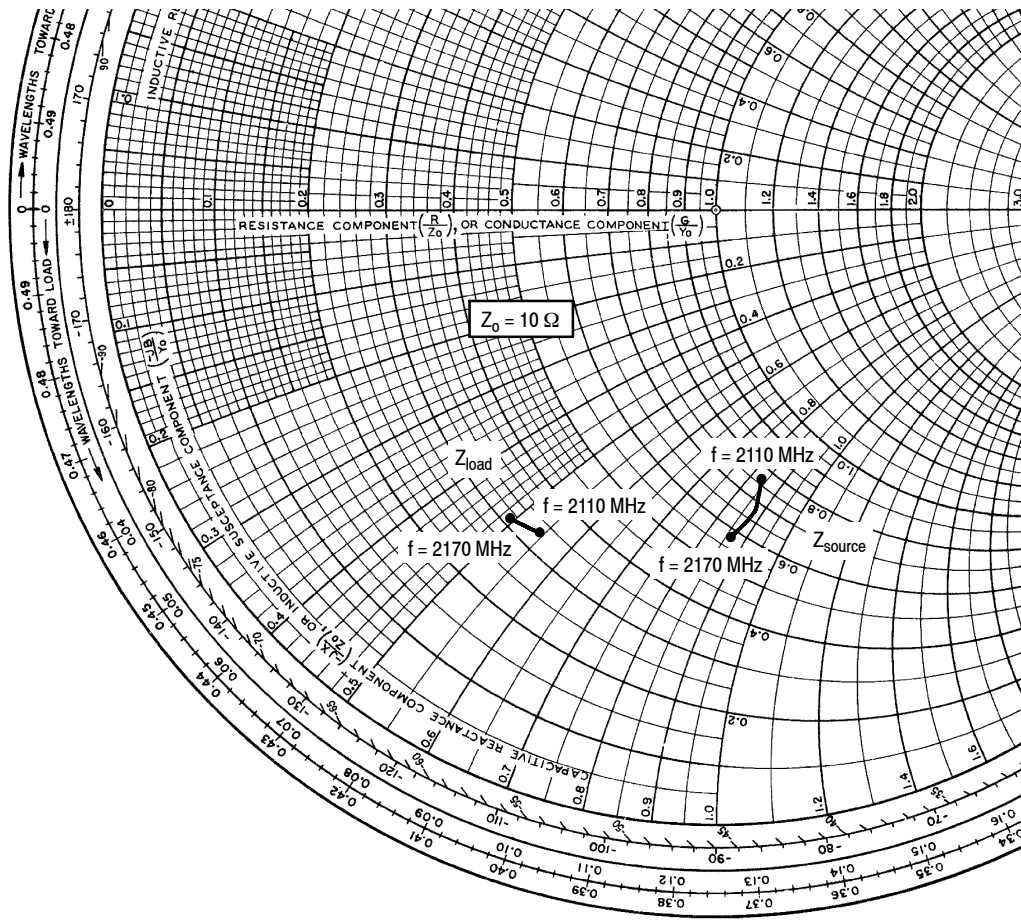


**Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal**



**Figure 14. 2-Carrier W-CDMA Spectrum**

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$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 610 \text{ mA}$ ,  $P_{out} = 14 \text{ W Avg.}$

| f<br>MHz | $Z_{source}$<br>$\Omega$ | $Z_{load}$<br>$\Omega$ |
|----------|--------------------------|------------------------|
| 2110     | $7.59 - j8.39$           | $3.31 - j5.35$         |
| 2140     | $6.71 - j8.83$           | $3.17 - j5.16$         |
| 2170     | $5.84 - j8.62$           | $3.06 - j4.92$         |

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

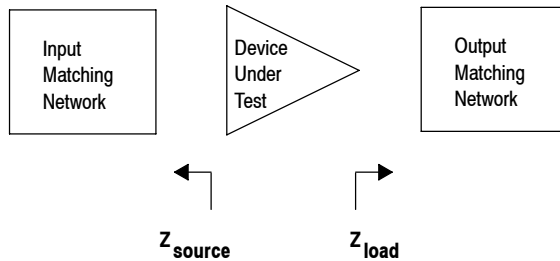
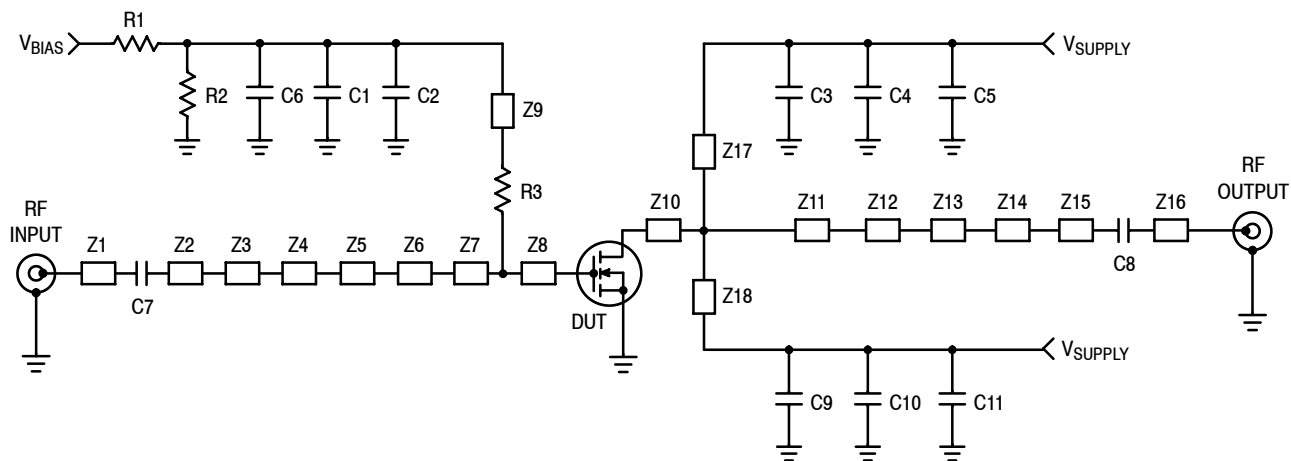


Figure 15. Series Equivalent Source and Load Impedance

### TD-SCDMA CHARACTERIZATION



|     |                            |
|-----|----------------------------|
| Z1  | 0.250" x 0.080" Microstrip |
| Z2  | 0.129" x 0.080" Microstrip |
| Z3* | 0.565" x 0.258" Microstrip |
| Z4  | 0.160" x 0.080" Microstrip |
| Z5* | 0.300" x 0.455" Microstrip |
| Z6  | 0.350" x 0.080" Microstrip |
| Z7  | 0.350" x 0.755" Microstrip |
| Z8  | 0.115" x 0.755" Microstrip |
| Z9  | 0.680" x 0.080" Microstrip |
| Z10 | 0.115" x 1.000" Microstrip |

|      |  |
|------|--|
| Z11  | 0.240" x 1.000" Microstrip                                 |
| Z12* | 0.270" x 0.360" Microstrip                                 |
| Z13  | 0.230" x 0.080" Microstrip                                 |
| Z14* | 0.588" x 0.290" Microstrip                                 |
| Z15  | 0.595" x 0.080" Microstrip                                 |
| Z16  | 0.200" x 0.080" Microstrip                                 |
| Z17  | 0.935" x 0.080" Microstrip                                 |
| Z18  | 0.955" x 0.080" Microstrip                                 |
| PCB  | Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$ |

\* Copper foil tape soldered onto PCB

Figure 16. MRF6S21060NR1(NBR1) Test Circuit Schematic — TD-SCDMA

Table 7. MRF6S21060NR1(NBR1) Test Circuit Component Designations and Values — TD-SCDMA

| Part                 | Description                         | Part Number        | Manufacturer |
|----------------------|-------------------------------------|--------------------|--------------|
| C1                   | 100 nF Chip Capacitor               | CDR33BX104AKYS     | Kemet        |
| C2, C7               | 4.7 pF Chip Capacitors              | ATC100B4R7BT500XT  | ATC          |
| C3, C8, C9           | 6.8 pF Chip Capacitors              | ATC100B6R8BT500XT  | ATC          |
| C4, C5, C6, C10, C11 | 10 $\mu$ F, 35 V Chip Capacitors    | GRM55DR61H106KA88L | Murata       |
| R1                   | 1 k $\Omega$ , 1/4 W Chip Resistor  | CRCW12061001FKEA   | Vishay       |
| R2                   | 10 k $\Omega$ , 1/4 W Chip Resistor | CRCW12061002FKEA   | Vishay       |
| R3                   | 10 $\Omega$ , 1/4 W Chip Resistor   | CRCW120610R0FKEA   | Vishay       |

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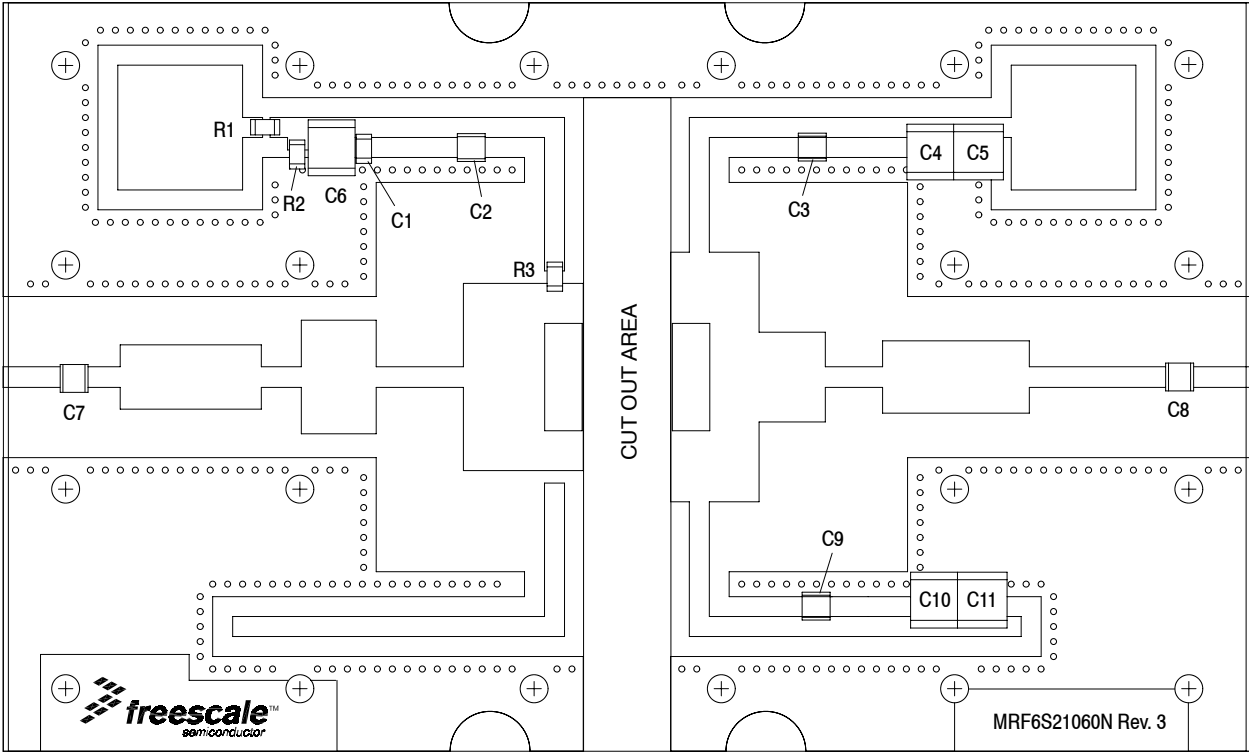
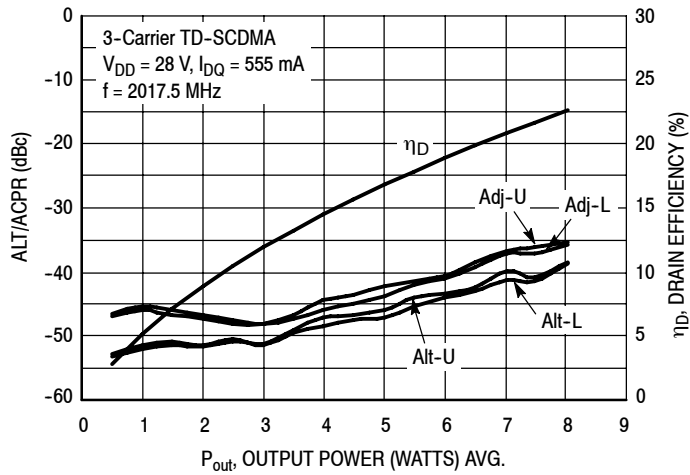
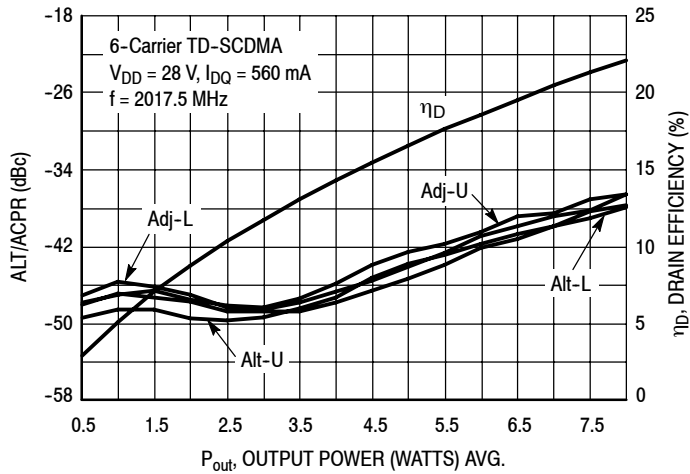


Figure 17. MRF6S21060NR1(NBR1) Test Circuit Component Layout — TD-SCDMA

### TYPICAL CHARACTERISTICS

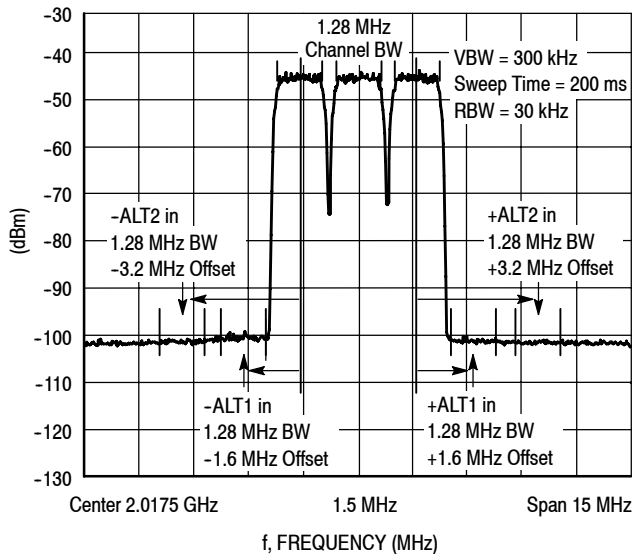


**Figure 18. 3-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power**

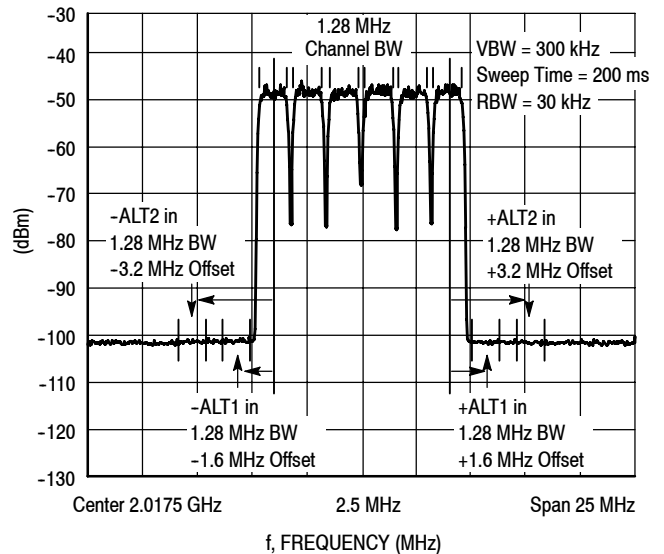


**Figure 19. 6-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power**

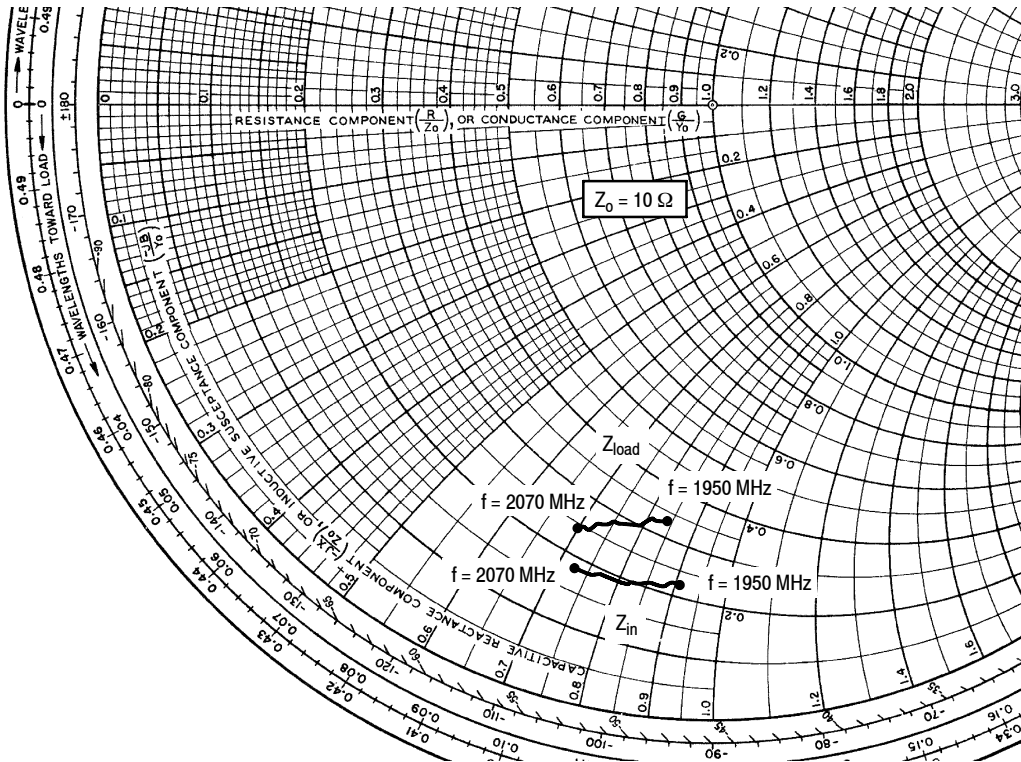
### TD-SCDMA TEST SIGNAL



**Figure 20. 3-Carrier TD-SCDMA Spectrum**



**Figure 21. 6-Carrier TD-SCDMA Spectrum**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 560 \text{ mA}$

| f MHz | $Z_{in}$ $\Omega$ | $Z_{load}$ $\Omega$ |
|-------|-------------------|---------------------|
| 1950  | 2.227 - j9.127    | 3.341 - j8.372      |
| 1960  | 2.168 - j8.942    | 3.239 - j8.218      |
| 1970  | 2.124 - j8.757    | 3.168 - j8.084      |
| 1980  | 2.073 - j8.606    | 3.083 - j7.966      |
| 1990  | 2.031 - j8.447    | 3.009 - j7.865      |
| 2000  | 1.987 - j8.306    | 2.929 - j7.743      |
| 2010  | 1.940 - j8.155    | 2.845 - j7.639      |
| 2020  | 1.911 - j8.000    | 2.775 - j7.529      |
| 2030  | 1.891 - j7.835    | 2.696 - j7.410      |
| 2040  | 1.856 - j7.711    | 2.615 - j7.309      |
| 2050  | 1.831 - j7.589    | 2.549 - j7.207      |
| 2060  | 1.808 - j7.461    | 2.479 - j7.086      |
| 2070  | 1.782 - j7.325    | 2.422 - j6.983      |

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

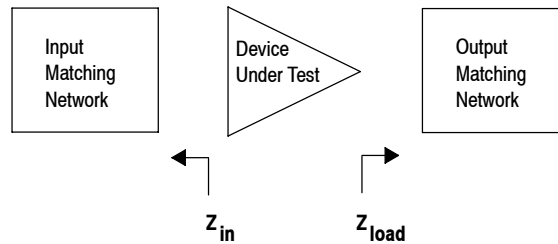
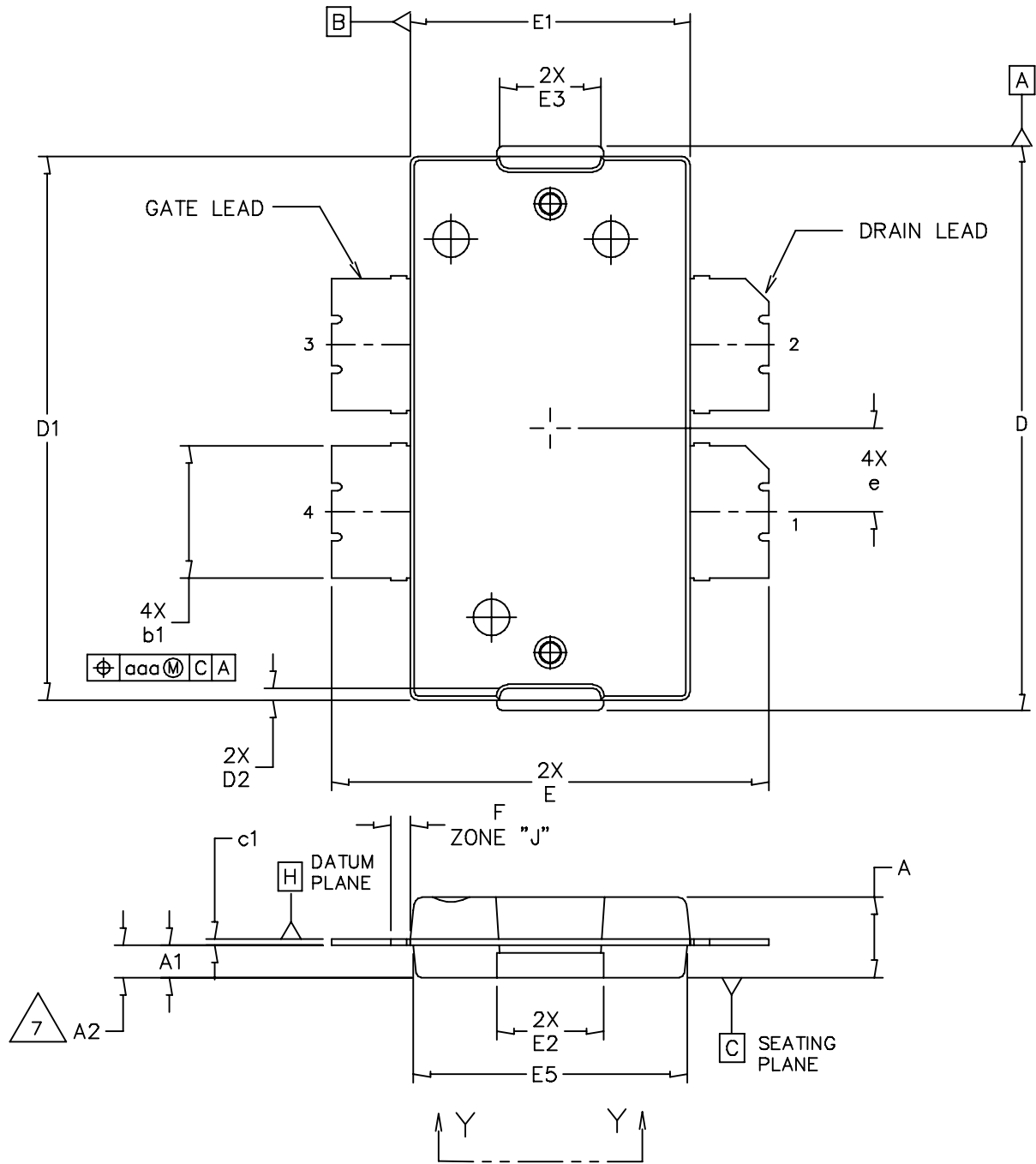
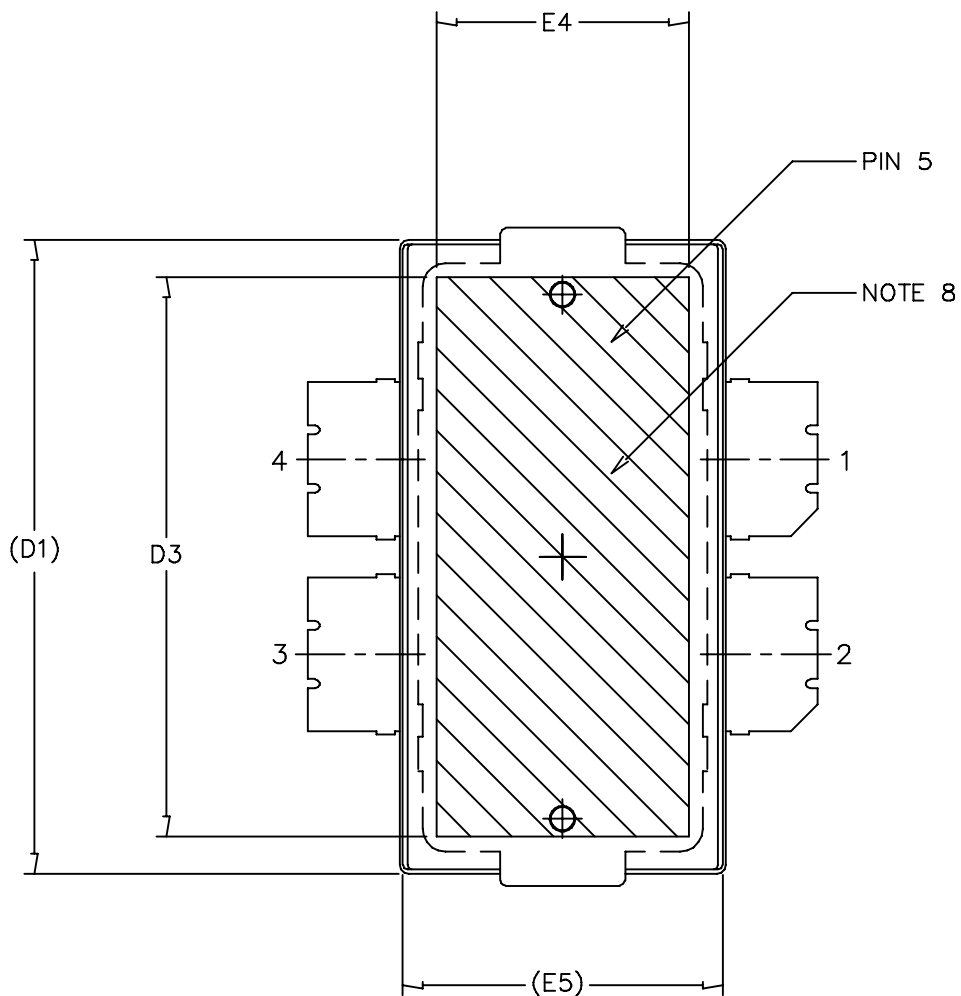


Figure 22. Series Equivalent Input and Load Impedance — TD-SCDMA

**PACKAGE DIMENSIONS**



|   |  |                    |                          |                            |             |
|---|--|--------------------|--------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. |  | MECHANICAL OUTLINE |                          | PRINT VERSION NOT TO SCALE |             |
| TITLE:<br>TO-270<br>4 LEAD, WIDE BODY                   |  |                    | DOCUMENT NO: 98ASA10577D |                            | REV: D      |
|   |  |                    | CASE NUMBER: 1486-03     |                            | 13 AUG 2007 |
|   |  |                    | STANDARD: NON-JEDEC      |                            |             |



|   |                    |                            |             |
|---|--------------------|----------------------------|-------------|
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| TITLE:<br>TO-270<br>4 LEAD, WIDE BODY                   |                    | DOCUMENT NO: 98ASA10577D   | REV: D      |
|   |                    | CASE NUMBER: 1486-03       | 13 AUG 2007 |
|   |                    | STANDARD: NON-JEDEC        |             |

NOTES:

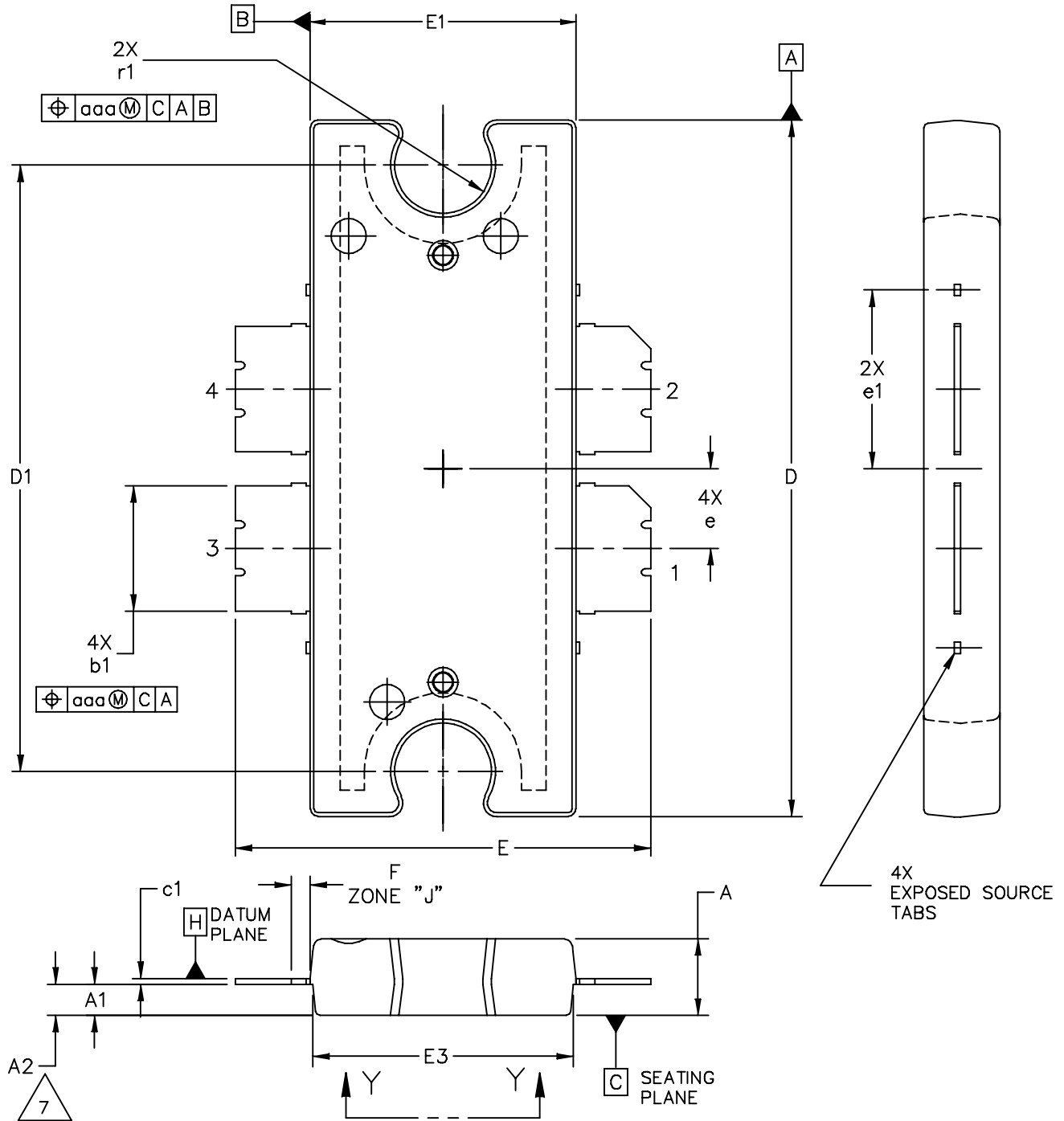
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:

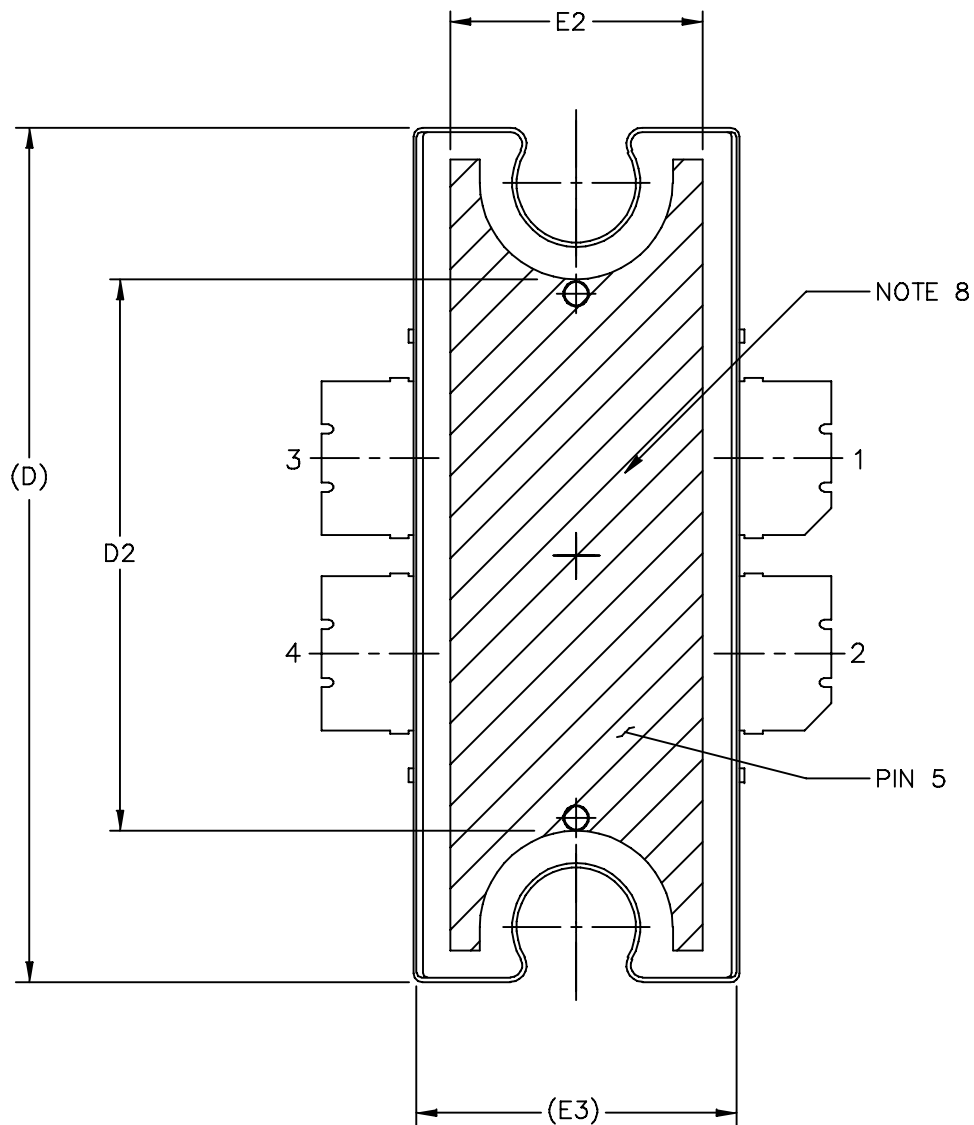
PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

| DIM | INCH |      | MILLIMETER |       | DIM | INCH     |      | MILLIMETER |      |
|-----|------|------|------------|-------|-----|----------|------|------------|------|
|     | MIN  | MAX  | MIN        | MAX   |     | MIN      | MAX  | MIN        | MAX  |
| A   | .100 | .104 | 2.54       | 2.64  | F   | .025 BSC |      | 0.64 BSC   |      |
| A1  | .039 | .043 | 0.99       | 1.09  | b1  | .164     | .170 | 4.17       | 4.32 |
| A2  | .040 | .042 | 1.02       | 1.07  | c1  | .007     | .011 | .18        | .28  |
| D   | .712 | .720 | 18.08      | 18.29 | e   | .106 BSC |      | 2.69 BSC   |      |
| D1  | .688 | .692 | 17.48      | 17.58 | aaa | .004     |      | .10        |      |
| D2  | .011 | .019 | 0.28       | 0.48  |     |          |      |            |      |
| D3  | .600 | ---  | 15.24      | ---   |     |          |      |            |      |
| E   | .551 | .559 | 14         | 14.2  |     |          |      |            |      |
| E1  | .353 | .357 | 8.97       | 9.07  |     |          |      |            |      |
| E2  | .132 | .140 | 3.35       | 3.56  |     |          |      |            |      |
| E3  | .124 | .132 | 3.15       | 3.35  |     |          |      |            |      |
| E4  | .270 | ---  | 6.86       | ---   |     |          |      |            |      |
| E5  | .346 | .350 | 8.79       | 8.89  |     |          |      |            |      |

|   |  |                    |                          |                            |             |
|---|--|--------------------|--------------------------|----------------------------|-------------|
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| TITLE:<br><br>TO-270<br>4 LEAD WIDE BODY                |  |                    | DOCUMENT NO: 98ASA10577D |                            | REV: D      |
|   |  |                    | CASE NUMBER: 1486-03     |                            | 13 AUG 2007 |
|   |  |                    | STANDARD: NON-JEDEC      |                            |             |



|   |  |                          |  |                            |  |
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| TITLE:<br><b>TO-272</b><br>4 LEAD, WIDE BODY            |  | DOCUMENT NO: 98ASA10575D |  | REV: E                     |  |
|   |  | CASE NUMBER: 1484-04     |  | 31 AUG 2007                |  |
|   |  | STANDARD: NON-JEDEC      |  |                            |  |



|   |                          |                            |  |
|---|--------------------------|----------------------------|--|
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| TITLE:<br>TO-272<br>4 LEAD, WIDE BODY                   | DOCUMENT NO: 98ASA10575D | REV: E                     |  |
|   | CASE NUMBER: 1484-04     | 31 AUG 2007                |  |
|   | STANDARD: NON-JEDEC      |                            |  |



NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:  
 PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE        PIN 4 - GATE  
 PIN 5 - SOURCE

| DIM | INCH     |      | MILLIMETER |       | DIM | INCH           |      | MILLIMETER     |      |
|-----|----------|------|------------|-------|-----|----------------|------|----------------|------|
|     | MIN      | MAX  | MIN        | MAX   |     | MIN            | MAX  | MIN            | MAX  |
| A   | .100     | .104 | 2.54       | 2.64  | b1  | .164           | .170 | 4.17           | 4.32 |
| A1  | .039     | .043 | 0.99       | 1.09  | c1  | .007           | .011 | .18            | .28  |
| A2  | .040     | .042 | 1.02       | 1.07  | r1  | .063           | .068 | 1.60           | 1.73 |
| D   | .928     | .932 | 23.57      | 23.67 | e   | .106 BSC       |      | 2.69 BSC       |      |
| D1  | .810 BSC |      | 20.57 BSC  |       | e1  | .239 INFO ONLY |      | 6.07 INFO ONLY |      |
| D2  | .600     | ---  | 15.24      | ---   | aaa | .004           |      | .10            |      |
| E   | .551     | .559 | 14         | 14.2  |     |                |      |                |      |
| E1  | .353     | .357 | 8.97       | 9.07  |     |                |      |                |      |
| E2  | .270     | ---  | 6.86       | ---   |     |                |      |                |      |
| E3  | .346     | .350 | 8.79       | 8.89  |     |                |      |                |      |
| F   | .025 BSC |      | 0.64 BSC   |       |     |                |      |                |      |

|   |                          |                    |                            |
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| TITLE:<br><br>TO-272<br>4 LEAD WIDE BODY                | DOCUMENT NO: 98ASA10575D |                    | REV: E                     |
|   | CASE NUMBER: 1484-04     |                    | 31 AUG 2007                |
|   | STANDARD: NON-JEDEC      |                    |                            |

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date      | Description   |
|----------|-----------|---|
| 4        | Dec. 2006 | <ul style="list-style-type: none"> <li>• Added "TD-SCDMA" to data sheet description, p. 1</li> <li>• Updated Part Numbers in Table 7, Component Designations and Values, to RoHS compliant part numbers, p. 4</li> <li>• Added TD-SCDMA test circuit schematic, component designations and values, component layout, typical characteristic curves, test signal and series impedance, p. 9-12</li> <li>• Added Product Documentation and Revision History, p. 17</li> </ul>   |
| 5        | Dec. 2008 | <ul style="list-style-type: none"> <li>• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2</li> <li>• Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1</li> <li>• Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table and related "Continuous use at maximum temperature will affect MTTF" footnote added and changed 220°C to 225°C in Capable Plastic Package bullet, p. 1</li> <li>• Corrected <math>V_{DS}</math> to <math>V_{DD}</math> in the RF test condition voltage callout for <math>V_{GS(Q)}</math>, and added "Measured in Functional Test", On Characteristics table, p. 2</li> <li>• Updated PCB information to show more specific material details, Figs. 1, 16, Test Circuit Schematic, p. 3, 9</li> <li>• Updated Part Numbers in Tables 6, 7, Component Designations and Values, to latest RoHS compliant part numbers, p. 3, 9</li> <li>• Removed lower voltage tests from Fig. 11, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 6</li> <li>• Replaced Fig. 12, MTTF versus Junction Temperature with updated graph. Removed Amps<sup>2</sup> and listed operating characteristics and location of MTTF calculator for device, p. 7</li> <li>• Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 13-15. Added pin numbers 1 through 4 on Sheet 1.</li> <li>• Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 16-18. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations.</li> </ul> |

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