

# NCP2811

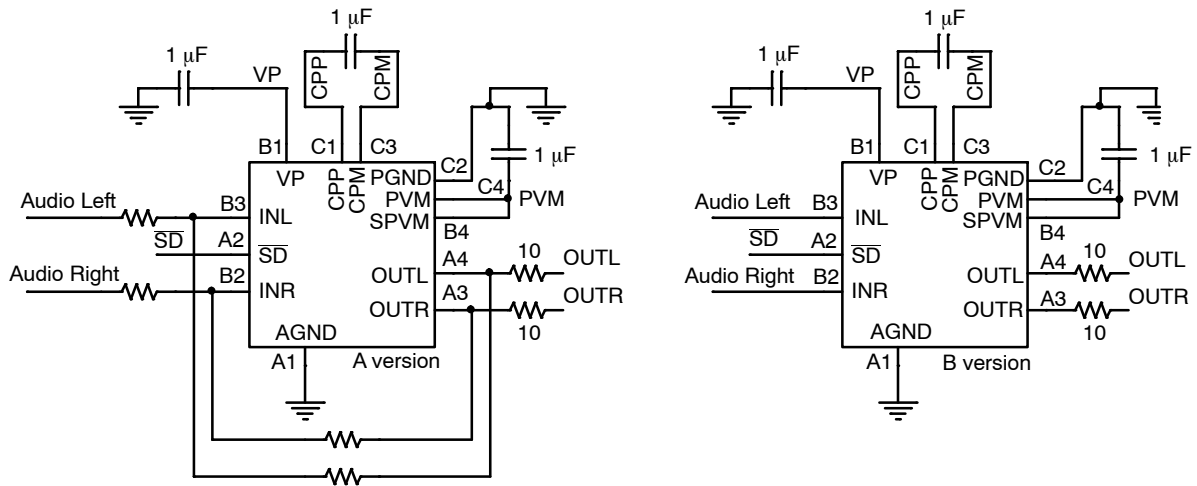


Figure 1. Application Schematics

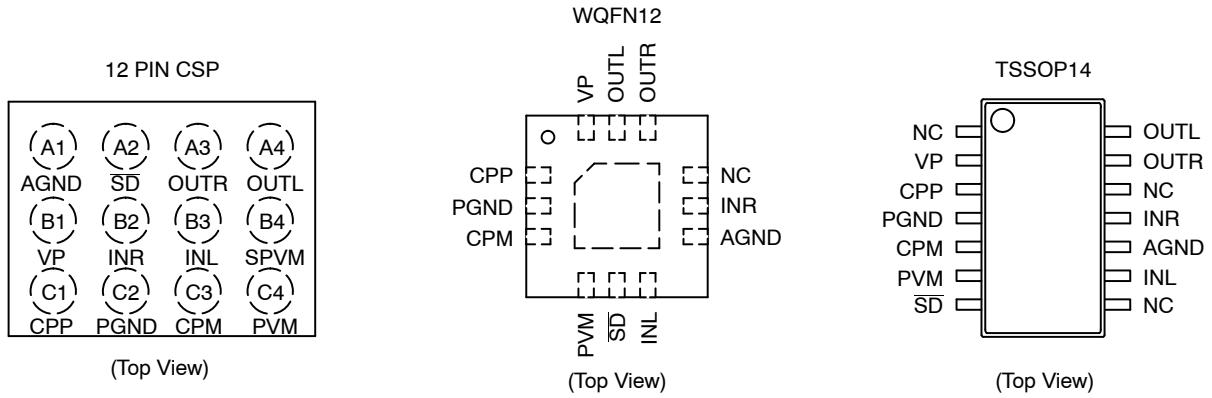


Figure 2. Pin Configurations

# NCP2811

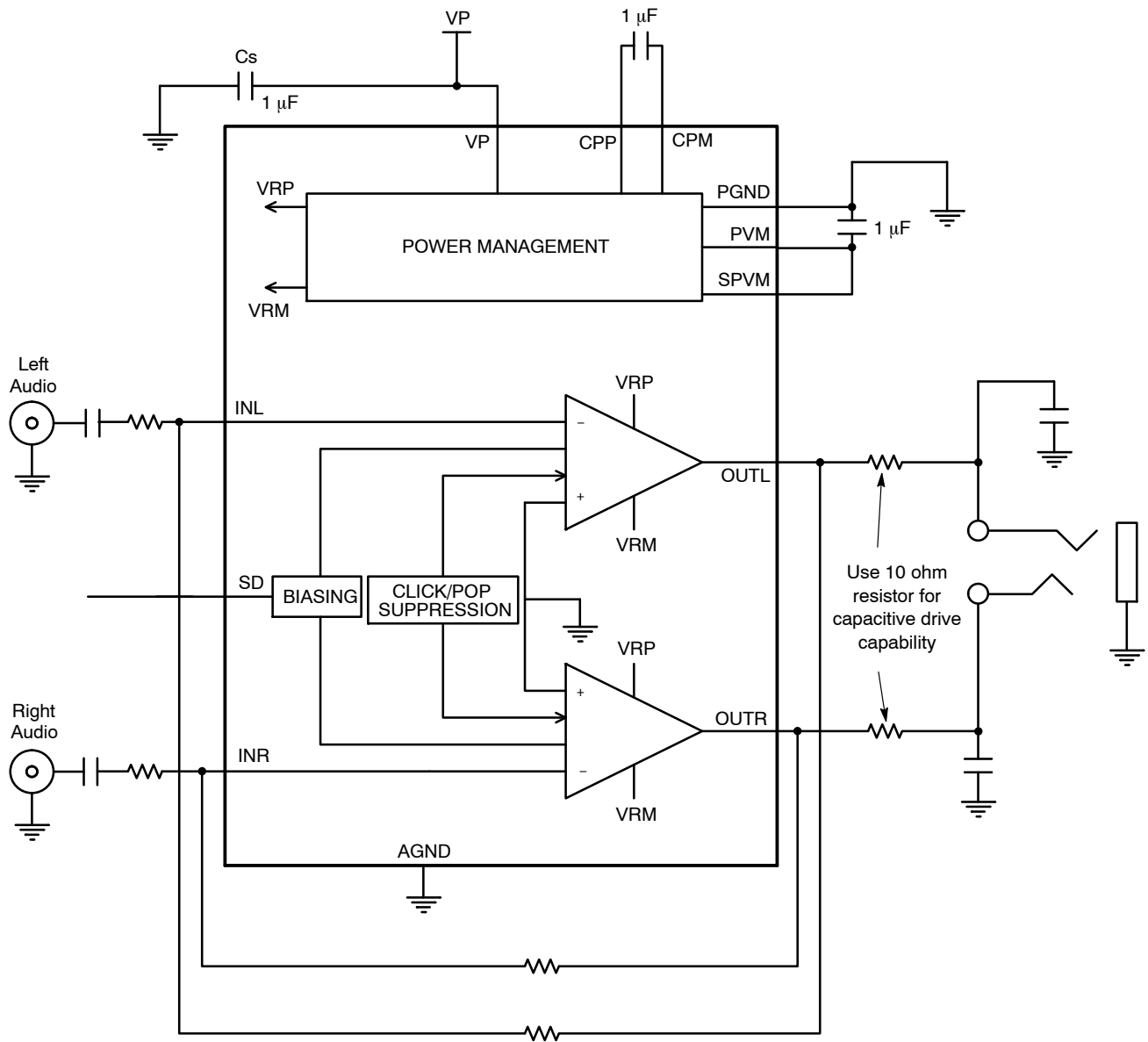


Figure 3. Typical Application Schematic version A

# NCP2811

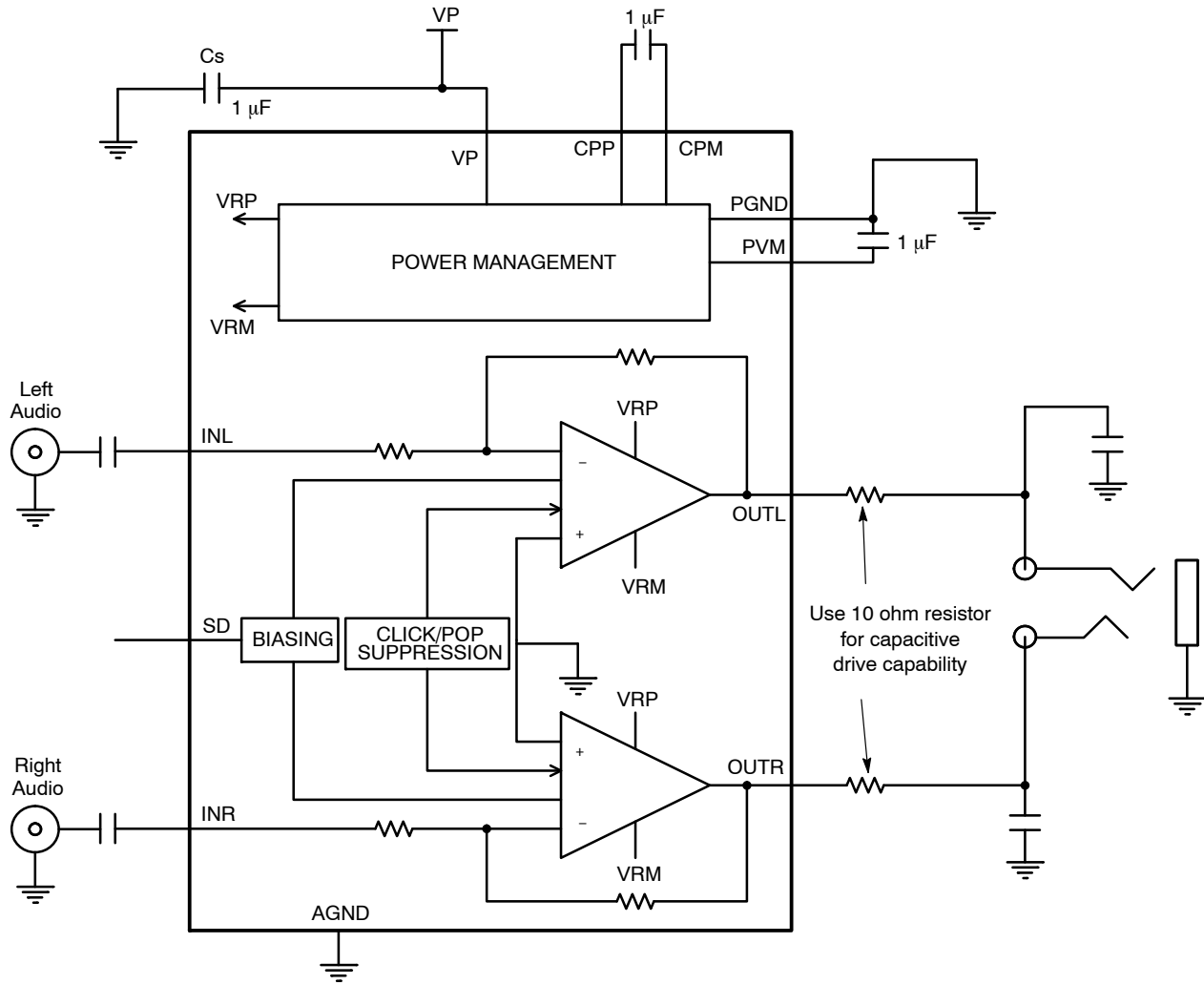


Figure 4. Typical Application Schematic version B

Table 1. PIN FUNCTION DESCRIPTION

PIN CSP	PIN TQFN	PIN TS-SOP	PIN NAME	TYPE	DESCRIPTION
A1	7	10	AGND	GROUND	Analog ground. Connect to ground reference
A2	5	7	SD	INPUT	Enable activation
A3	10	13	OUTR	OUTPUT	Right audio channel output signal
A4	11	14	OUTL	OUTPUT	Left audio channel output signal
B1	12	2	VP	POWER	Positive supply voltage. It can be connected for example to a Lithium/Ion battery
B2	8	11	INR	INPUT	Right input of the first audio source
B3	6	9	INL	INPUT	Left input of the first audio source
B4	-	-	SPVM	POWER	Amplifier negative power supply voltage. Connect to PVM
C1	1	3	CPP	INPUT/OUTPUT	Charge pump flying capacitor positive terminal. A 1 μF ceramic filtering capacitor to CPM is needed
C2	2	4	PGND	GROUND	Power ground, connect to ground reference
C3	3	5	CPM	INPUT	Charge pump flying capacitor negative terminal. A 1 μF ceramic filtering capacitor to CPP is needed
C4	4	6	PVM	OUTPUT	Charge pump output. A 1 μF ceramic filtering capacitor to ground is needed

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**Table 2. MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
AVIN, PVIN Pins: Power Supply Voltage (Note 2)	V <sub>P</sub>	- 0.3 to + 6.0	V
INL, INR Pins: Input (Note 2) A version B version	V <sub>IN</sub>	-V <sub>P</sub> - 0.3 to V <sub>P</sub> + 0.3 -2 to +2	V
$\overline{SD}$ Pin: Input (Note 2)	V <sub>YY</sub>	-0.3 to V <sub>P</sub> + 0.3	V
Human Body Model (HBM) ESD Rating are (Note 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 3)	ESD MM	200	V
CSP 1.5 x 2.0 mm package (Notes 6 and 7) Thermal Resistance Junction to Case	R <sub>θJC</sub>	(Note 7)	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to + 85	°C
Operating Junction Temperature Range	T <sub>J</sub>	-40 to + 125	°C
Maximum Junction Temperature (Note 6)	T <sub>JMAX</sub>	+ 150	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Notes:**

- Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T<sub>A</sub> = 25°C.
- According to JEDEC standard JESD22-A108B.
- This device series contains ESD protection and passes the following tests:  
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114 for all pins.  
Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115 for all pins.
- Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.
- The thermal shutdown set to 150°C (typical) avoids irreversible damage on the device due to power dissipation.
- The R<sub>JA</sub> is highly dependent of the PCB Heatsink area. For example, R<sub>JA</sub> can equal 195°C/W with 50 mm<sup>2</sup> total area and also 135°C/W with 50 mm<sup>2</sup>. The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

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**Table 3. ELECTRICAL CHARACTERISTICS** Min & Max Limits apply for  $T_A$  between  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $T_J$  up to  $+125^{\circ}\text{C}$  for  $V_{IN}$  between 2.7 V to 5.0 V (Unless otherwise noted). Typical values are referenced to  $T_A = +25^{\circ}\text{C}$  and  $V_{IN} = 3.6\text{ V}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_P$	Operational Power Supply		2.7		5.0	V
$I_{DD}$	Supply quiescent current	Both channels enabled		6.0		mA
$I_{SD}$	Shutdown current	$V_P = 2.7\text{ V to }5.0\text{ V}$			1	$\mu\text{A}$
$V_{OS}$	Output offset voltage	$V_P = 2.7\text{ V to }5.0\text{ V}$		$\pm 1$		mV
$V_{IH}$	High-Level input voltage SD pin		1.2			V
$V_{IL}$	Low-Level input voltage SD pin				0.4	V
$R_{SD}$	SD pin pull-down impedance			190		$\text{K}\Omega$
$T_{WU}$	Turning on time			1		ms
$T_{SD}$	Thermal shutdown temperature			160		$^{\circ}\text{C}$
$V_{LP}$	Max output swing (peak value)	$V_P = 2.9\text{ V to }5.0\text{ V}$ Headset $\geq 16\ \Omega$ THD+N = 1%	1			$V_{RMS}$
$P_O$	Max output power (output in phase)	$V_P = 2.7\text{V}$ , THD+N = 1% Headset = $16\ \Omega$		27		mW
		$V_P = 2.7\text{V}$ , THD+N = 1% Headset = $32\ \Omega$		37		
		$V_P = 3.6\text{V}$ , THD+N = 1% Headset = $16\ \Omega$		90		
		$V_P = 3.6\text{V}$ , THD+N = 1% Headset = $32\ \Omega$		64		
		$V_P = 5.0\text{V}$ , THD+N = 1% Headset = $16\ \Omega$		110		
		$V_P = 5.0\text{V}$ , THD+N = 1% Headset = $32\ \Omega$		64		
	Crosstalk (Note 8)	Headset $\geq 16\ \Omega$		-80	-60	dB
PSRR	Power supply rejection ratio (Note 8)	$V_P = 2.7\text{ V to }5.0\text{ V}$ Input shorted to ground $F = 217\text{ Hz}$ $F = 1\text{ kHz}$		-106 -95		dB
THD+N	Total harmonic distortion + noise (Note 8)	Headset = $16\ \Omega$ $P_{OUT} = 25\text{ mW}$		0.01		%
$V_N$	Output noise voltage (Note 8)	A-Weighting filter		7		$\mu\text{V}_{RMS}$
$Z_{IN}$	Input impedance	B version only		20		$\text{K}\Omega$
$Z_{SD}$	Output impedance in shutdown mode			10		$\text{K}\Omega$
UVLO	UVLO threshold	Falling edge		2.3		V
UVLO <sub>HYST</sub>	UVLO hysteresis			100		mV
$A_v$	Voltage Gain	B version only	-1.53	-1.5	-1.48	V/V

8. Guaranteed by design and characterized.

TYPICAL OPERATING CHARACTERISTICS

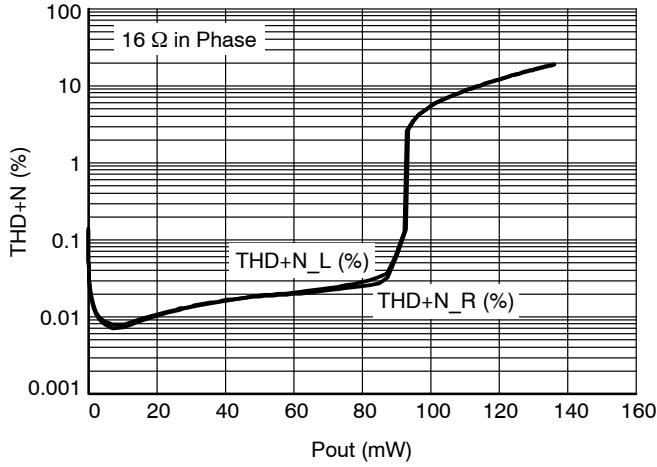


Figure 5. THD+N vs. Pout @ Vp = 3.6 V

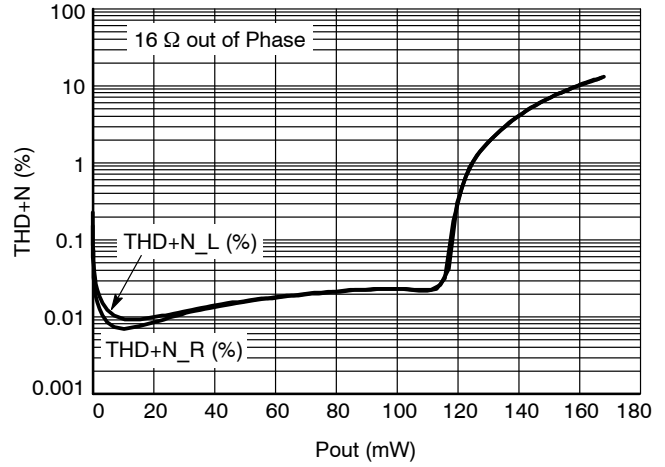


Figure 6. THD+N vs. Pout @ Vp = 3.6 V

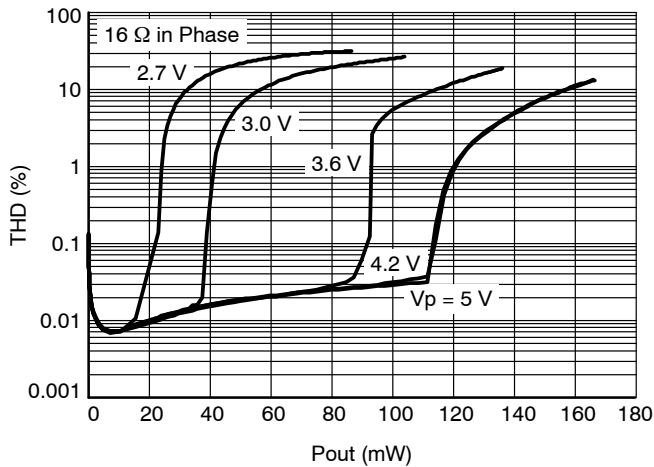


Figure 7. THD+N vs. Pout LEFT

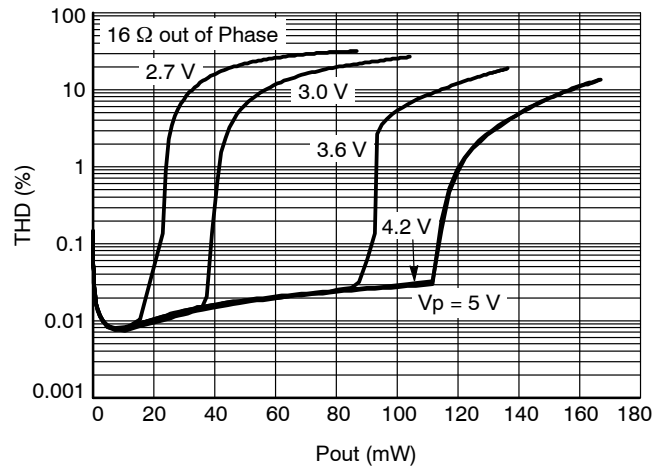


Figure 8. THD+N vs. Pout RIGHT

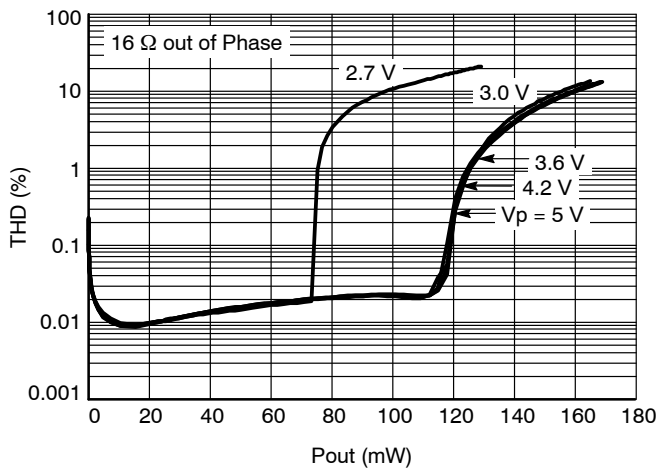


Figure 9. THD+N vs. Pout LEFT

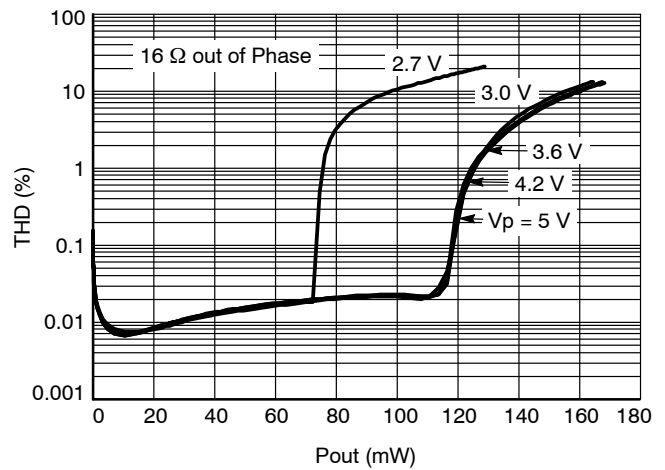


Figure 10. THD+N vs. Pout RIGHT

TYPICAL OPERATING CHARACTERISTICS

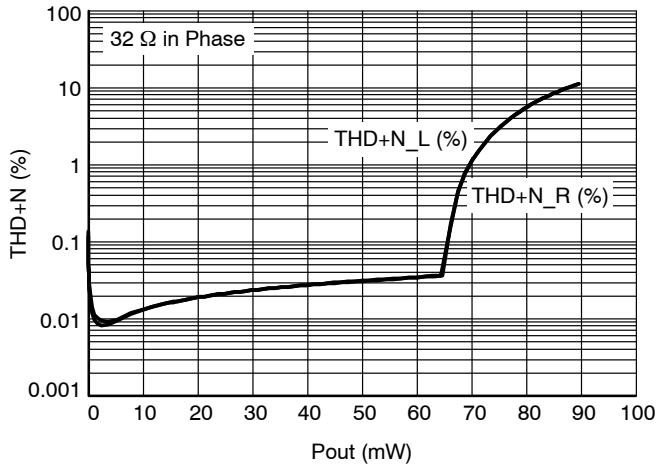


Figure 11. THD+N vs. Pout @ Vp = 3.6 V

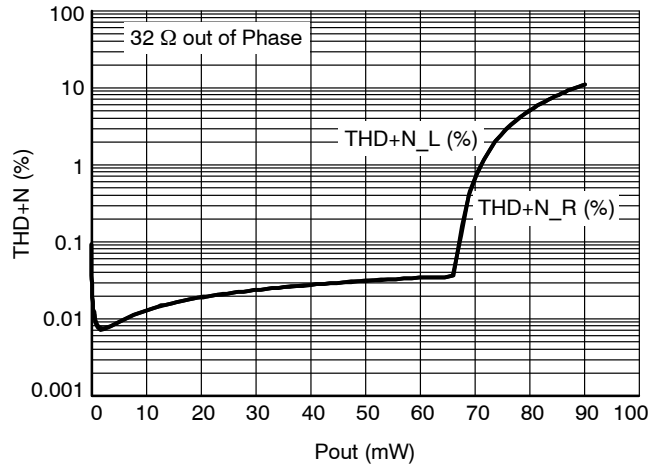


Figure 12. THD+N vs. Pout @ Vp = 3.6 V

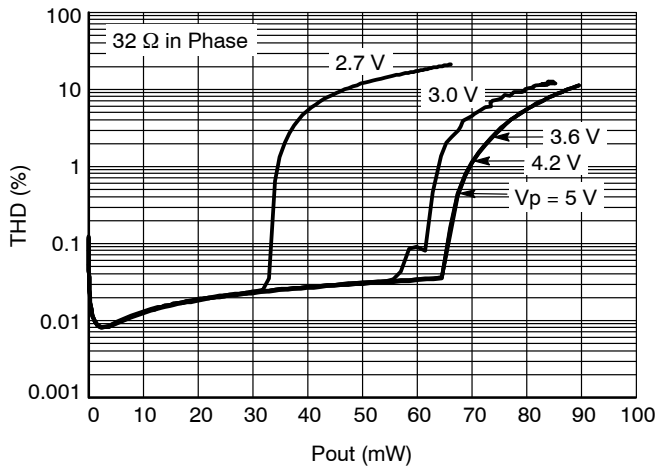


Figure 13. THD+N vs. Pout LEFT

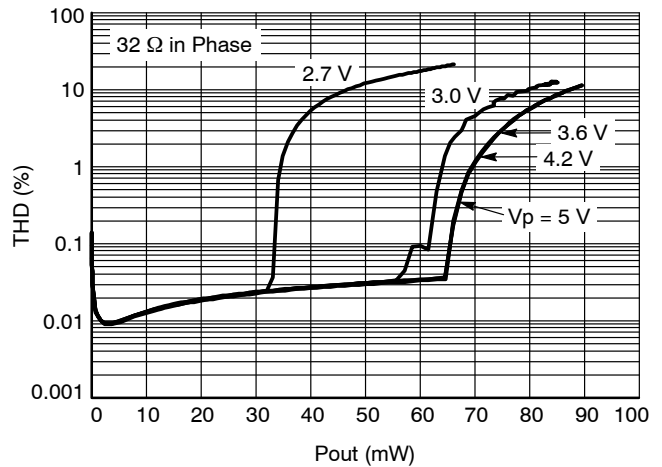


Figure 14. THD+N vs. Pout RIGHT

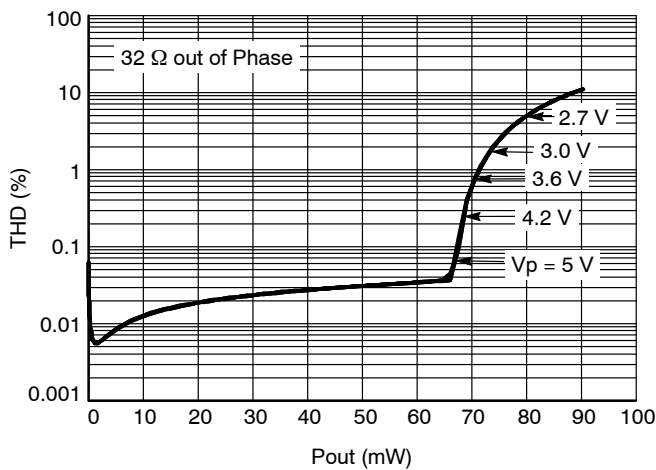


Figure 15. THD+N vs. Pout LEFT

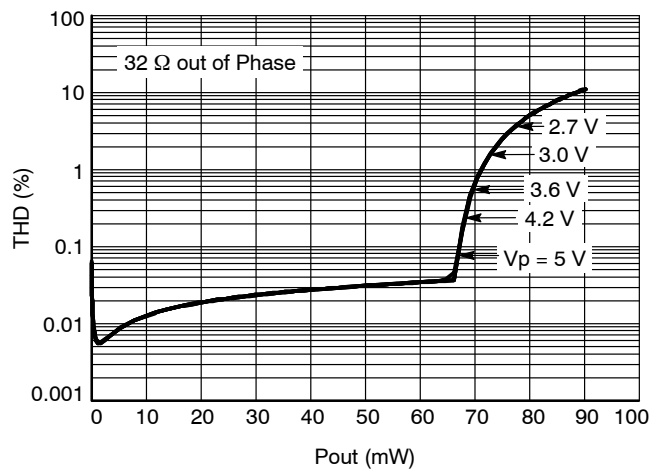


Figure 16. THD+N vs. Pout RIGHT

TYPICAL OPERATING CHARACTERISTICS

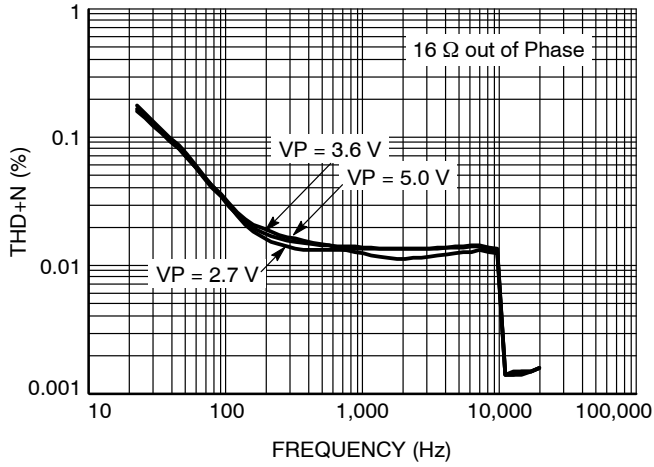


Figure 17. THD vs. Frequency LEFT @ Pout = 32 mW

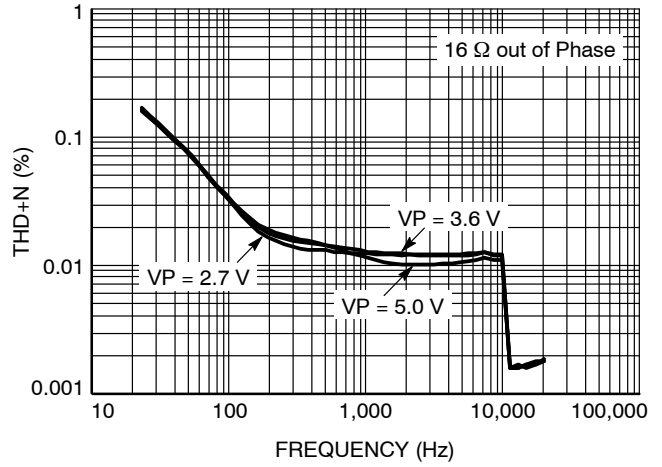


Figure 18. THD vs. Frequency RIGHT @ Pout = 32 mW

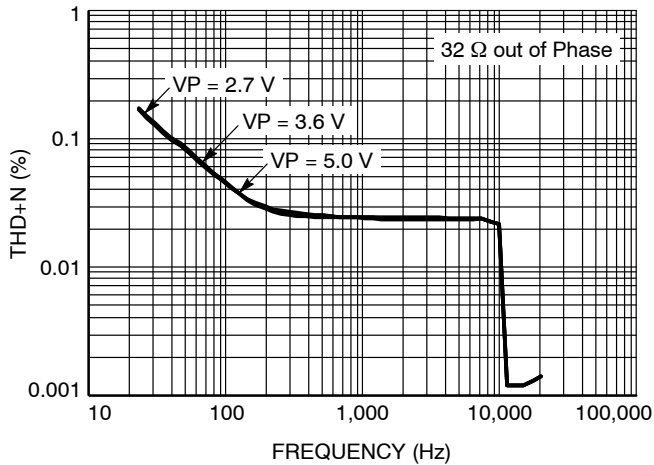


Figure 19. THD vs. Frequency LEFT @ Pout = 32 mW

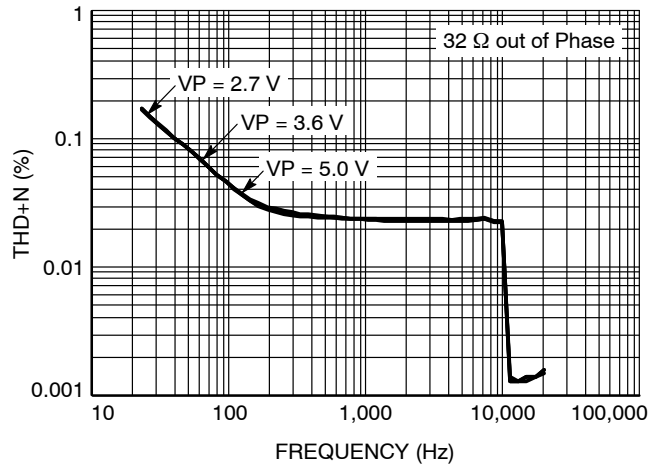


Figure 20. THD vs. Frequency RIGHT @ Pout = 32 mW

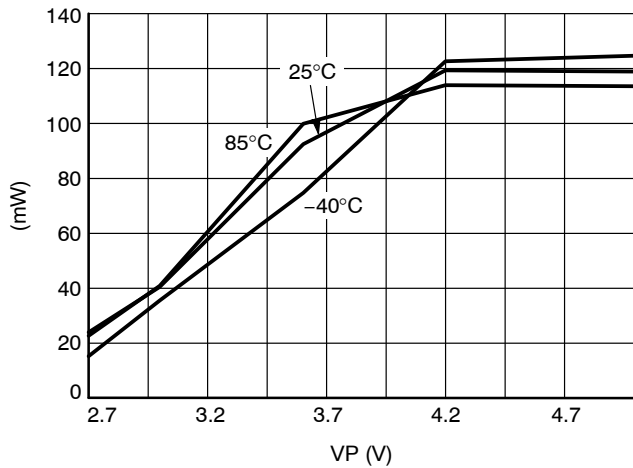


Figure 21. Maximum Output Power LEFT vs. VP (THD+N < 1%)

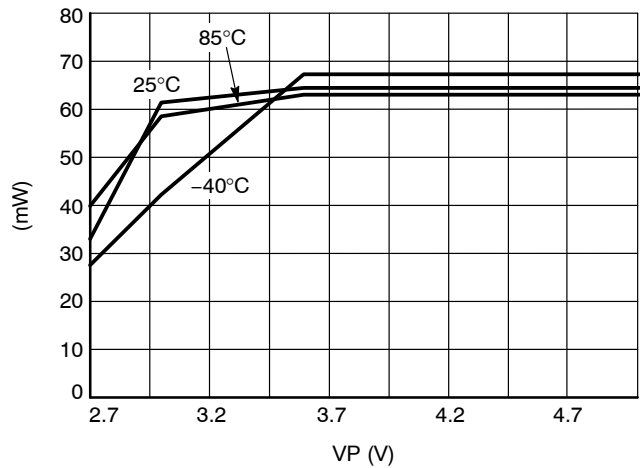


Figure 22. Maximum Output Power LEFT vs. VP (THD+N < 0.1%)



# NCP2811

## TYPICAL OPERATING CHARACTERISTICS

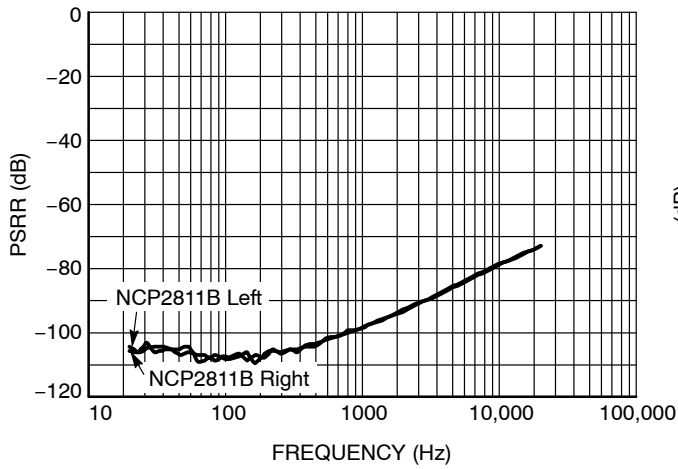


Figure 23. PSRR at  $V_p = 3.6\text{ V}$

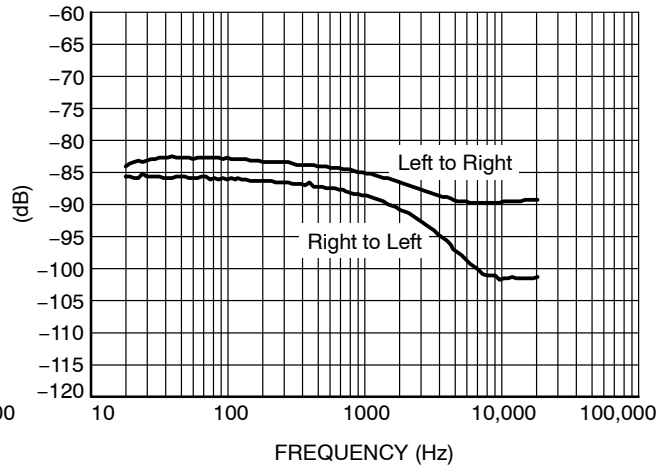


Figure 24. Crosstalk vs. Frequency  
@  $V_p = 3.6\text{ V}$

## DETAIL OPERATING DESCRIPTION

### Detailed Descriptions

The NCP2811 is a stereo headphone amplifier with a true ground architecture. This architecture eliminates the need to use 2 external big capacitors required by conventional headphone amplifier.

The structure of the NCP2811 is basically composed of 2 true ground amplifiers, an UVLO, a short circuit protection and also a thermal shutdown. A special circuitry is embedded to eliminate any pop and click noise that occurs during turn on and turn off time. The A version has an external gain selectable by two resistor, B version has a gain of 1.5 V/V.

### NOCAP™

NOCAP™ is a patented architecture which requires only 2 small ceramic capacitors. It generates a symmetrical positive and negative voltage and it allows the output of the amplifiers to be biased around the ground.

### Current Limit Protection Circuit

The NCP2811 embed a protection circuitry against short to ground. When an output is shorted to GND and when a signal appears at the input, the current is limited to 300 mA.

### Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceed 160°C, and will be switch on again when the temperature decrease below 140°C.

### Under Voltage Lockout

When the battery voltage decreases below 2.3 V, the amplifiers are turned off. The hysteresis to turn on it again is 100 mV.

### Pop and Click Suppression Circuitry

The NCP2811 includes a special circuitry to eliminate any pop and click noise during turn on and turn off time. Basic amplifier creates an offset during these transitions at the output which give a parasitic noise called “pop and click noise”. The NCP2811 eliminates this problem.

### Gain Setting Resistor Selection (R<sub>in</sub> & R<sub>f</sub>, A version only)

R<sub>in</sub> and R<sub>f</sub> set the closed loop gain of the amplifier. A low gain configuration (close to 1) minimizes the THD + noise values and maximizes the signal to noise ratio.

A closed loop gain in the range of 1 to 10 is recommended to optimize overall system performance.

The formula to calculate the gain is:

$$A_v = - \frac{R_f}{R_{in}}$$

### Input Capacitor Selection

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high-pass

filter with R<sub>in</sub> (externally selectable for A version, 20 kΩ for B version).

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation in the audio bandwidth (20 Hz – 20 kHz).

The cut off frequency for the input high-pass filter is:

$$F_c = \frac{1}{2\pi R_{in} C_{in}}$$

A F<sub>c</sub> < 20 Hz is recommended.

### Charge Pump Capacitor Selection

Use ceramic capacitor with low ESR for better performances. X5R / X7R capacitor is recommended.

The flying capacitor (C2) serves to transfer charge during the generation of the negative voltage.

The CPVM capacitor (C3) must be equal at least to the CFly capacitor to allow maximum transfer charge. The CPVM value must not exceed 1 μF. Higher capacitor value can damage the part.

Table 4 suggests typical value and manufacturer:

**Table 4.**

Value	Reference	Package	Manufacturer
1 μF	C1005X5R0J105K	0402	TDK
1 μF	GRM155R60J105K19	0402	Murata

Lower value of capacitors can be used but the maximum output power is reduced and the device may not operate to specifications.

### Power Supply Decoupling Capacitor (C1)

The NCP2811 is a True Ground amplifier which requires the adequate decoupling capacitor to reduce noise and THD+N. Use X5R / X7R ceramic capacitor and place it closed to the CPVDD pin. A value of 1 μF is recommended.

### Shutdown Function

The device enters in shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 500 nA. In this configuration, the output impedance is 10 kΩ on each output.

### Output Resistor for Capacitive Drive Capability

Under normal operation, NCP2811 maximum direct capacitive load is in the 80 pF range. If, for any reason, high value capacitive loads should be connected to NCP2811 outputs, an additional 10 Ω resistor should be placed between the NCP2811 output and the capacitive load to ensure amplifier stability.

### Layout Recommendation

Connect C1 as close as possible of the V<sub>p</sub> pin.

Connect C2 and C3 as close as possible of the NCP2811.

Route audio signal and AGND far from V<sub>p</sub>, CPP, CPM, PVM and PGND to avoid any perturbation due to the switching.

# NCP2811

**Table 5. ORDERING INFORMATION**

Device	Package	Shipping†
NCP2811ADTBR2G	TSSOP-14 (Pb-Free)	2500/Tape & Reel
NCP2811BDTBR2G	TSSOP-14 (Pb-Free)	2500/Tape & Reel
NCP2811AFCT1G	Flip-Chip 12 (Pb-Free)	3000/Tape & Reel
NCP2811BFCT1G	Flip-Chip 12 (Pb-Free)	3000/Tape & Reel
NCP2811BFCCT1G	Flip-Chip 12 (Backside Laminate Coating) (Pb-Free)	3000/Tape & Reel
NCP2811AMTTXG	WQFN12 (Pb-Free)	3000/Tape & Reel
NCP2811BMTTXG	WQFN12 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

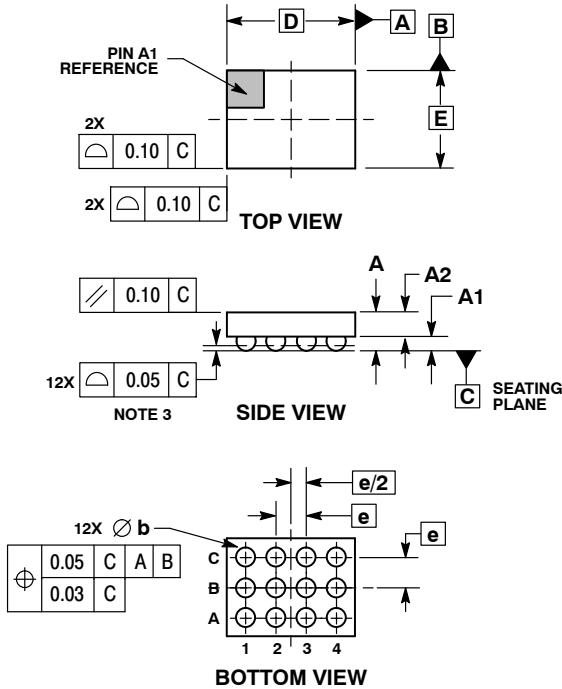


### 12 PIN FLIP-CHIP, 2.0x1.5, 0.5P CASE 499AZ-01 ISSUE O

DATE 20 MAY 2008



SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	0.54	0.60
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.00 BSC	
E	1.50 BSC	
e	0.50 BSC	

### GENERIC MARKING DIAGRAM\*

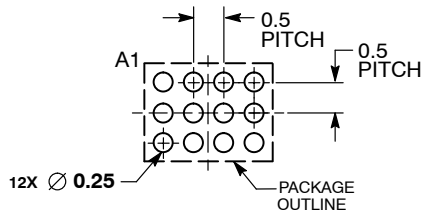


- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "■", may or may not be present.

### SOLDERING FOOTPRINT\*



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<b>DESCRIPTION:</b>	<b>12 PIN FLIP-CHIP, 2.0 X 1.5, 0.5P</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

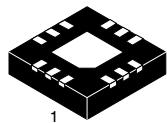
## PACKAGE DIMENSIONS

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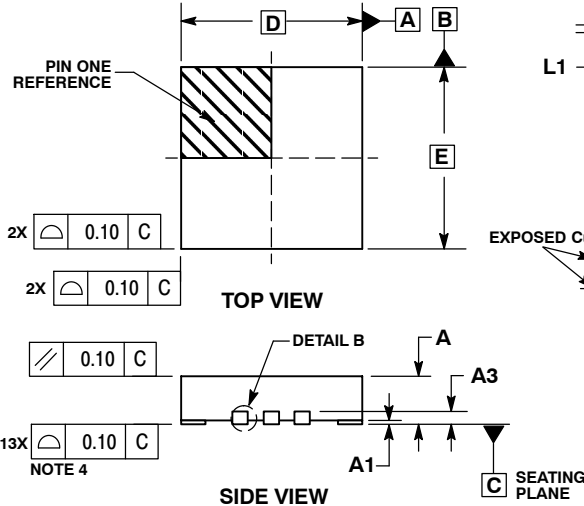


DATE 20 JAN 2009

WQFN12 3x3, 0.5P  
CASE 510AH-01  
ISSUE O



SCALE 4:1

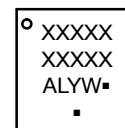


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.65	0.85
A1	0.00	0.05
A3	0.22	REF
b	0.20	0.30
D	3.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.30	1.50
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

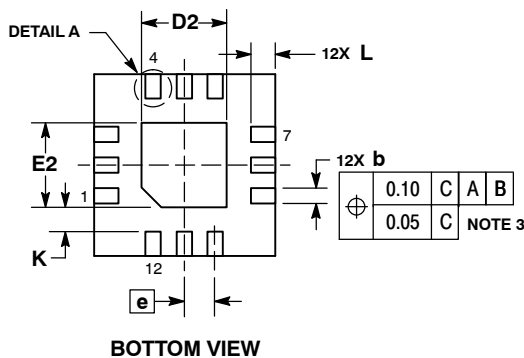
**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON38317E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>WQFN12, 3X3, 0.5P</b>	<b>PAGE 1 OF 2</b>



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT**



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