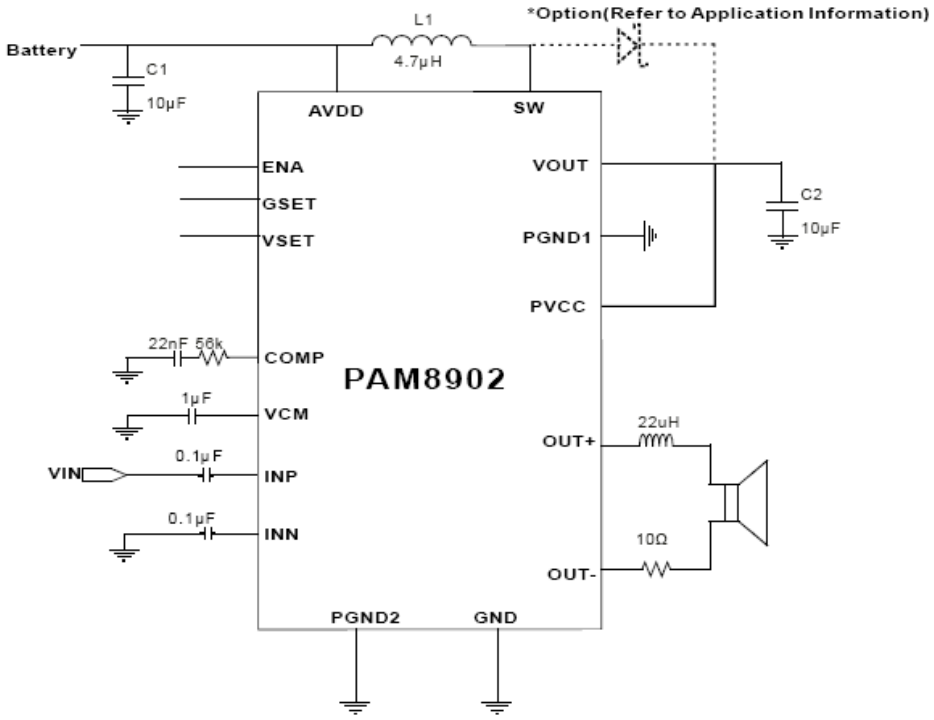
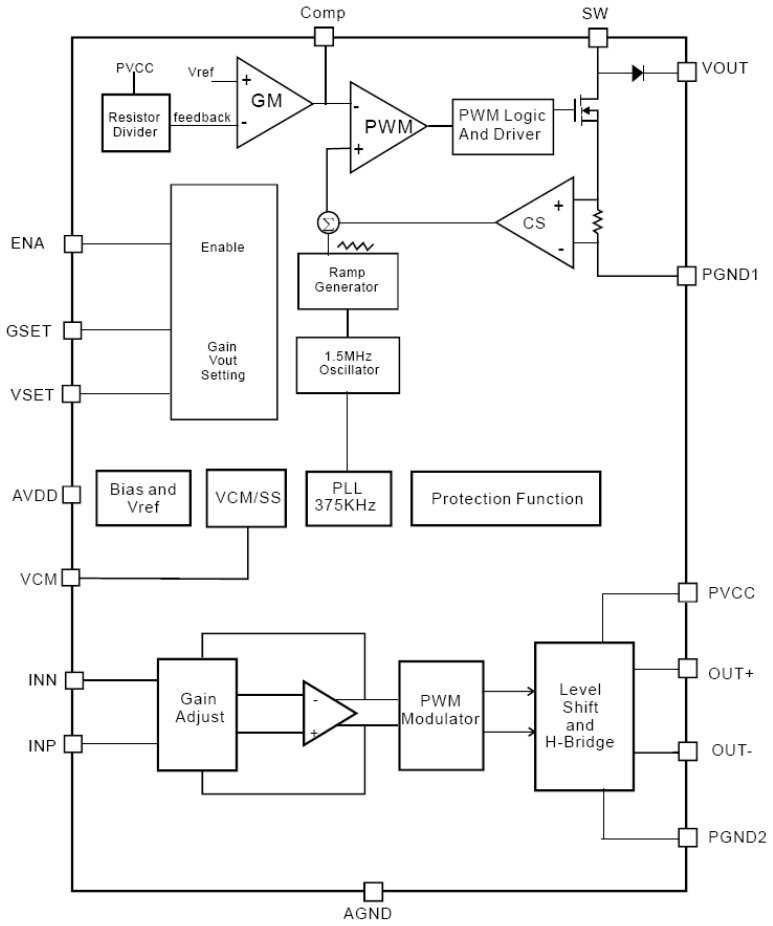
Typical Applications Circuit



Pin Descriptions

Pin Name	Bump (CSP)	Pin Number QFN4x4	Function
PVCC	A1	16	Audio Amplifier Power Supply
VOUT	A2	1	Boost Converter Output
SW	A3	2	Boost Converter Switching Node
PGND1	A4	4	Boost Converter Power Ground
OUT+	B1	15	Positive Differential Audio Output
VSET	B2	3	Boost Converter Output Voltage Setting(8V,12V,17.5V)
COMP	B3	5	Boost Converter Compensation
AVDD	B4	6	Power Supply
OUT-	C1	14	Negative Differential Audio Output
GSET	C2	11	Amplifier Gain Setting (18dB , 22dB , 26dB)
VCM	C3	7	Common Mode Bypass Cap
AGND	C4	8	Analog Ground
PGND2	D1	13	ClassD Power Ground
ENA	D2	12	Whole Chip Enable
INN	D3	10	Negative Differential Audio Input
INP	D4	9	Positive Differential Audio Input

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage	6.0	V
Input Voltage	-0.3 to V_{DD} +0.3	
Maximum Junction Temperature	+150	°C
Storage Temperature	-65 to +150	
Soldering Temperature	350, 10sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage Range	2.5 to 5.5	V
Ambient Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	°C

Thermal Information

Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Ambient)	CSP	θ_{JA}	90	°C/W
	QFN4x4-16		52	
Thermal Resistance (Junction to Case)	CSP	θ_{JC}	75	
	QFN4x4-16		30	

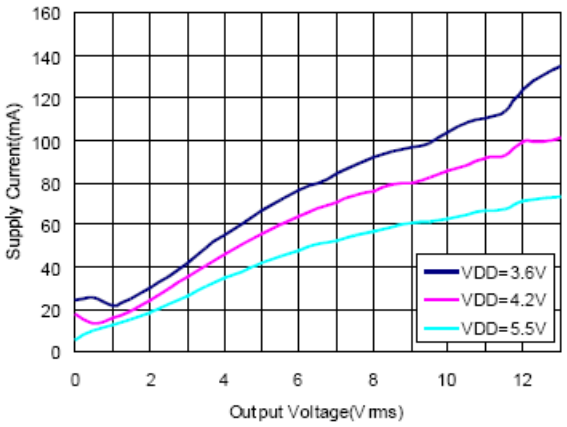
Electrical Characteristics (@T_A = +25°C, V_{DD} = 3.6V, C_L = 1µF, V_{SET} Float, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{DD}		2.5		5.5	V
Quiescent Current	I_Q	EN > 1.2V, V_{SET} = High		30	48	mA
		EN > 1.2V, V_{SET} = Floating		10	18	
		EN > 1.2V, V_{SET} = GND		5	12	
Shutdown Current	I_{SD}	EN = 0V		0.1	1	µA
Wake-Up Time	T_{WU}	EN from Low to High		40		mS
Chip Enable	V_{EH}		1.2			V
Chip Disable	V_{EL}				0.4	
GSET/ VSET High	V_H		V_{DD} -0.5		V_{DD}	V
GSET/ VSET Floating	V_F		1		V_{DD} -1	
GSET/ VSET Low	V_L		0		0.5	
Under Voltage Lockout Threshold	UVLO	VDD from High to Low		2.2		V
Under Voltage Lockout Hysteresis	UVLO(H)	VDD from Low to High		0.2		
Thermal Shutdown Threshold	OTP			150		°C
Thermal Shutdown Lockout Hysyeresis	OTP(H)			30		°C
Boost Converter						
Output Voltage	V_O1	V_{SET} = GND, No Load	7.2	8	8.8	V
	V_O2	V_{SET} = NC, No Load	10.8	12	13.2	V
	V_O3	V_{SET} = AVDD, No Load	16	17.5	19	V
Current Limit	C_L	Average Input Current		0.8		A
Lowside MOSFET $R_{DS(ON)}$	R_{LS}	I_O = 50mA		0.5		Ω
Boost Switching Frequency	f_{OSCB}		1.1	1.5	1.9	MHz
Class D						
Class D Amplifier Switching Frequency	f_{OSCD}	Input AC-GND	225	375	475	KHz
Common Mode Reject Ratio	CMRR	V_{IN} = + -100mV, V_{DD} = 3.6V		60		dB
Output Offset Voltage	V_{OS}	Output Offset Voltage		5	50	mV
$R_{DS(ON)}$	RP	High Side		1.5		Ω
		Low Side		0.6		Ω
Closed-Loop Voltage Gain	A_V1	G_{SET} = AVDD, VO = $1V_{RMS}$	25	26	27	dB
	A_V2	G_{SET} = NC, VO = $1V_{RMS}$	21	22	23	
	A_V3	G_{SET} = GND, VO = $1V_{RMS}$	17	18	19	
Power Supply Reject Ratio	PSRR	200m V_{PP} Supply Ripple @ 217Hz		70		dB
Total Harmonic Distortion Plus Noise	THD+N	V_O = 5VRMS		0.3		%
Signal to Noise Ratio	SNR	Input AC Ground, A–Weighting		90		dB

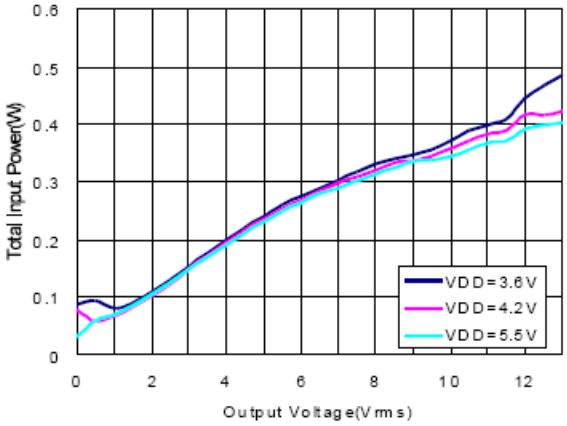
Typical Performance Characteristics

(@T_A = +25°C, V_{DD} = 4.2V, Gain = 26dB, C_{IN} = 1µF, C_{LOAD} = 1µF, unless otherwise specified.)

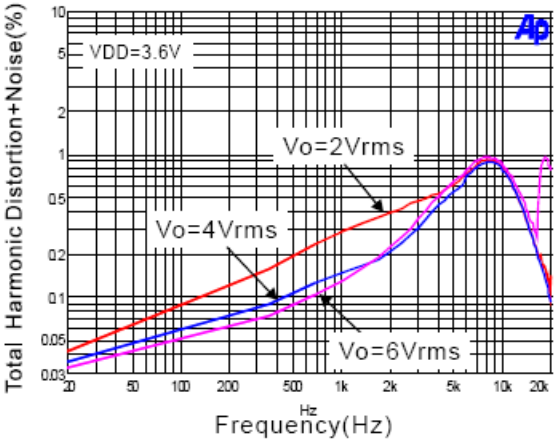
1. Total Supply Current VS Output Voltage



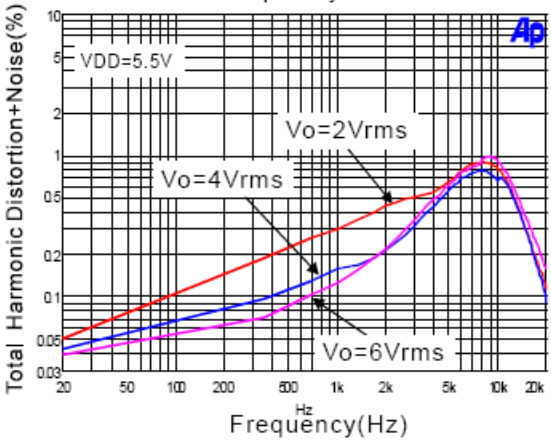
2. Total Input Power VS Output Voltage



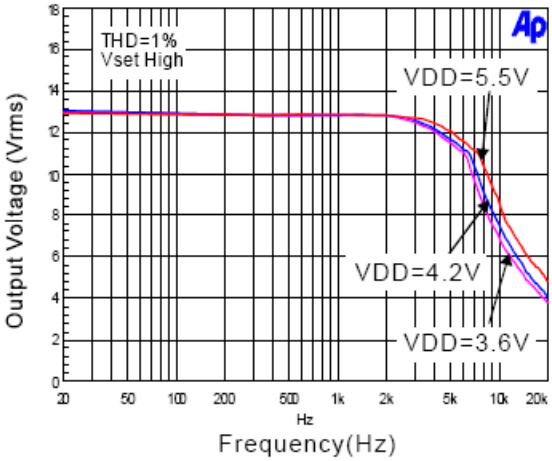
3. THD+N VS Frequency



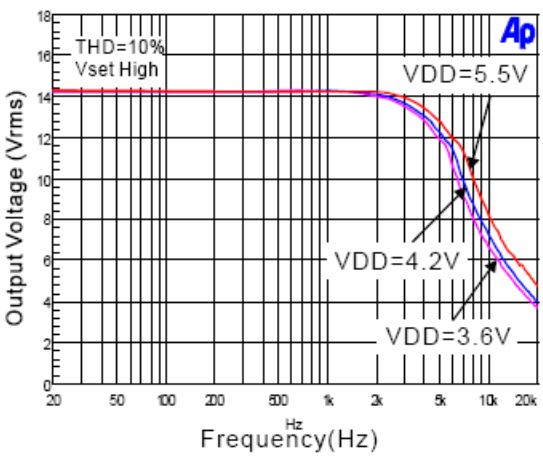
4. THD+N VS Frequency



5. Output Voltage RMS VS Frequency

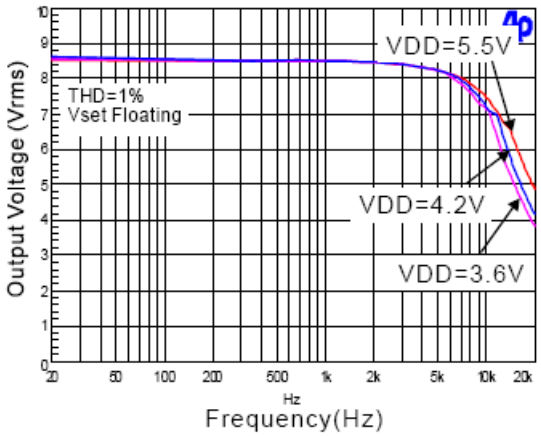


6. Output Voltage RMS VS Frequency

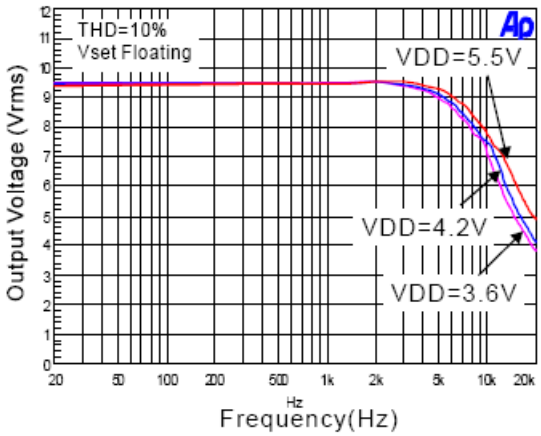


Typical Performance Characteristics (cont.) (@T_A = +25°C, V_{DD} = 5V, Gain = 18dB, unless otherwise specified.)

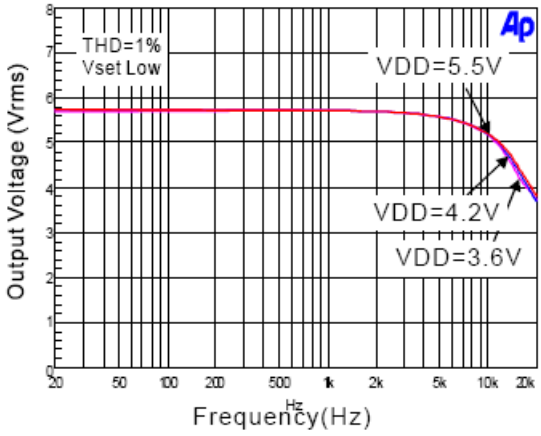
7. Output Voltage RMS VS Frequency



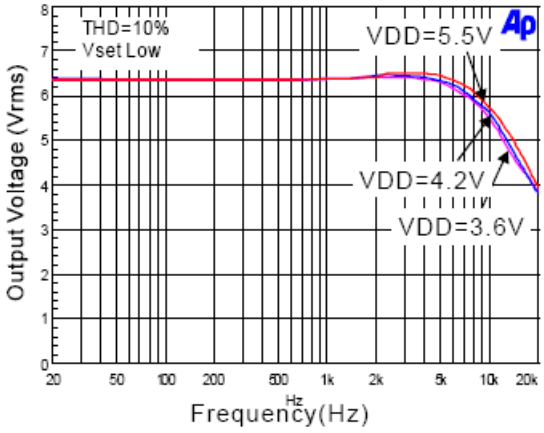
8. Output Voltage RMS VS Frequency



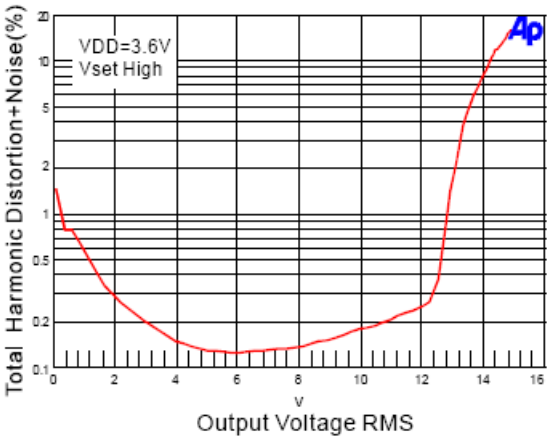
9. Output Voltage RMS VS Frequency



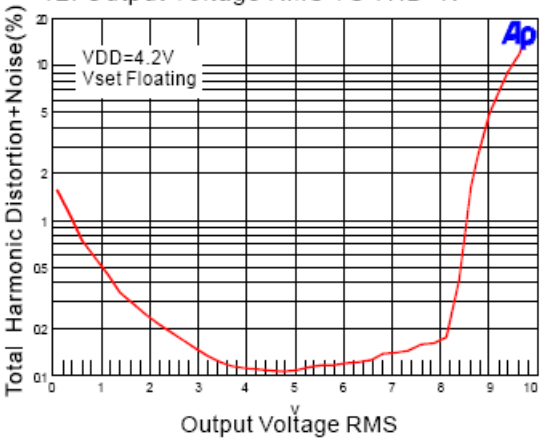
10. Output Voltage RMS VS Frequency



11. Output Voltage RMS VS THD+N



12. Output Voltage RMS VS THD+N



Application Information

Select Boost Converter Output Voltage

Customer can use V_{SET} pin to set boost converor output voltage between 8V, 12V and 17.5V. V_{SET} pin configuration table as below:

V_{SET} Pin Configuration	Min	Max	PVCC Voltage	Audio Amplifier Maximum Output Voltage
Connect to AVDD	AVDD – 0.5	AVDD	17.5V	11 V_{RMS} (V_{PP} = 31.1V)
Floating	1V	AVDD – 1V	12V	8 V_{RMS} (V_{PP} = 22.6V)
Connect to GND	GND	0.5V	8V	5 V_{RMS} (V_{PP} = 14.1V)

Input Resistance (R_I)

The input resistors ($R_I = R_{IN} + R_{EX}$) set the gain of the amplifier according to Equation 1 when anti-saturation is inactive.

$G = 20 \text{ Log } [12.8*R_F/ (R_{IN} + R_{EX})]$ (dB)

G_{SET}	R_{IN}	R_{FB}
$G_{SET} = V_{DD}$	77.4kΩ	122.6kΩ
G_{SET} = Floating	100kΩ	100kΩ
G_{SET} = GND	122.6kΩ	77.4kΩ

Where R_{IN} is a 77.4KΩ internal resistor, R_{EX} is the external input resistor, R_F is a 122.6KΩ internal resistor. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%. Place the input resistors very close to the PAM8902 to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to lower. Lower gain allows the PAM8902 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise. In addition to these features, higher value of R_I minimizes pop noise.

Input Capacitors (C_I)

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance R_I form is a high-pass filter with the corner frequency determined in the follow equation:

$$F_C = \frac{1}{2\Pi R_I C_I}$$

It is important to consider the value of C_I as it directly affects the low frequency performance of the circuit.
For example, when R_I is 150k and the specification calls for a flat bass response are down to 150Hz.
Equation is reconfigured as followed:

$$C_I = \frac{1}{2\Pi R_{IFC}}$$

When input resistance variation is considered, the C_I is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I, $R_I + R_F$) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at V_{DD} /2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Application Information

Decoupling Capacitor

The PAM8902 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent series-resistance (ESR) ceramic capacitor, typically 1µF is placed as close as possible to the device AVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10µF or greater placed near the AVDD supply trace is recommended.

External Schottky Diode

Use external schottky diode can get the best driving capability and efficiency.

Since internal power diode has limited driving capability, only in following conditions customer can remove the external schottky diode to reduce the cost.

1. VSET = GND or Floating and C_L less than 1µF.
2. The signal frequency less than 4KHz.
3. Haptic application (50-500Hz)

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8902 contains shutdown circuitry amplifier off when a logic low is placed on the ENA pin. By switching the ENA pin connected to GND, the PAM8902 supply current draw will be minimized in idle mode.

Under-Voltage Lock-Out (UVLO)

The PAM8902 incorporates circuitry designed to detect supply voltage. When the supply voltage drops to 2.2V or below, the PAM8902 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or ENA pin.

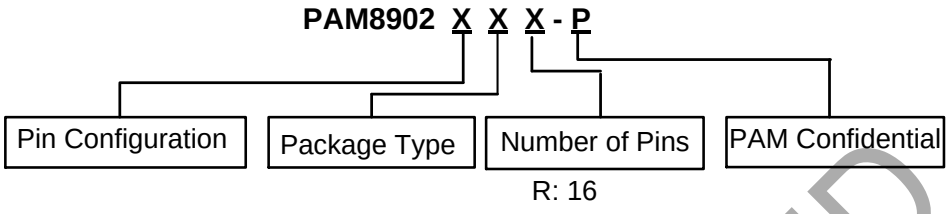
Short-Circuit Protection (SCP)

The PAM8902 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorted or output-to-GND shorted occurs. When a short circuit occurs, the device goes into a latch state and must be reset by cycling the voltage on the ENA pin to a logic low and then back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Over-Temperature Protection (OTP)

Thermal protection on the PAM8902 prevents the device from damage when the internal die temperature exceeds +150°C. There is a +15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled in this condition both OUT+ and OUT- will become high impedance. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by +30°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

Ordering Information



Part Number	Part Marking	Package Type	Standard Package
PAM8902ZER-P	BG YW	CSP-16L	3000Units/Tape&Reel
PAM8902KER-P	P8902 XXXYW	QFN4x4-16L	3000Units/Tape&Reel

Marking Information

Y: Last Digital of Manufacturing Year

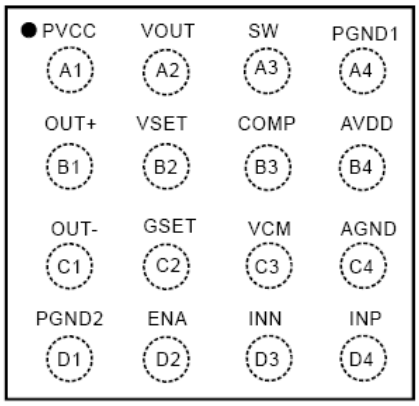
6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011

W: Week Code

Item	Week Code	Item	Week Code	Item	Week Code	Item	Week Code
1	A	14	N	27	A	40	N
2	B	15	O	28	B	41	O
3	C	16	P	29	C	42	P
4	D	17	Q	30	D	43	Q
5	E	18	R	31	E	44	R
6	F	19	S	32	F	45	S
7	G	20	T	33	G	46	T
8	H	21	U	34	H	47	U
9	I	22	V	35	I	48	V
10	J	23	W	36	J	49	W
11	K	24	X	37	K	50	X
12	L	25	Y	38	L	51	Y
13	M	26	Z	39	M	52	Z

Marking Information (cont.)

16 Ball CSP
Top View

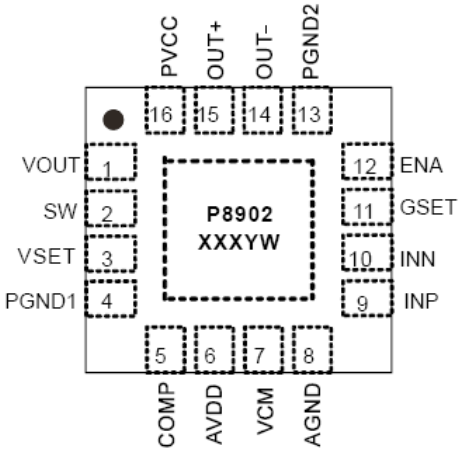


Marking

BG
YW

BG: Product Code of PAM8902
Y: Year
W: Week

Top View
QFN 4X4 16L

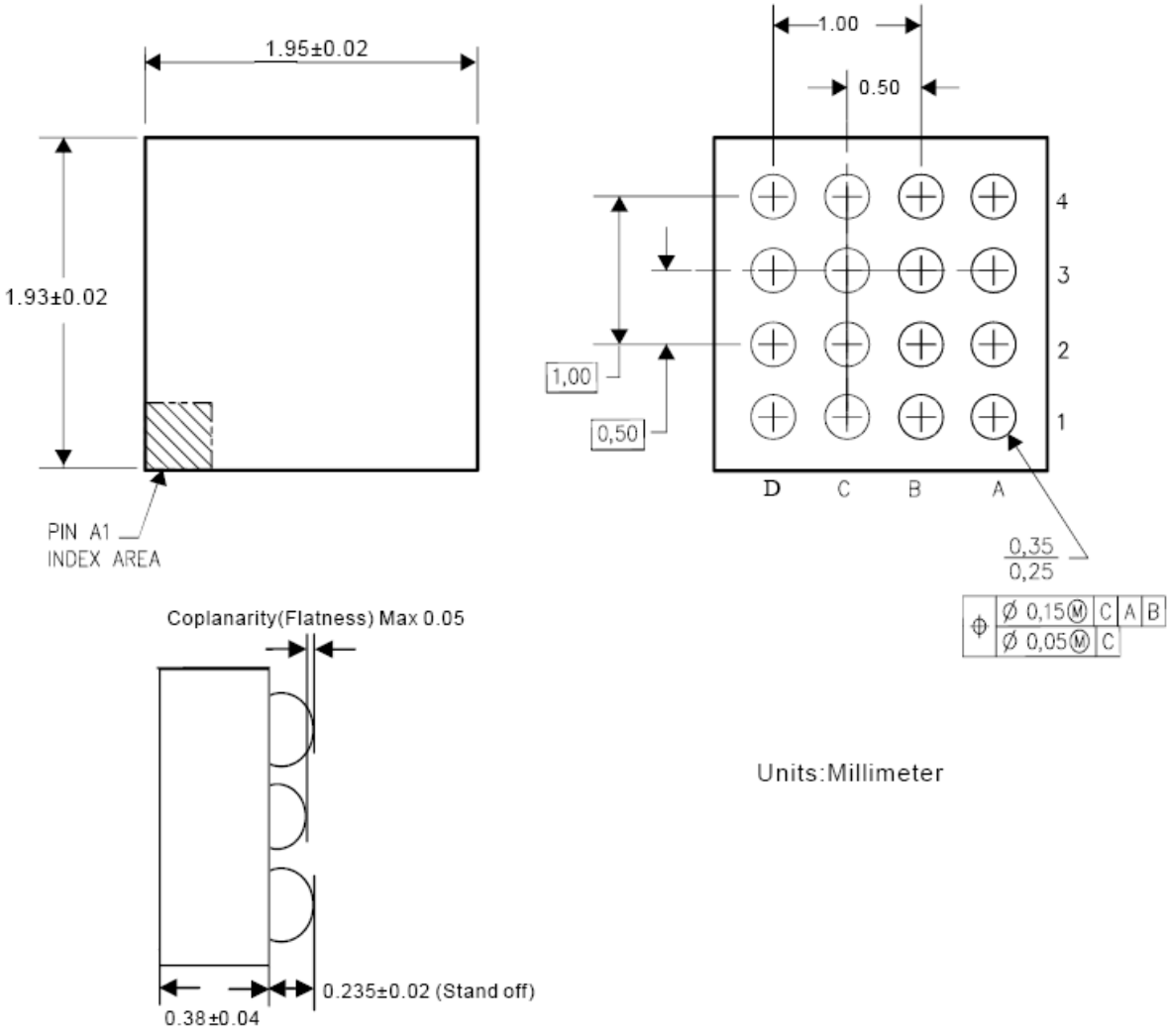


Y: Year
W: Week
X: Internal Code

●: Pin 1 Indicator

Package Outline Dimensions (All dimensions in mm.)

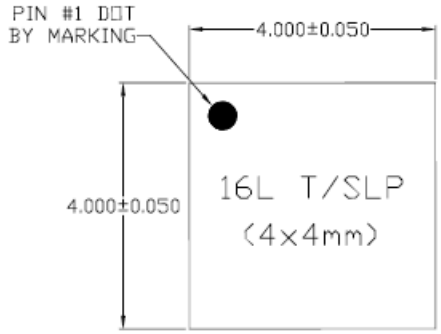
CSP-16



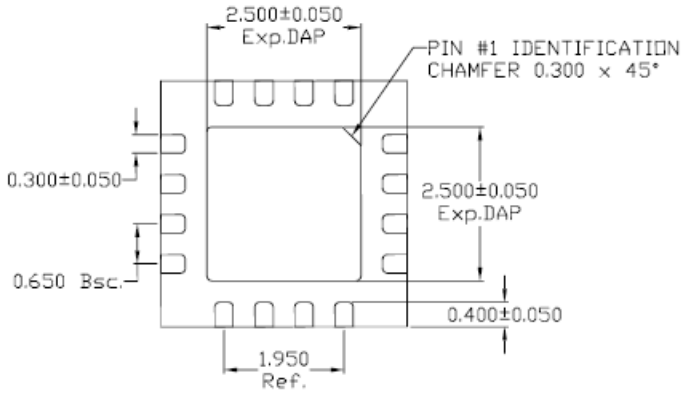
Units:Millimeter

Package Outline Dimensions (cont.) (All dimensions in mm.)

QFN4x4-16



TOP VIEW



BOTTOM VIEW

NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE
BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

SIDE VIEW

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