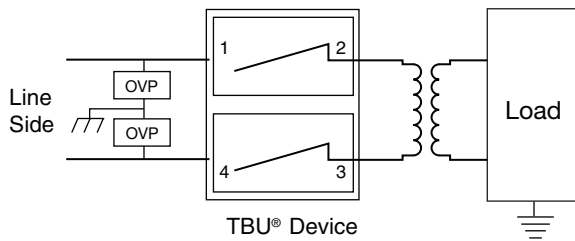


## Environmental Characteristics

Parameter	Value
Moisture Sensitivity Level	1
ESD Classification (HBM)	1B

## Reference Application

The TBU® device can be used to protect against excessive voltage surges in transformer coupled equipment, as shown in the figure below. The TBU® protector prevents any surges from causing damage. An overvoltage protection device, such as an MOV or GDT, may be used to provide additional overvoltage protection if the surge voltage is likely to be above the maximum rating of the TBU® device.



## Basic TBU Operation

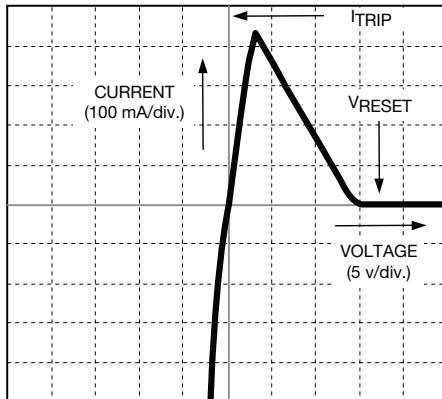
The TBU® device is a silicon-based, solid-state, resettable device which is placed in series with a signal path. The TBU® device operates in approximately 1  $\mu$ s - once line current exceeds the TBU® device's trigger current  $I_{\text{trigger}}$ . When operated, the TBU® device will limit the current to less than the  $I_{\text{trigger}}$  value within the  $t_{\text{block}}$  duration. If voltage above  $V_{\text{reset}}$  is continuously sustained, the TBU® device will subsequently reduce the current to a quiescent current level within a period of time that is dependent upon the applied voltage.

After the surge, the TBU® device resets when the voltage across the TBU® device falls to the  $V_{\text{reset}}$  level. The TBU® device will automatically reset on lines which have no DC bias or have DC bias below  $V_{\text{reset}}$  (such as unpowered signal lines).

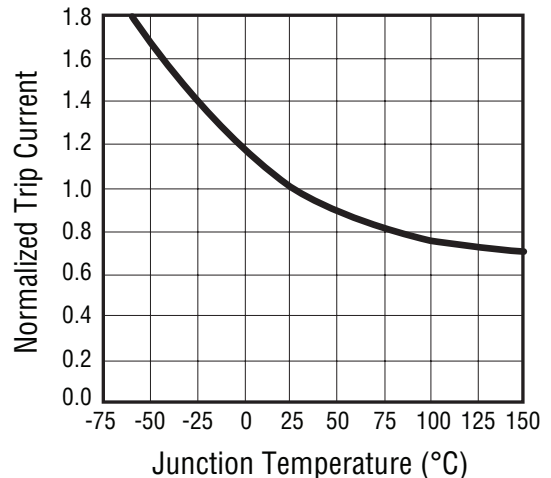
If the line has a normal DC bias above  $V_{\text{reset}}$ , the voltage across the TBU® device may not fall below  $V_{\text{reset}}$  after the surge. In such cases, special care needs to be taken to ensure that the TBU® device will reset, otherwise an automatic or manual power down will be required. Bourns application engineers can provide further assistance.

## Performance Graphs

### V-I Characteristic - TBU-DT085-300-WH (Pin 2-1 & Pin 3-4)

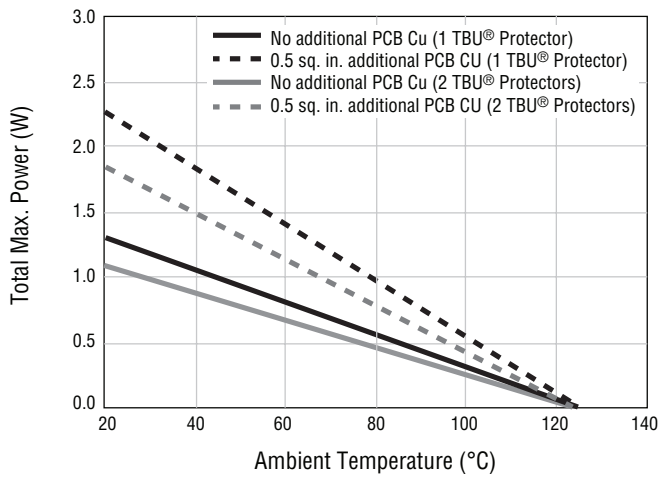


### Typical Trigger Current vs. Temperature

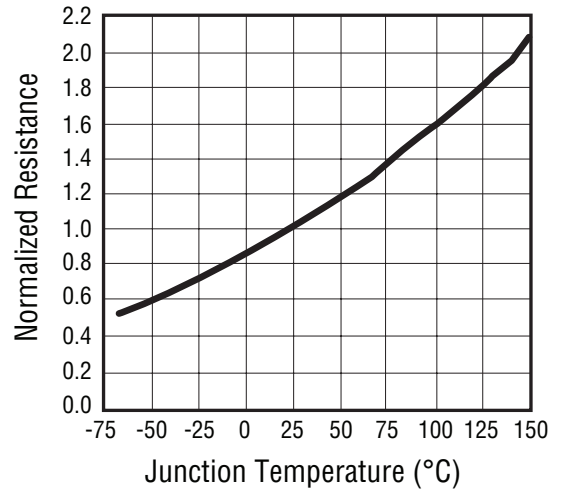


## Performance Graphs (Continued)

### Power Derating Curve

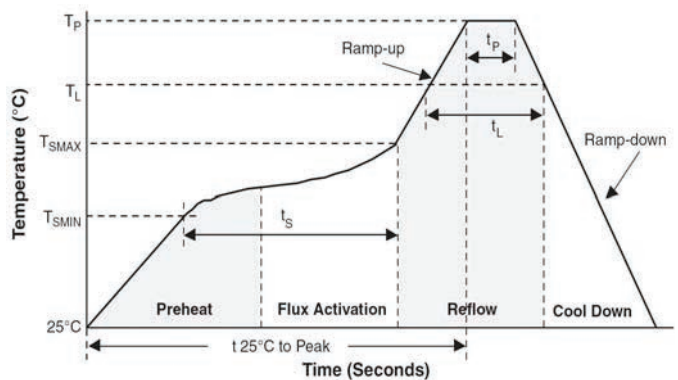


### Typical Resistance vs. Temperature



### Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (T <sub>smax</sub> to T <sub>p</sub> )	3 °C/sec. max.
Preheat	
- Temperature Min. (T <sub>smin</sub> )	150 °C
- Temperature Max. (T <sub>smax</sub> )	200 °C
- Time (t <sub>smin</sub> to t <sub>smax</sub> )	60-180 sec.
Time maintained above:	
- Temperature (T <sub>L</sub> )	217 °C
- Time (t <sub>L</sub> )	60-150 sec.
Peak/Classification Temperature (T <sub>p</sub> )	260 °C
Time within 5 °C of Actual Peak Temp. (t <sub>p</sub> )	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.

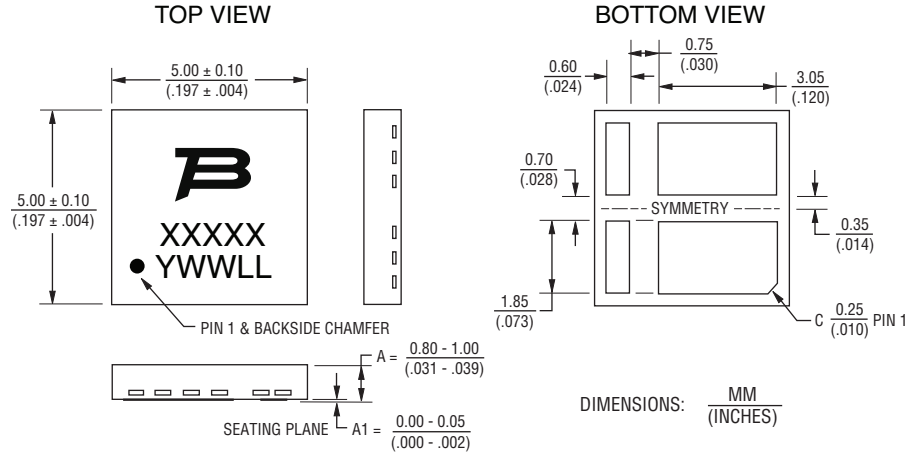


Specifications are subject to change without notice.

Users should verify actual device performance in their specific applications.

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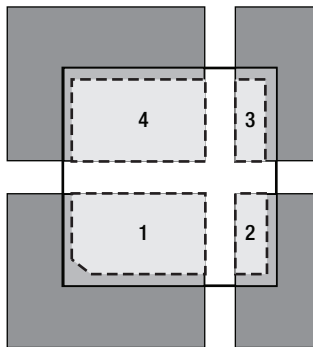
## Product Dimensions



## Recommended Pad Layout

TBU® High-Speed Protectors have a 100 % matte-tin termination finish. For improved thermal dissipation, the recommended layout uses PCB copper areas which extend beyond the exposed solder pad. The exposed solder pads should be defined by a solder mask which matches the pad layout of the TBU® device in size and spacing. It is recommended that they should be the same dimension as the TBU® pads but if smaller solder pads are used, they should be centered on the TBU® package terminal pads and not more than 0.10-0.12 mm (0.004-0.005 in.) smaller in overall width or length. Solder pad areas should not be larger than the TBU® pad sizes to ensure adequate clearance is maintained. The recommended

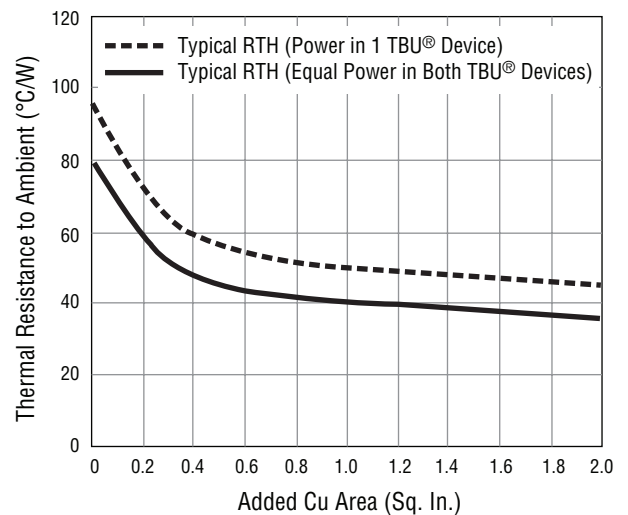
stencil thickness is 0.10-0.12 mm (0.004-0.005 in.) with a stencil opening size 0.025 mm (0.0010 in.) less than the solder pad size. Extended copper areas beyond the solder pad significantly improve the junction to ambient thermal resistance, resulting in operation at lower junction temperatures with a corresponding benefit of reliability. All pads should soldered to the PCB, including pads marked as NC or NU but no electrical connection should be made to these pads. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad.



Pad Designation	
Pad #	Pin Out
1	Line Side 1
2	Load Side 1
3	Load Side 2
4	Line Side 2

Dark grey areas show added PCB copper area for better thermal resistance.

## Thermal Resistance vs. Additional PCB Cu Area



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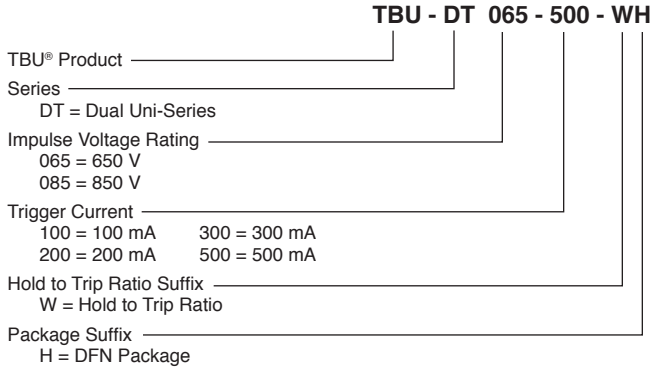
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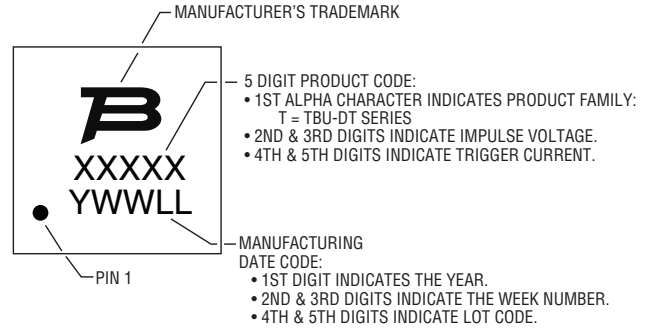
# TBU-DT Series - TBU® High-Speed Protectors

**BOURNS®**

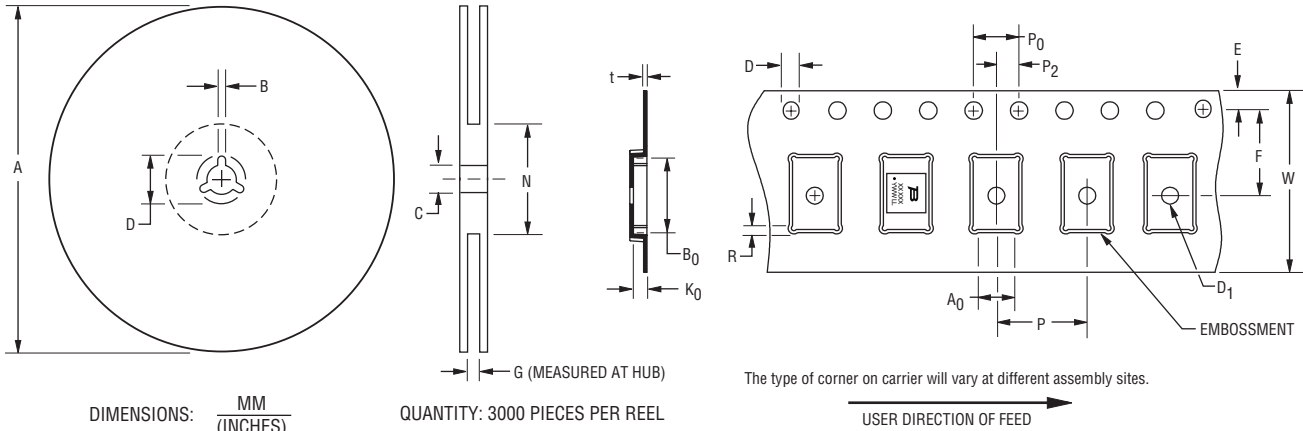
## How to Order



## Typical Part Marking



## Packaging Specifications



A		B		C		D		G	N
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
326	330	1.5	2.5	12.8	13.5	20.2	-	16.5	102
(12.835)	(13.002)	(.059)	(.098)	(.504)	(.531)	(.795)		(.650)	(4.016)

A <sub>0</sub>		B <sub>0</sub>		D		D <sub>1</sub>		E		F	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
5.15	5.35	5.15	5.35	1.5	1.6	1.5	-	1.65	1.85	5.45	5.55
(.203)	(.211)	(.203)	(.211)	(.059)	(.063)	(.059)		(.065)	(.073)	(.214)	(.218)

K <sub>0</sub>		P		P <sub>0</sub>		P <sub>2</sub>		R		t	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1.0	1.2	7.9	8.1	3.8	4.2	1.95	2.05	0	0.5	0.25	0.35
(.039)	(.047)	(.311)	(.319)	(.150)	(.165)	(.077)	(.081)	(0)	(.020)	(.010)	(.014)

W	
Min.	Max.
11.7	12.3
(.461)	(.484)

DIMENSIONS:  $\frac{\text{MM}}{\text{(INCHES)}}$

REV. 02/19

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