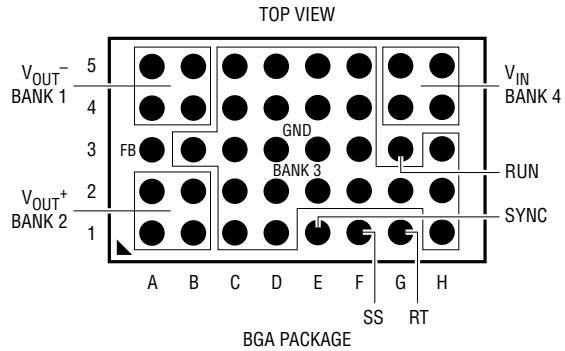
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN 20V
RT, SYNC 5V
SS, FB 2.5V
V_{OUT}^+ (V_{OUT}^- = 0V) 16V
V_{OUT}^- (V_{OUT}^+ = 0V) .....–16V
Maximum Internal Temperature ..... 125°C
Maximum Solder Temperature ..... 250°C
Storage Temperature ..... –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
40-LEAD (11.25mm × 6.25mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 28.7°C/W, θ_{JB} = 7.6°C/W,
θ_{JCtop} = 40.3°C/W, $\theta_{JCbottom}$ = 10.5°C/W
θ VALUES DETERMINED PER JEDEC 51-9, 51-12
WEIGHT = 0.9g

ORDER INFORMATION

http://www.linear.com/product/LTM8045#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM8045EY#PBF	SAC305 (RoHS)	LTM8045Y	e1	BGA	3	–40°C to 125°C
LTM8045IY#PBF	SAC305 (RoHS)	LTM8045Y	e1	BGA	3	–40°C to 125°C
LTM8045IY	SnPb (63/37)	LTM8045Y	e0	BGA	3	–40°C to 125°C
LTM8045MPY#PBF	SAC305 (RoHS)	LTM8045Y	e1	BGA	3	–55°C to 125°C
LTM8045MPY	SnPb (63/37)	LTM8045Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 12V unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input DC Voltage		●	2.8		18	V
Positive Output DC Voltage	I_{OUT} = 0.7A, R_{FB} = 15.4kΩ, V_{OUT}^- Grounded I_{OUT} = 0.375A, R_{FB} =165kΩ, V_{OUT}^- Grounded			2.5 15		V V
Negative Output DC Voltage	I_{OUT} = 0.7A, R_{FB} = 30.0kΩ, V_{OUT}^+ Grounded I_{OUT} = 0.375A, R_{FB} =178kΩ, V_{OUT}^+ Grounded			–2.5 –15		V V
Continuous Output DC Current	V_{IN} = 12V, V_{OUT} = 2.5V or –2.5V V_{IN} = 12V, V_{OUT} = 15V or –15V				0.7 0.375	A A
V_{IN} Quiescent Current	V_{RUN} = 0V Not Switching			0 10	1	µA mA
Line Regulation	4V ≤ V_{IN} ≤ 18V, I_{OUT} = 0.2A			0.6		%
Load Regulation	0.01A ≤ I_{OUT} ≤ 0.58A			0.2		%
Output RMS Voltage Ripple	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 580mA, 100kHz to 4MHz			4		mV
Input Short-Circuit Current	V_{OUT}^+ = V_{OUT}^- = 0V, V_{IN} = 12V			200		mA
Switching Frequency	R_T = 45.3k R_T = 464k	● ●	1800 180	2000 200	2200 220	kHz kHz
Voltage at FB Pin (Positive Output) Voltage at FB Pin (Negative Output)		● ●	1.195 0	1.215 5	1.235 12	V mV
Current into FB Pin (Positive Output) Current into FB Pin (Negative Output)		● ●	81 81	83.3 83.3	86 86.5	µA µA
RUN Pin Threshold Voltage	RUN Pin Rising RUN Pin Falling		 1.235	1.32 1.29	1.385	V V
RUN Pin Current	V_{RUN} = 3V V_{RUN} = 1.3V V_{RUN} = 0V		 9.7	40 11.6 0	60 13.4 0.1	µA µA µA
SS Sourcing Current	SS = 0V		5	8	13	µA
Synchronization Frequency Range			200		2000	kHz
Synchronization Duty Cycle			35		65	%
SYNC Input Low Threshold			0.4			V
SYNC Input High Threshold					1.3	V

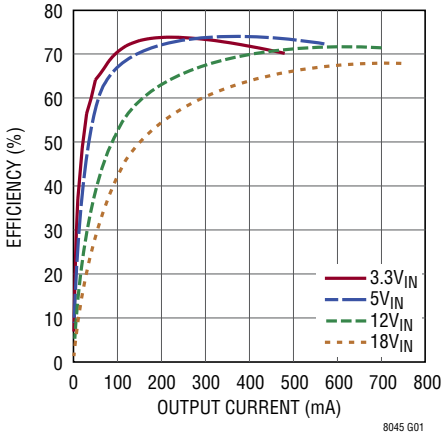
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8045E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8045I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8045MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

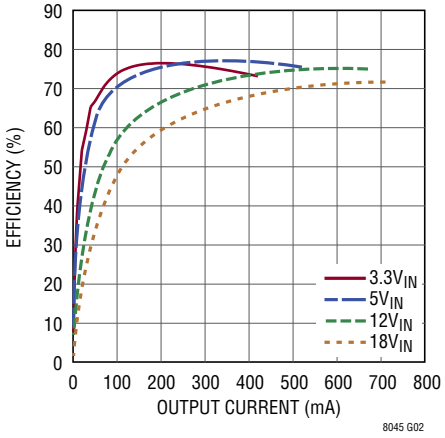
Note 3: This µModule converter includes overtemperature protection that is intended to protect the device during momentary overload conditions. Internal temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum internal operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

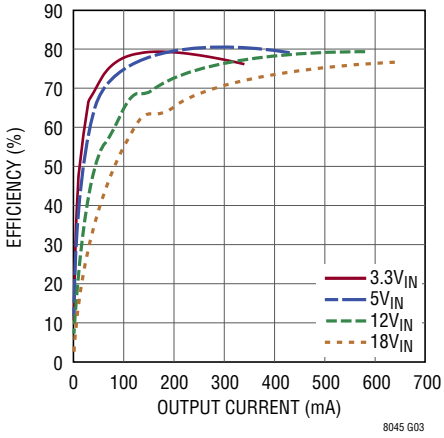
Efficiency
2.5V_{OUT} SEPIC



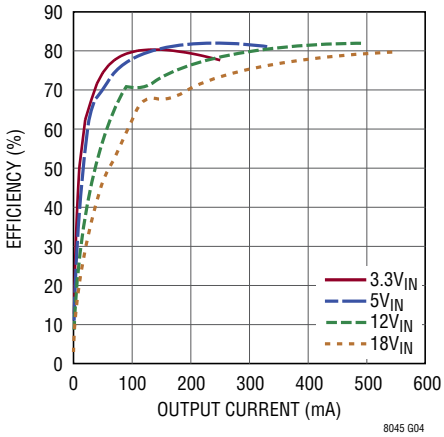
Efficiency
3.3V_{OUT} SEPIC



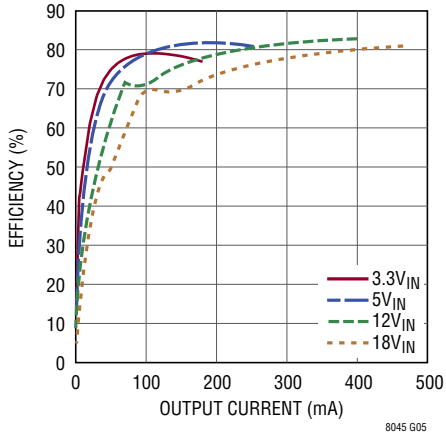
Efficiency
5V_{OUT} SEPIC



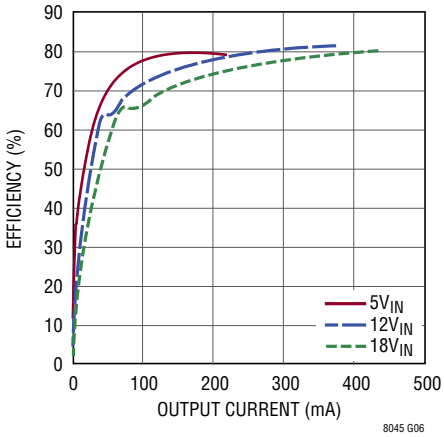
Efficiency
8V_{OUT} SEPIC



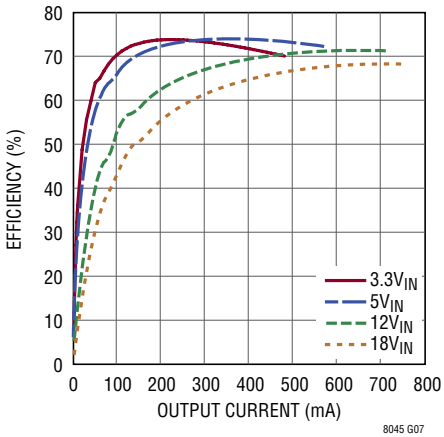
Efficiency
12V_{OUT} SEPIC



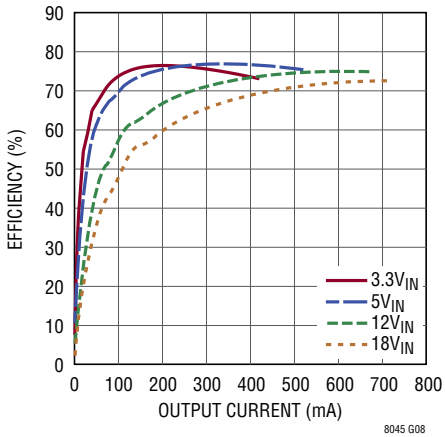
Efficiency
15V_{OUT} SEPIC



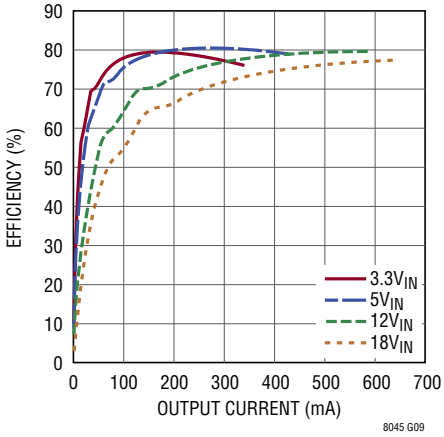
Efficiency
–2.5V_{OUT} Inverting Converter



Efficiency
–3.3V_{OUT} Inverting Converter

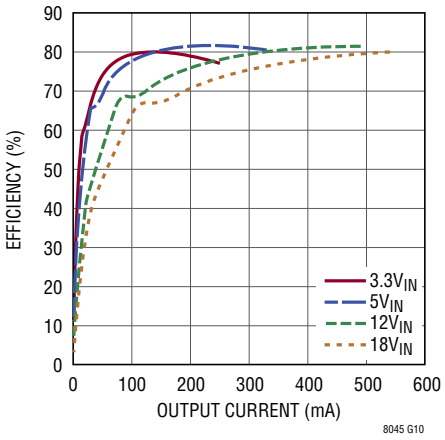


Efficiency
–5V_{OUT} Inverting Converter

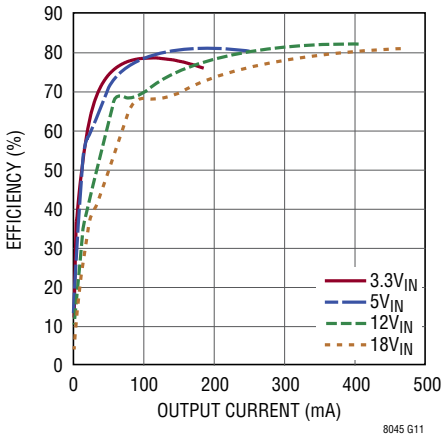


TYPICAL PERFORMANCE CHARACTERISTICS

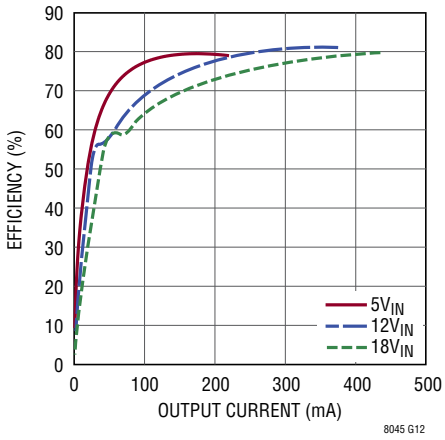
Efficiency
–8V_{OUT} Inverting Converter



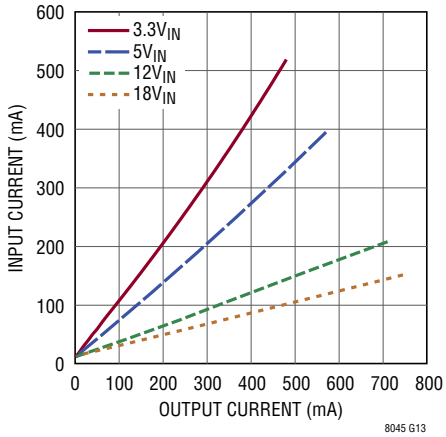
Efficiency
–12V_{OUT} Inverting Converter



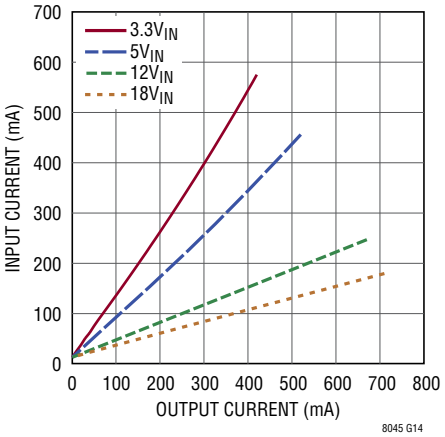
Efficiency
–15V_{OUT} Inverting Converter



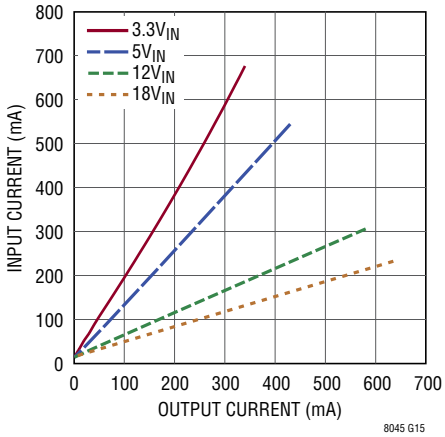
Input Current vs Output Current,
2.5V_{OUT} SEPIC



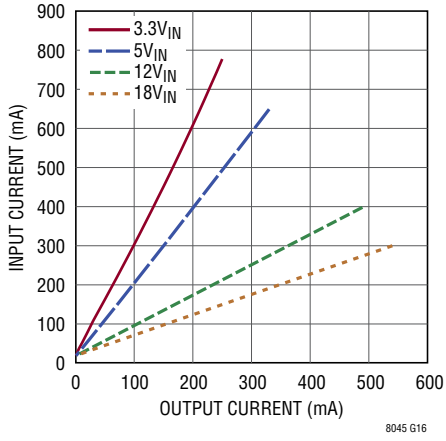
Input Current vs Output Current,
3.3V_{OUT} SEPIC



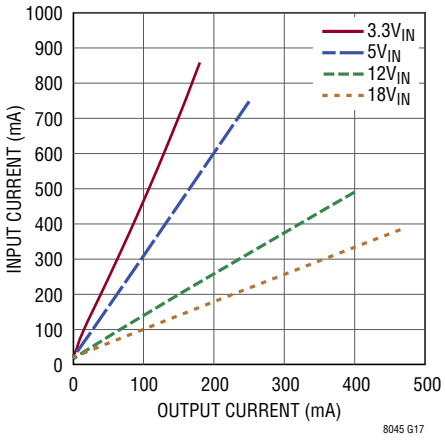
Input Current vs Output Current,
5V_{OUT} SEPIC



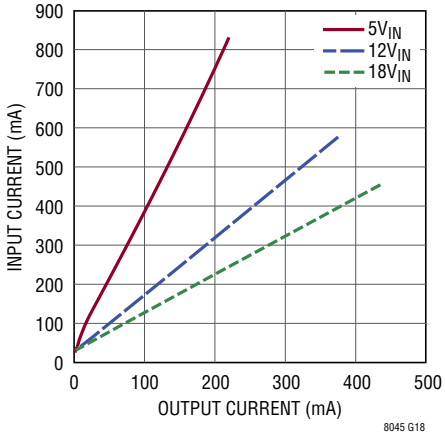
Input Current vs Output Current,
8V_{OUT} SEPIC



Input Current vs Output Current,
12V_{OUT} SEPIC

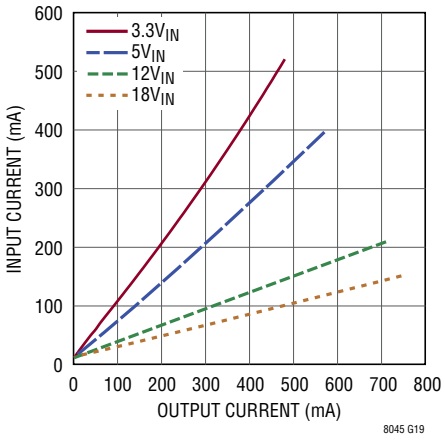


Input Current vs Output Current,
15V_{OUT} SEPIC

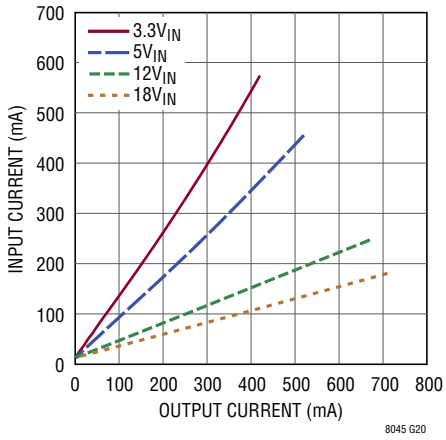


TYPICAL PERFORMANCE CHARACTERISTICS

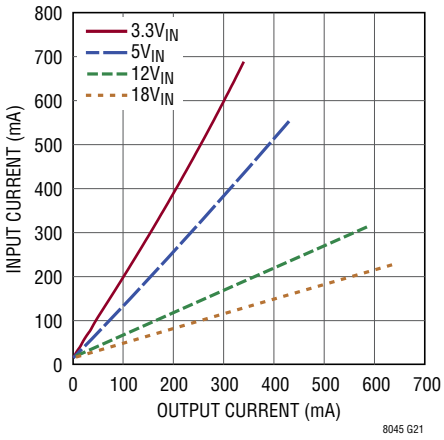
Input Current vs Output Current, –2.5V_{OUT} Inverting Converter



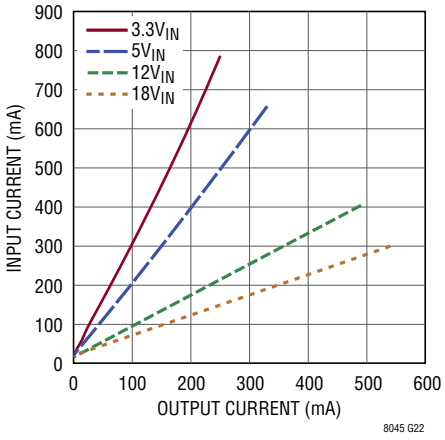
Input Current vs Output Current, –3.3V_{OUT} Inverting Converter



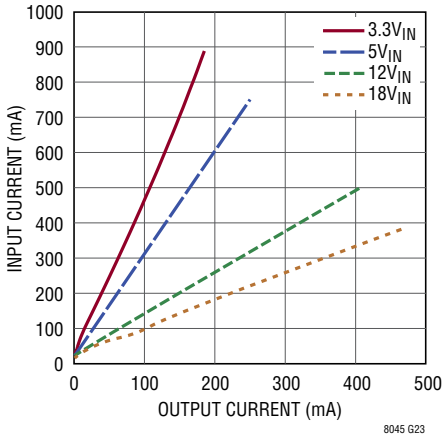
Input Current vs Output Current, –5V_{OUT} Inverting Converter



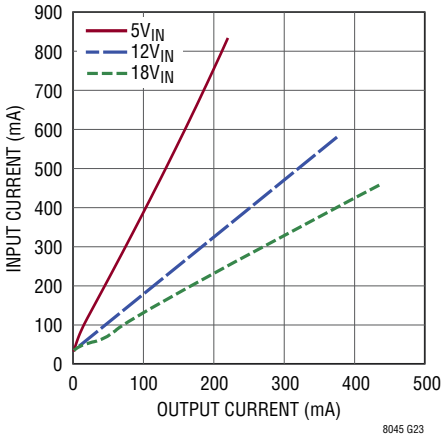
Input Current vs Output Current, –8V_{OUT} Inverting Converter



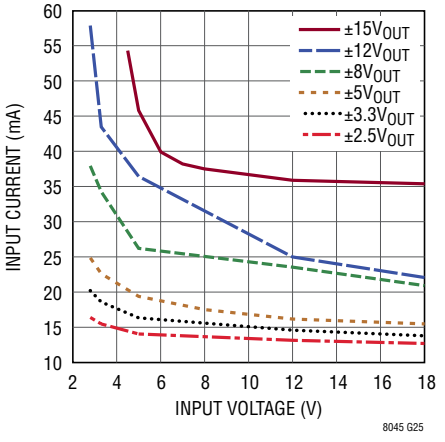
Input Current vs Output Current, –12V_{OUT} Inverting Converter



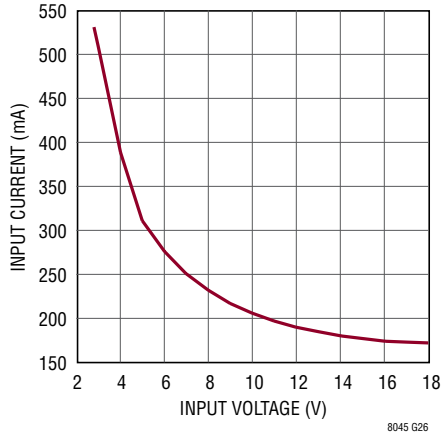
Input Current vs Output Current, –15V_{OUT} Inverting Converter



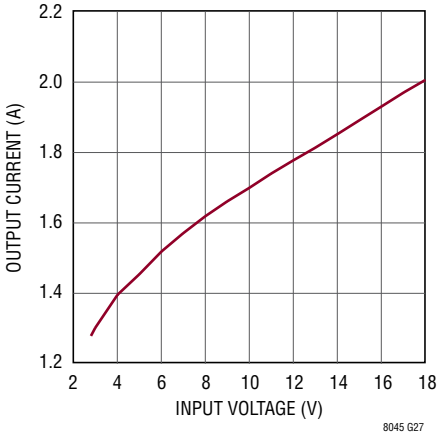
Input Current vs Input Voltage, 5mA Load



Input Current vs Input Voltage, Output Shorted

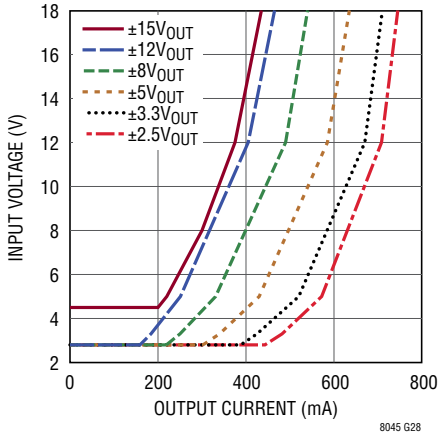


Output Current vs Input Voltage, Output Shorted

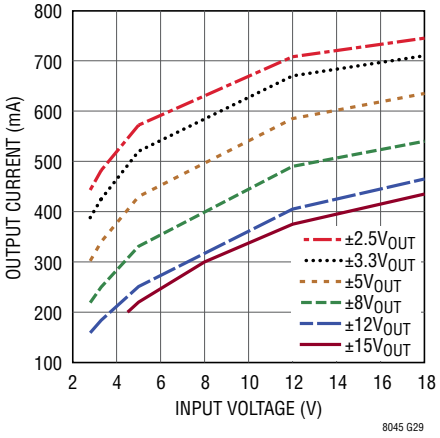


TYPICAL PERFORMANCE CHARACTERISTICS

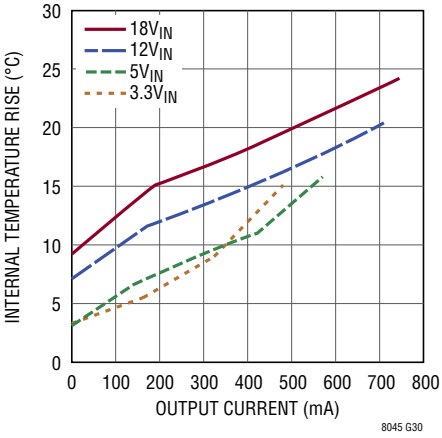
Minimum Required Input Voltage vs Output Current



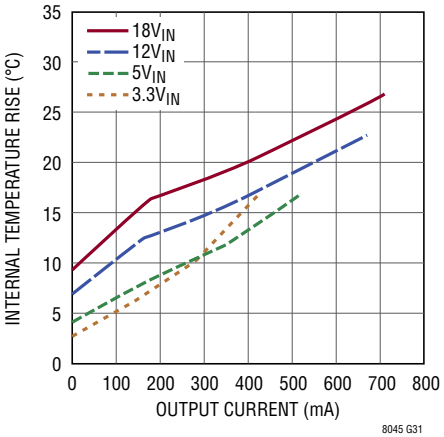
Maximum Output Current vs Input Voltage



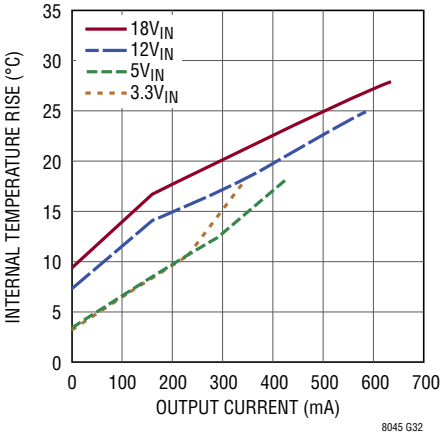
Internal Temperature Rise vs Output Current, 2.5V_{OUT} SEPIC



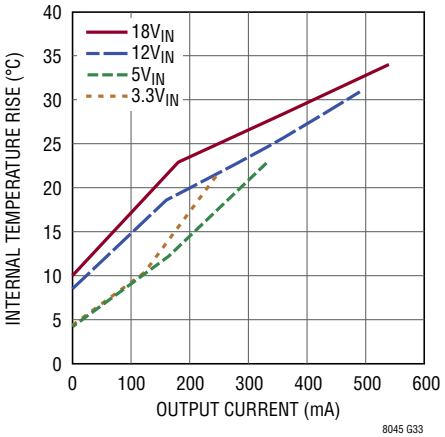
Internal Temperature Rise vs Output Current, 3.3V_{OUT} SEPIC



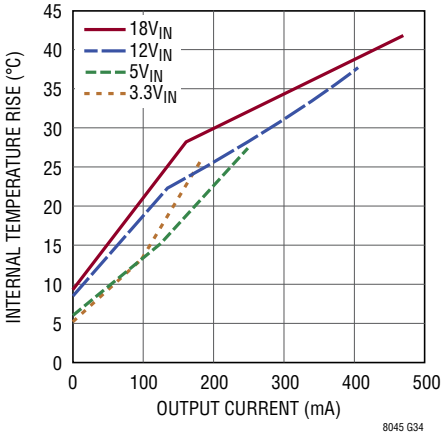
Internal Temperature Rise vs Output Current, 5V_{OUT} SEPIC



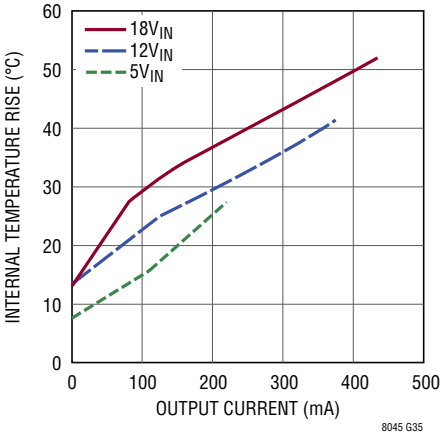
Internal Temperature Rise vs Output Current, 8V_{OUT} SEPIC



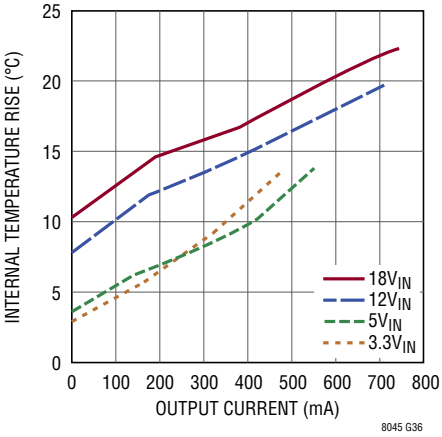
Internal Temperature Rise vs Output Current, 12V_{OUT} SEPIC



Internal Temperature Rise vs Output Current, 15V_{OUT} SEPIC

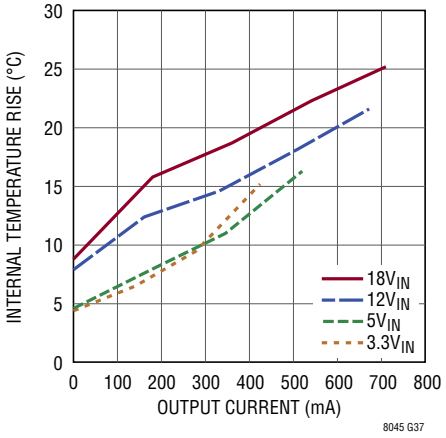


Internal Temperature Rise vs Output Current, –2.5V_{OUT} Inverting Converter

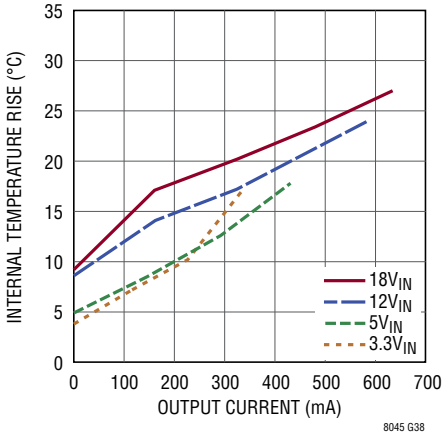


TYPICAL PERFORMANCE CHARACTERISTICS

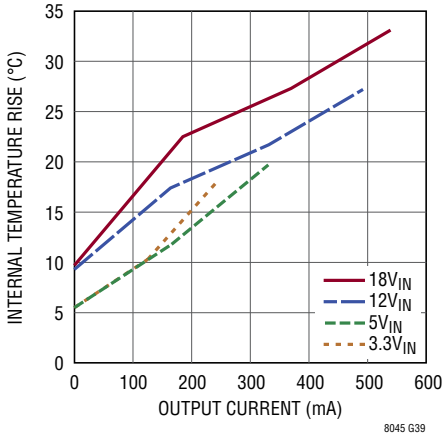
Internal Temperature Rise vs Output Current, –3.3V_{OUT} Inverting Converter



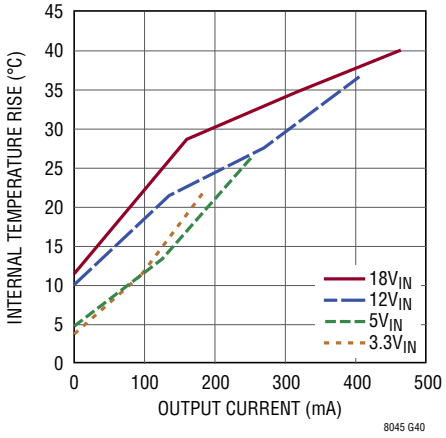
Internal Temperature Rise vs Output Current, –5V_{OUT} Inverting Converter



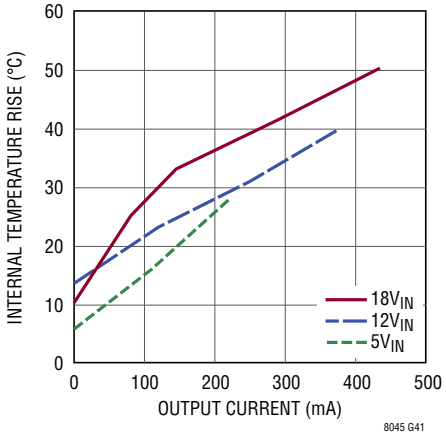
Internal Temperature Rise vs Output Current, –8V_{OUT} Inverting Converter



Internal Temperature Rise vs Output Current, –12V_{OUT} Inverting Converter



Internal Temperature Rise vs Output Current, –15V_{OUT} Inverting Converter



PIN FUNCTIONS

V_{OUT}^- (Bank 1): V_{OUT}^- is the negative output of the LTM8045. Apply an external capacitor between V_{OUT}^+ and V_{OUT}^-. Tie this net to GND to configure the LTM8045 as a positive output SEPIC regulator.

V_{OUT}^+ (Bank 2): V_{OUT}^+ is the positive output of the LTM8045. Apply an external capacitor between V_{OUT}^+ and V_{OUT}^-. Tie this net to GND to configure the LTM8045 as a negative output inverting regulator.

GND (Bank 3): Tie these GND pins to a local ground plane below the LTM8045 and the circuit components. GND MUST BE CONNECTED EITHER TO V_{OUT}^+ OR V_{OUT}^- FOR PROPER OPERATION. In most applications, the bulk of the heat flow out of the LTM8045 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{FB}) to this net.

V_{IN} (Bank 4): The V_{IN} pin supplies current to the LTM8045's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor.

FB (Pin A3): If configured as a SEPIC, the LTM8045 regulates its FB pin to 1.215V. Apply a resistor between FB and V_{OUT}^+. Its value should be $R_{FB} = [(V_{OUT} - 1.215)/0.0833]k\Omega$. If the LTM8045 is configured as an inverting converter, the LTM8045 regulates the FB pin to 5mV. Apply a resistor between FB and V_{OUT}^- of value $R_{FB} = [(|V_{OUT}| + 0.005)/0.0833]k\Omega$.

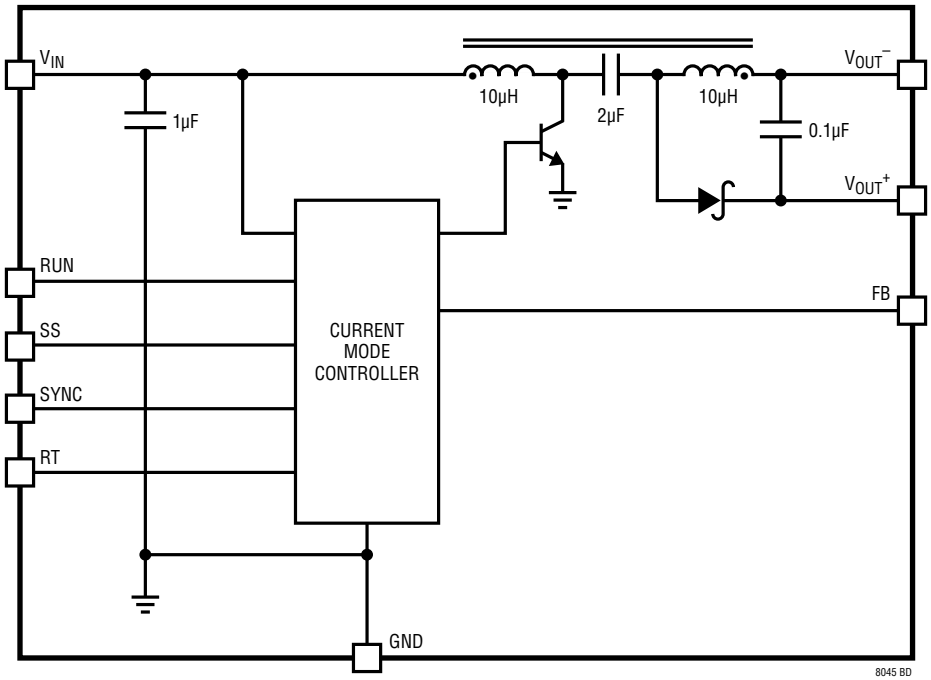
SYNC (Pin E1): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. Ground this pin if the SYNC function is not used. See the Applications Information section for more information.

SS (Pin F1): Place a soft-start capacitor here. Upon start-up, the SS pin will be charged by a (nominally) 275k resistor to about 2.2V.

RT (Pin G1): The RT pin is used to program the switching frequency of the LTM8045 by connecting a resistor from this pin to ground. The necessary resistor value for the LTM8045 is determined by the equation $R_T = (91.9/f_{OSC}) - 1$, where f_{OSC} is the typical switching frequency in MHz and R_T is in $k\Omega$. Do not leave this pin open.

RUN (Pin G3): This pin is used to enable/disable the chip and restart the soft-start sequence. Drive below 1.235V to disable the chip. Drive above 1.385V to activate chip and restart the soft-start sequence. Do not float this pin.

BLOCK DIAGRAM



OPERATION

The LTM8045 is a stand-alone switching DC/DC converter that may be configured either as a SEPIC (single-ended primary inductance converter) or inverting power supply simply by tying V_{OUT}^- or V_{OUT}^+ to GND, respectively. It accepts an input voltage up to 18VDC. The output is adjustable between 2.5V and 15V for the SEPIC, and between –2.5V and –15V for the inverting configuration. The LTM8045 can provide 700mA at V_{IN} = 12V when V_{OUT} = 2.5V or –2.5V.

As shown in the Block Diagram, the LTM8045 contains a current mode controller, power switching element, power coupled inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8045 is a fixed frequency PWM converter.

The LTM8045 switching can free run by applying a resistor to the RT pin or synchronize to an external source at a frequency between 200kHz and 2MHz. To synchronize to an external source, drive a valid signal source into the SYNC pin. An R_T resistor is required whether or not a SYNC signal is applied. See the Applications Information section for more details.

The LTM8045 also features RUN and SS pins to control the start-up behavior of the device. The RUN pin may also be used to implement an accurate undervoltage lockout function by applying just one or two resistors.

The LTM8045 is equipped with a thermal shutdown to protect the device during momentary overload conditions. It is set above the 125°C absolute maximum internal temperature rating to avoid interfering with normal specified operation, so internal device temperatures will exceed the absolute maximum rating when the overtemperature protection is active. Therefore, continuous or repeated activation of the thermal shutdown may impair device reliability.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{FB} and R_T values.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitudes, polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8045 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column.

Table 1. Recommended Component Values and Configuration
(T_A = 25°C. See the Typical Performance Characteristics for Load Conditions)

SEPIC Topology

V_{IN} (V)	V_{OUT} (V)	C_{IN}	C_{OUT}	R_{FB} (k)	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$ (k)	f_{MAX} (MHz)	$R_{T(MIN)}$ (k)
2.8 to 18	2.5	4.7µF, 25V, 1206	100µF, 6.3V, 1210	15.4	600kHz	154	1.3	69.8
2.8 to 18	3.3	4.7µF, 25V, 1206	100µF, 6.3V, 1210	24.9	700kHz	130	1.5	60.4
2.8 to 18	5	4.7µF, 25V, 1206	100µF, 6.3V, 1210	45.3	800kHz	115	2	45.3
2.8 to 18	8	4.7µF, 25V, 1206	47µF, 10V, 1210	80.6	1MHz	90.9	2	45.3
2.8 to 18	12	4.7µF, 25V, 1206	22µF, 16V, 1210	130	1.2MHz	75.0	2	45.3
4.5 to 18	15	4.7µF, 25V, 1206	22µF, 25V, 1210	165	1.5MHz	60.4	2	45.3

Inverting Topology

V_{IN} (V)	V_{OUT} (V)	C_{IN}	C_{OUT}	R_{FB} (k)	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$ (k)	f_{MAX} (MHz)	$R_{T(MIN)}$ (k)
2.8 to 18	–2.5	4.7µF, 25V, 0805	47µF, 6.3V, 1206	30.1	600kHz	154	1.3	69.8
2.8 to 18	–3.3	4.7µF, 25V, 0805	47µF, 6.3V, 1206	39.2	650kHz	140	1.5	60.4
2.8 to 18	–5	4.7µF, 25V, 0805	22µF, 6.3V, 1206	60.4	700kHz	130	2	45.3
2.8 to 18	–8	4.7µF, 25V, 1206	22µF, 10V, 1206	95.3	1MHz	90.9	2	45.3
2.8 to 18	–12	4.7µF, 25V, 1206	10µF, 16V, 1206	143	1.2MHz	75.0	2	45.3
4.5 to 18	–15	4.7µF, 25V, 1206	4.7µF, 25V, 1206	178	1.5MHz	60.4	2	45.3

APPLICATIONS INFORMATION

Setting Output Voltage

The output voltage is set by connecting a resistor (R_{FB}) from V_{OUT}^+ to the FB pin for a SEPIC and from V_{OUT}^- to the FB pin for an inverting converter. R_{FB} is determined from the equation $R_{FB} = [(V_{OUT} – 1.215)/0.0833]k\Omega$ for a SEPIC and from $R_{FB} = [(|V_{OUT}| + 0.005)/0.0833]k\Omega$ for an inverting converter.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8045. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8045 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Programming Switching Frequency

The LTM8045 has an operational switching frequency range between 200kHz and 2MHz. The free running frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any circumstance.

When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by the resistor from RT to ground. The R_T value is calculated by the following equation:

$$R_T = \frac{91.9}{f_{OSC}} - 1$$

where f_{OSC} is the typical switching frequency in MHz and R_T is in $k\Omega$.

Switching Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the corresponding input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8045 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8045 in some fault conditions. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Switching Frequency Synchronization

The switching frequency can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal at the SYNC pin. Switching will occur at the SYNC clock frequency. Drive SYNC low and the switching frequency will revert to the internal free-running oscillator after a few clock periods.

Switching will stop if SYNC is driven high.

The duty cycle of SYNC must be between 35% and 65% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 200kHz to 2MHz unless it is stopped low to enable the free-running oscillator.
2. The SYNC frequency can always be higher than the free-running oscillator frequency, f_{OSC}, but should not be less than 25% below f_{OSC} (f_{OSC} is set by R_T).

APPLICATIONS INFORMATION

Soft-Start

The LTM8045 soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor connected from the SS pin to GND programs the slew rate. In the event of a commanded shutdown or lockout (RUN pin), internal undervoltage lockout or a thermal shutdown, the soft-start capacitor is automatically discharged before charging resumes, thus assuring that the soft-start occurs when the LTM8045 restarts. The soft-start time is given by the equation:

$t_{SS} = C_{SS}/5.45,$

where C_{SS} is in µF and t_{SS} is in seconds.

Configurable Undervoltage Lockout

Figure 1 shows how to configure an undervoltage lockout (UVLO) for the LTM8045. Typically, UVLO is used in situations where the input supply is current-limited, has a relatively high source resistance, or ramps up/down slowly. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current-limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

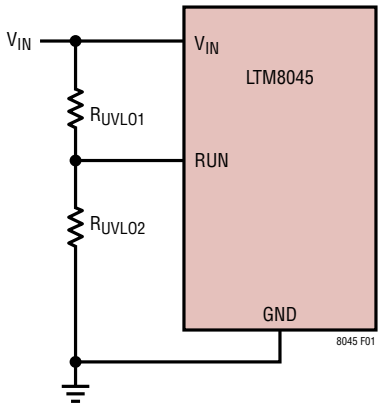


Figure 1. The RUN Pin May Be Used to Implement an Accurate UVLO

The RUN pin has a voltage hysteresis with typical thresholds of 1.32V (rising) and 1.29V (falling) and an internal circuit that draws typically 11.6µA at the RUN threshold. This makes R_{UVLO2} optional, allowing UVLO implementation with a single resistor. Resistor R_{UVLO2} is optional. R_{UVLO2} can be included to reduce the overall UVLO voltage variation caused by variations in the RUN pin current (see the Electrical Characteristics section). A good choice for R_{UVLO2} is ≤10k ±1%. After choosing a value for R_{UVLO2}, R_{UVLO1} can be determined from either of the following:

$$R_{UVLO1} = \frac{V_{IN(RISING)} - 1.32V}{\frac{1.32V}{R_{UVLO2}} + 11.6\mu A}$$

or

$$R_{UVLO1} = \frac{V_{IN(FALLING)} - 1.29V}{\frac{1.29V}{R_{UVLO2}} + 11.6\mu A}$$

where $V_{IN(RISING)}$ and $V_{IN(FALLING)}$ are the V_{IN} threshold voltages when rising or falling, respectively.

For example, to disable the LTM8045 for V_{IN} voltages below 3.5V using the single resistor configuration, choose:

$$R_{UVLO1} = \frac{3.5V - 1.29V}{\frac{1.29V}{\infty} + 11.6\mu A} = 191k$$

To activate the LTM8045 for V_{IN} voltage greater than 4.5V using the two resistor configuration, choose R_{UVLO2} = 10k and:

$$R_{UVLO1} = \frac{4.5V - 1.32V}{\frac{1.32V}{10k} + 11.6\mu A} = 22.1k$$

Internal Undervoltage Lockout

The LTM8045 monitors the V_{IN} supply voltage in case V_{IN} drops below a minimum operating level (typically about 2.3V). When V_{IN} is detected low, the power switch is deactivated, and while sufficient V_{IN} voltage persists, the soft-start capacitor is discharged. After V_{IN} is detected high, the LTM8045 will reactivate and the soft-start capacitor will begin charging.

APPLICATIONS INFORMATION

Thermal Shutdown

If the part is too hot, the LTM8045 engages its thermal shutdown, terminates switching and discharges the soft-start capacitor. When the part has cooled, the part automatically restarts. This thermal shutdown is set to engage at temperatures above the 125°C absolute maximum internal operating rating to ensure that it does not interfere with functionality in the specified operating range. This means that internal temperatures will exceed the 125°C absolute maximum rating when the overtemperature protection is active, possibly impairing the device's reliability.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8045. The LTM8045 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 2 for the suggested layout of the inverting topology application and Figure 3 for the suggested layout of the SEPIC topology application. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8045.
3. Place the Cout capacitor as close as possible to the V_{OUT}^+ and V_{OUT}^- connections of the LTM8045.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the LTM8045.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8045.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figures 2 and 3. The LTM8045 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

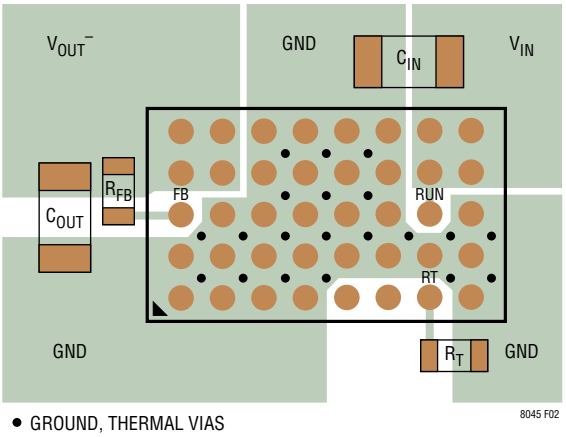


Figure 2. Layout Showing Suggested External Components, GND Plane and Thermal Vias for the Inverting Topology Application

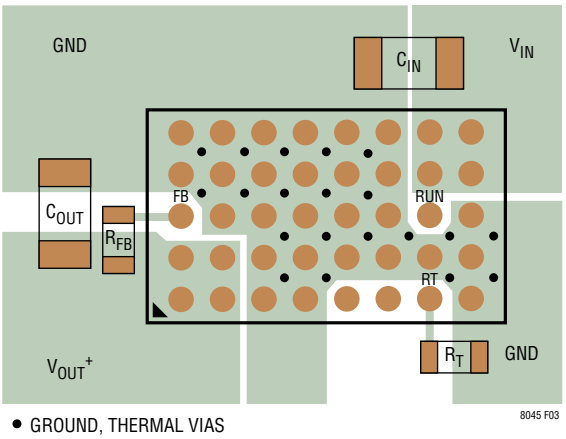


Figure 3. Layout Showing Suggested External Components, GND Plane and Thermal Vias for the SEPIC Topology Application

APPLICATIONS INFORMATION

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM8045. However, these capacitors can cause problems if the LTM8045 is plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8045 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8045's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8045 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series with V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

Thermal Considerations

The LTM8045 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8045 mounted to a 25.8cm^2 4-layer FR4 printed circuit board with a copper thickness of 2oz for the top and bottom layer and 1oz for the inner layers. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in the Pin Configuration section of the data sheet are based on modeling the µModule package mounted on a test board specified per JESD 51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The thermal coefficients provided in this page are based on JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration section of the data sheet typically gives four thermal coefficients:

- θ_{JA} – Thermal resistance from junction to ambient
- $\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case
- θ_{JCtop} – Thermal resistance from junction to top of the product case
- θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

- θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
- $\theta_{JCbottom}$ is the thermal resistance between the junction and bottom of the package with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

APPLICATIONS INFORMATION

- θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two-sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 4.

The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8045 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8045. The bulk of the heat flow out of the LTM8045 is through the bottom of the µModule converter and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

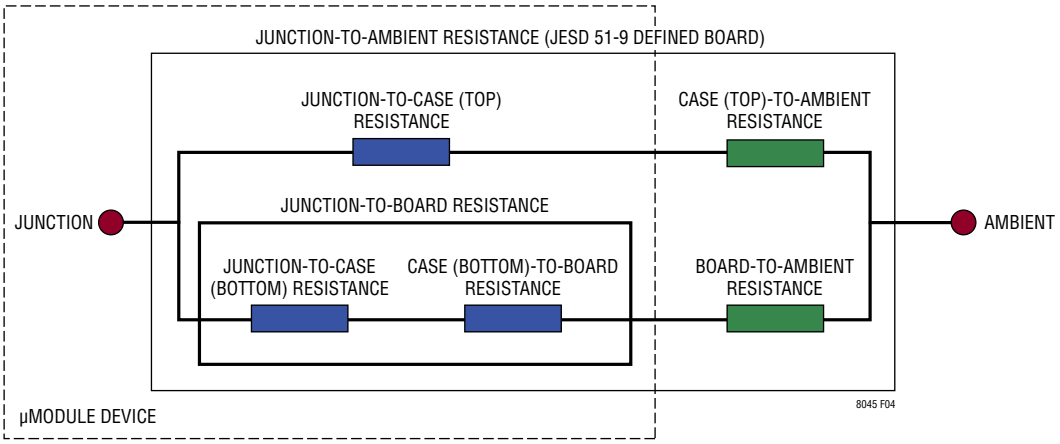
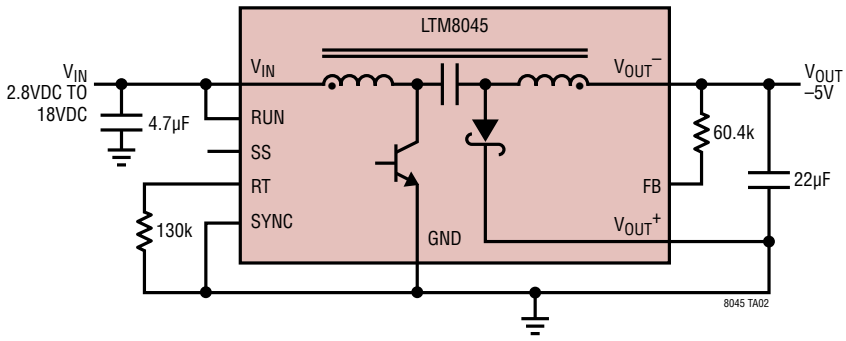


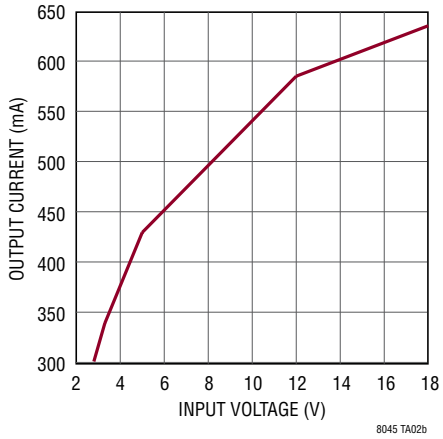
Figure 4.

TYPICAL APPLICATIONS

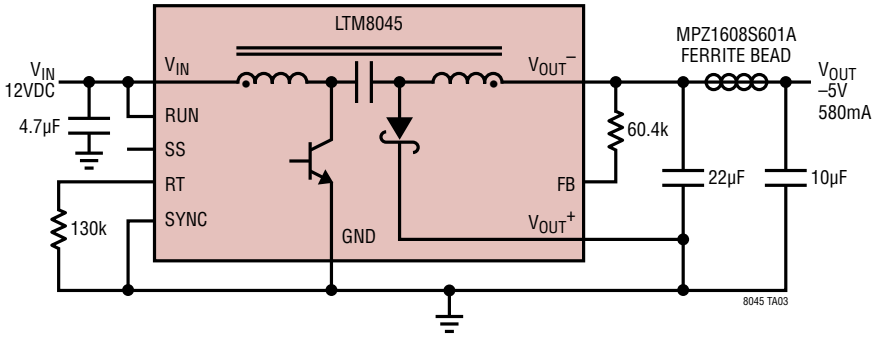
–5V Inverting Converter



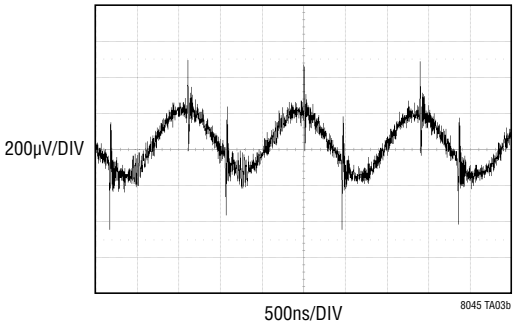
Maximum Output Current vs Input Voltage –5V$_{OUT}$ Inverting Converter



–5V Inverting Converter with Added Output Filter

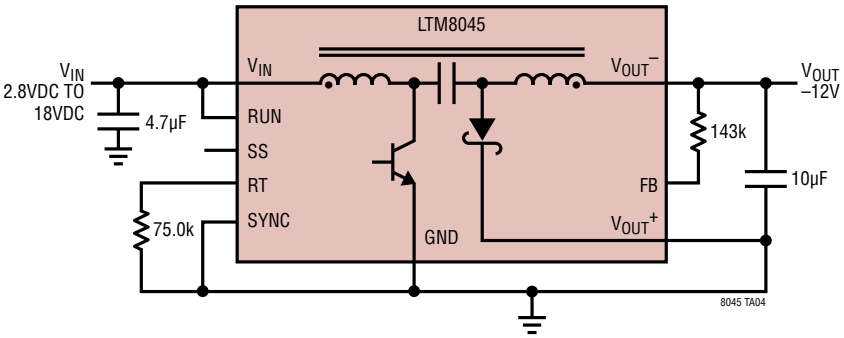


Output Ripple and Noise



MEASURED PER AN70,
USING HP461A AMPLIFIER,
150MHz BW

–12V Inverting Converter

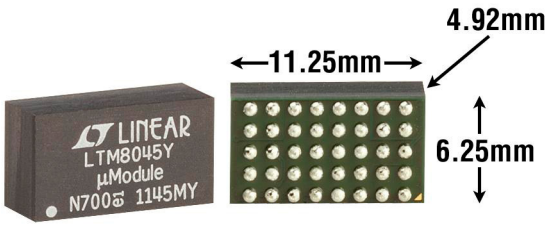


PACKAGE DESCRIPTION

Table 2. Pin Assignment Table (Arranged by Pin Number)

PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION
A1	V_{OUT}^+	B1	V_{OUT}^+	C1	GND	D1	GND
A2	V_{OUT}^+	B2	V_{OUT}^+	C2	GND	D2	GND
A3	FB	B3	GND	C3	GND	D3	GND
A4	V_{OUT}^-	B4	V_{OUT}^-	C4	GND	D4	GND
A5	V_{OUT}^-	B5	V_{OUT}^-	C5	GND	D5	GND
E1	SYNC	F1	SS	G1	RT	H1	GND
E2	GND	F2	GND	G2	GND	H2	GND
E3	GND	F3	GND	G3	RUN	H3	GND
E4	GND	F4	GND	G4	V_{IN}	H4	V_{IN}
E5	GND	F5	GND	G5	V_{IN}	H5	V_{IN}

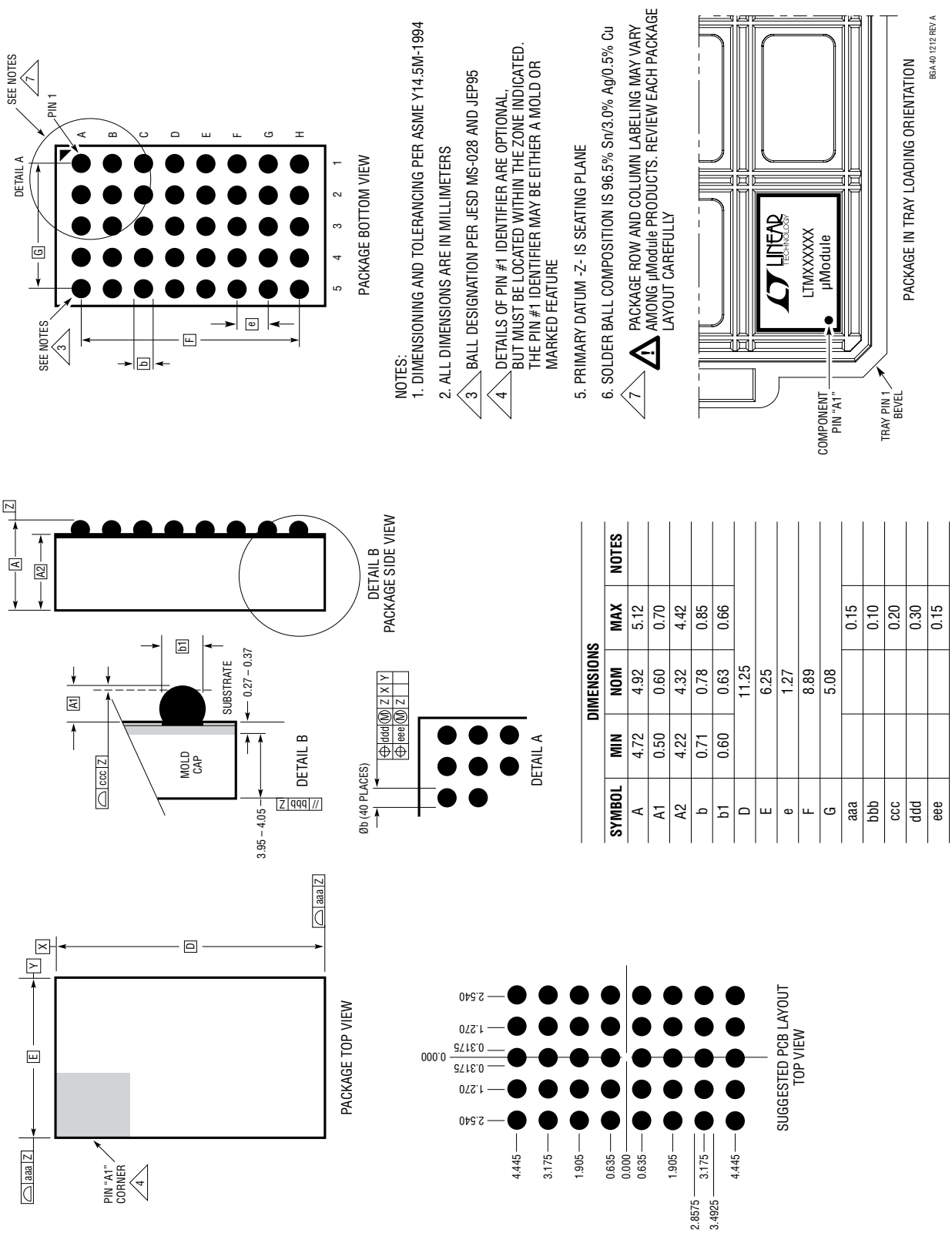
PACKAGE PHOTO



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM8045#packaging for the most recent package drawings.

BGA Package
40-Lead (11.25mm × 6.25mm × 4.92mm)
(Reference LTC DWG # 05-08-1867 Rev A)



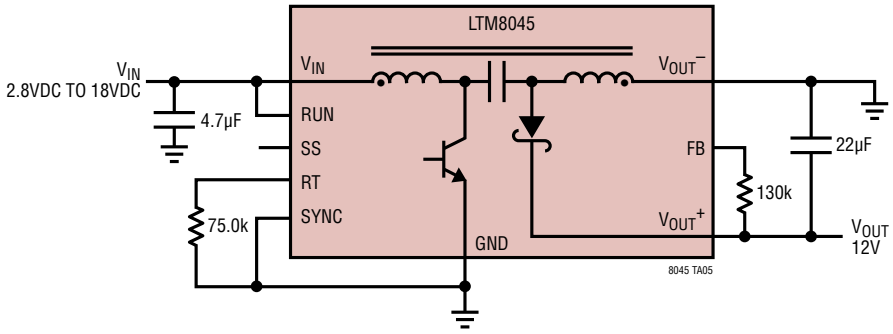
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.71	0.78	0.85	
b1	0.60	0.63	0.66	
D		11.25		
E		6.25		
e		1.27		
F		8.89		
G		5.08		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 40				

REVISION HISTORY

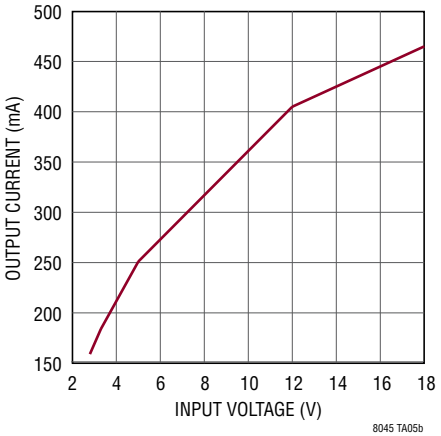
REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/13	Output voltage maximum: changed from 16V and –16V to 15V and –15V, respectively	1
B	02/14	Add SnPb BGA package option	1, 2
C	10/16	Table 1: changed from R_{ADJ} to R_{FB}	12

TYPICAL APPLICATION

12V SEPIC Converter



Maximum Output Current vs Input Voltage $12V_{OUT}$ SEPIC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8047	1.5W, 725VDC Isolated µModule Regulator	1.5W Output Power, 3.1V ≤ V_{IN} ≤ 32V, 2.5V ≤ V_{OUT} ≤ 12V, 9mm × 11.25mm × 4.92mm BGA Package
LTM8048	1.5W, 725VDC Isolated µModule Regulator with Integrated Low Noise Post Regulator	1.5W Output Power, 3.1V ≤ V_{IN} ≤ 32V, 1.2V ≤ V_{OUT} ≤ 12V, 1mV_{P-P} Output Ripple, 9mm × 11.25mm × 4.92mm BGA Package
LTM8025	36V_{IN}, 3A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 24V, Synchronizable, 9mm × 15mm × 4.32mm LGA Package
LTM8033	36V, 3A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 24V, Synchronizable, 11.25mm × 15mm × 4.3mm LGA
LTM8026	36V_{IN}, 5A Step-Down µModule Regulator with Adjustable Current Limit	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, Adjustable Current Limit, Synchronizable, 11.25mm × 15mm × 2.82mm LGA
LTM8027	60V_{IN}, 4A DC/DC Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 60V, 2.5V ≤ V_{OUT} ≤ 24V, Synchronizable, 15mm × 15mm × 4.3mm LGA
LTM4613	36V_{IN}, 8A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	3.3V ≤ V_{OUT} ≤ 15V, 5V ≤ V_{IN} ≤ 36V, PLL Input, V_{OUT} Tracking and Margining, 15mm × 15mm × 4.3mm LGA
LTM8061	32V, 2A Step-Down µModule Battery Charger with Programmable Input Current Limit	Suitable for CC-CV Charging Single and Dual Cell Li-Ion or Li-Poly Batteries, 4.95V ≤ V_{IN} ≤ 32V, C/10 or Adjustable Timer Charge Termination, NTC Resistor Monitor Input, 9mm × 15mm × 4.32mm LGA
LTM8062A	32V, 2A Step-Down µModule Battery Charger with Integrated Maximum Peak Power Tracking (MPPT) for Solar Applications	Suitable for CC-CV Charging Method Battery Chemistries (Li-Ion, Li-Poly, Lead-Acid, $LiFePO_4$), User adjustable MPPT servo voltage, 4.95V ≤ V_{IN} ≤ 32V, 3.3V ≤ V_{BATT} ≤ 18.8V Adjustable, C/10 or Adjustable Timer Charge Termination, NTC Resistor Monitor Input, 9mm × 15mm × 4.32mm LGA
LTC2978	Octal Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, 16-Bit ADC with ±0.25% TUE, 3.3V to 15V Operation
LTC2974	Quad Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, Per Channel Voltage, Current and Temperature Measurements
LTC3880	Dual Output PolyPhase® Step-Down DC/DC Controller with Digital Power System Management	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, ±0.5% Output Voltage, Accuracy, MOSFET Gate Drivers

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