

- Speaker current and voltage monitoring (via the TDM-bus) for Acoustic Echo Cancellation (AEC) at the host
- 16 kHz/32 kHz/44.1 kHz/48 kHz sample frequencies supported
- Ultrasonic support via TDM running at 96 kHz
- Programmable interrupt control via a dedicated interrupt pin
- Low RF susceptibility
- Thermal foldback and overtemperature protection
- 15 kV system-level ESD protection without external components on amplifier output

3 Applications

- Mobile phones and Tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- Internet of Things applications embedding high quality audio

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BAT}	battery supply voltage	on pin VBAT V _{BAT} must not be lower than V _{DDD} in application	2.7	-	5.5	V
V _{DDD}	digital supply voltage	on pin VDDD	1.65	1.8	1.95	V
V _{DDP}	power supply voltage	on pin VDDP	2.7	-	10.0	V
R _L	load resistance		3.2	-	38	Ω
I _{BAT}	battery supply current	Active state on pin VBAT; Operating mode with load R _L = 6 Ω; DC-to-DC in Adaptive Boost mode, P _o = 380 mW, (average music power), V _{BAT} = 4.0 V, V _{BST} = 10 V	-	120	-	mA
		Idle state on pin VBAT; Operating mode with load R _L = 6 Ω; DC-to-DC in Adaptive Boost mode, P _o = 0 mW, V _{BAT} = 4.0 V, V _{BST} = 10 V	-	2.5	-	mA
		Power-down state	-	1	-	μA
I _{DDD}	digital supply current	Active state on pin VDDD; Operating mode with load R _L = 6 Ω; DC-to-DC in Adaptive Boost mode, P _o = 380 mW, (average music power), V _{BAT} = 4.0 V, V _{BST} = 10 V	-	5.2	-	mA
		Idle state on pin VDDD; Operating mode with load R _L = 6 Ω; DC-to-DC in Adaptive Boost mode, P _o = 0 mW, V _{BAT} = 4.0 V, V _{BST} = 10 V	-	3.6	-	mA
		Power-down state	1.6	3	19	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P _{o(AV)}	average output power	THD+N = 1 %; (R _L = 8 Ω; L _L = 44 μH); V _{BST} = 10.0 V; V _{BAT} = 4.0 V; V _{DDD} = 1.8 V	5.3	5.6	-	W
		THD+N = 1 %; (R _L = 6 Ω; L _L = 32 μH); V _{BST} = 10.0 V; V _{BAT} = 4.0 V; V _{DDD} = 1.8 V	5.8	6.1	-	W
		THD+N = 1 %; (R _L = 4 Ω; L _L = 30 μH); V _{BST} = 9.0 V; V _{BAT} = 4.0 V; V _{DDD} = 1.8 V	6	6.2	-	W

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9874UK/N1	WLCSP36	wafer level chip-scale package; 36 bumps; 2.62 mm x 2.51 mm x 0.5 mm body	SOT1780-5
TFA9874BUK/N1	WLCSP36	wafer level chip-scale package; 36 bumps; 2.62 mm x 2.51 mm x 0.525 mm body (backside coating included)	SOT1780-4

6 Block diagram

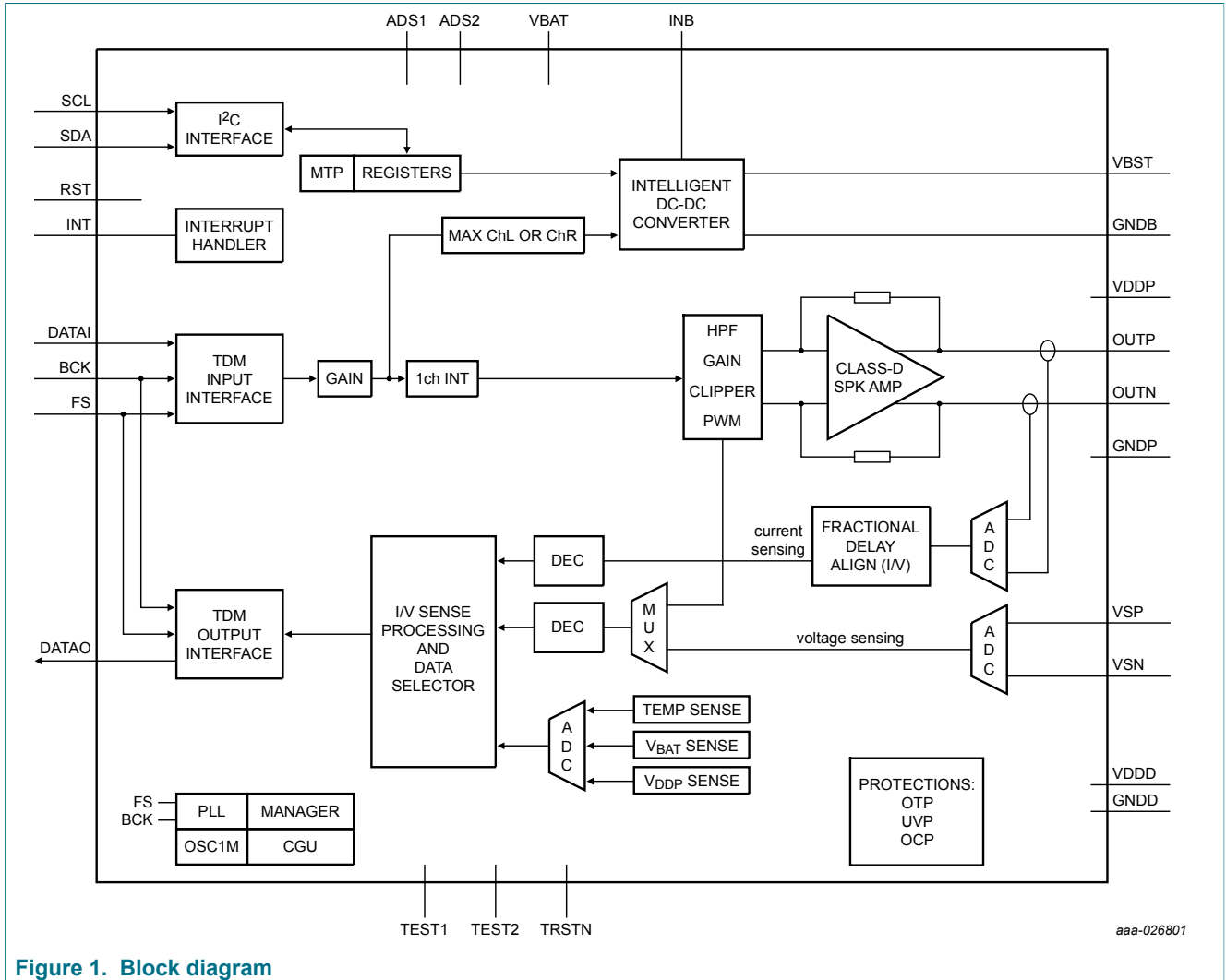
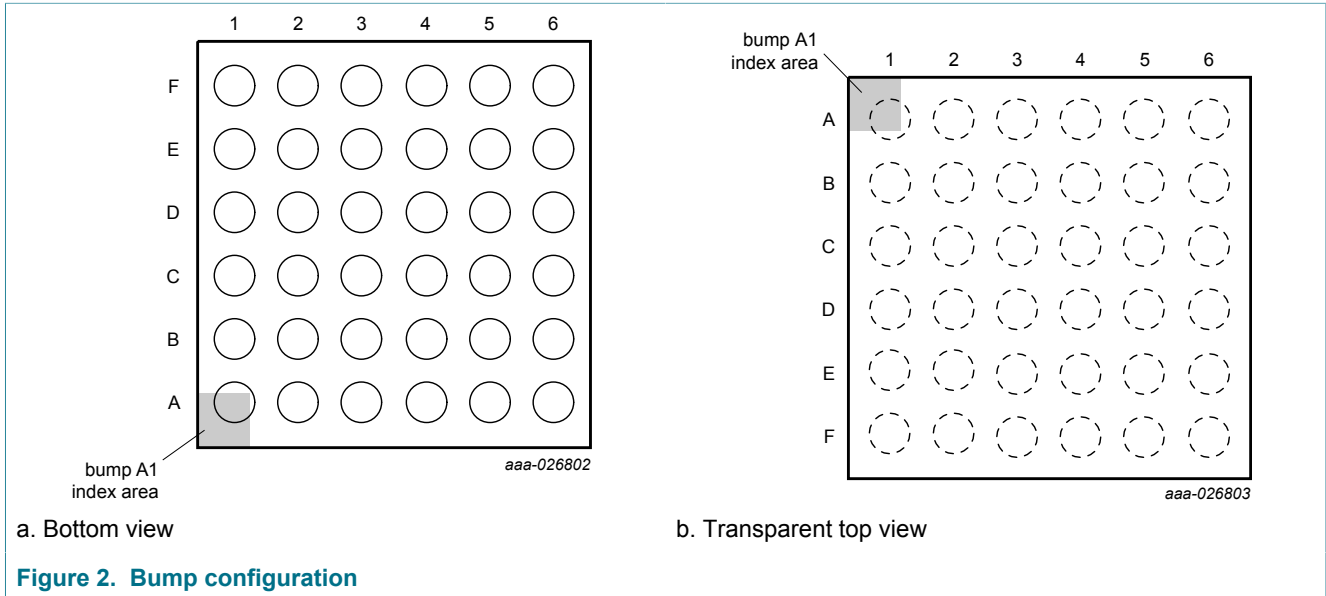


Figure 1. Block diagram

7 Pinning information

7.1 Pinning



	1	2	3	4	5	6
A	BCK	FS	VDDD	SCL	SDA	TRSTN
B	DATAO	DATAI	ADS2	ADS1	INT	VBAT
C	RST	GNDD	VSN	TEST2	TEST1	VSP
D	GNDB	GNDB	GNDB	GNDD	GNDP	GNDD
E	INB	INB	INB	OUTP	GNDP	OUTN
F	VBST	VBST	VBST	VDDP	VDDP	VDDP

aaa-030120

Transparent top view

Figure 3. Bump mapping

Table 3. Pinning

Symbol	Pin	Type	Description
BCK	A1	I	digital audio bit clock input for TDM interface
FS	A2	I	digital audio frame sync input for TDM interface
VDDD	A3	I	digital supply voltage
SCL	A4	I	digital I ² C-bus clock input
SDA	A5	I/O	digital I ² C-bus data input/output
TRSTN	A6	I	test signal input TRSTN, connect to PCB ground
DATAO	B1	I/O	digital audio data output for TDM interface
DATAI	B2	I	digital audio data input for TDM interface

Symbol	Pin	Type	Description
ADS2	B3	I	digital address select input 2
ADS1	B4	I	digital address select input 1
INT	B5	O	digital interrupt output
VBAT	B6	P	battery supply voltage
RST	C1	I	reset input
GNDD	C2	P	digital ground
VSN	C3	I/O	voltage sense negative input
TEST2	C4	I/O	test signal input 2; for test purposes only; connect to PCB ground, or connect via a capacitor to PCB ground
TEST1	C5	I/O	test signal input 1; for test purposes only; connect to PCB ground, or connect via a capacitor to PCB ground input
VSP	C6	I/O	voltage sense positive
GNDB	D1	P	boosted ground
GNDB	D2	P	boosted ground
GNDB	D3	P	boosted ground
GNDD	D4	P	digital ground
GNDP	D5	P	power ground
GNDD	D6	P	digital ground
INB	E1	P	DC-to-DC boost converter input
INB	E2	P	DC-to-DC boost converter input
INB	E3	P	DC-to-DC boost converter input
OUTP	E4	O	non-inverting output
GNDP	E5	P	power ground
OUTN	E6	O	inverting output
VBST	F1	O	boosted supply voltage output
VBST	F2	O	boosted supply voltage output
VBST	F3	O	boosted supply voltage output
VDDP	F4	P	power supply voltage
VDDP	F5	P	power supply voltage
VDDP	F6	P	power supply voltage

8 Functional description

The TFA9874B is a highly efficient Bridge Tied Load (BTL) class-D audio amplifier as depicted in block diagram; see [Figure 1](#).

TFA9874B contains a TDM input/output interface for communicating with the audio host. It also offers the possibility of providing an ultrasonic path to the speaker.

At low battery voltage levels, the gain (from TDM interface to speaker output) is automatically reduced to limit battery current (when battery safeguard is enabled).

The digital audio stream is converted into two Pulse Width Modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the output voltage to the level that is required by the ClassD amplifier.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BAT}	battery supply voltage	on pin VBAT	-0.3	-	+6	V
V _{BST}	booster output voltage	on pin VBST	-0.3	-	+12 ^[1]	V
V _{INB}	booster input voltage	on pin INB	-0.3	-	+12 ^[1]	V
V _{DDP}	power supply voltage	on pin VDDP	-0.3	-	+12 ^[1]	V
V _O	output voltage	on speaker connections; pins OUTP, OUTN	-0.3	-	+12 ^[1]	V
V _{DDD}	digital supply voltage	on pin VDDD	-0.3	-	+2.5	V
V _{low}	low voltage	on pins TEST1/TEST2	-0.3	-	+2.5	V
T _j	junction temperature		-	-	+125	°C
T _{stg}	storage temperature		-55	-	+150	°C
T _{amb}	ambient temperature		-40	-	+85	°C
V _{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	-2	-	+2	kV
		according to Charge Device Model (CDM)	-500	-	+500	V

[1] Using NXP demo board, with a 1 mm wire/PCB track length on INB pin, AC pulses between -6 V and +15 V can be observed without damaging the device, as these spikes do not end up inside the actual device.

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	4-layer application board	49	-	K/W

11 Characteristics

11.1 DC characteristics

Table 6. DC characteristics

All parameters are guaranteed for $V_{BAT} = 3.6\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10.0\text{ V}$, adaptive boost mode; $L_{BST} = 1\ \mu\text{H}^{[1]}$; $R_L = 8\ \Omega^{[1]}$; $L_L = 44\ \mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT V_{BAT} must not be lower than V_{DDD}	2.7	-	5.5	V
I_{BAT}	battery supply current	Active state: On pin VBAT; Operating mode with load $R_L = 6\ \Omega$; DC-to-DC in Adaptive Boost mode; $P_o = 380\text{ mW}$, (average music power), $V_{BAT} = 4.0\text{ V}$	-	120	-	mA
		Idle state: On pin VBAT; Operating mode with load $R_L = 6\ \Omega$ and no output signal (idle); DC-to-DC converter in Adaptive Boost mode; $V_{BAT} = 4.0\text{ V}$	-	2.5	-	mA
		Power-down state: On pin VBAT; DC-to-DC in Power-down mode; $T_j = 25\text{ }^\circ\text{C}$; no clock	-	1	-	μA
V_{DDP}	power supply voltage	on pin VDDP	2.7	-	10.0	V
V_{DDD}	digital supply voltage	on pin VDDD	1.65	1.8	1.95	V
I_{DDD}	digital supply current	Active state	-	5.2	-	mA
		Idle state	-	3.6	-	mA
		Power-down state	1.6	3	19	μA
Pins FS, BCK, DATA1, ADS1, ADS2, SCL, SDA, RST, TRSTN						
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	-	V_{DDD}	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDD}$	V
C_{in}	input capacitance		[2]	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin	-	-	0.1	μA
Pins DATA0, INT, push-pull output stages						
V_{OH}	HIGH-level output voltage		$V_{DDD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage		-	-	400	mV
Pins SDA, open-drain outputs, external 10 kΩ resistor to V_{DDD}						
V_{OH}	HIGH-level output voltage		$V_{DDD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 4\text{ mA}$	-	-	400	mV
Pins OUTP, OUTN						
R_{DSon}	drain-source on-state resistance	PMOS+NMOS transistors	-	430	520	m Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Protection						
$T_{act(th_prot)}$	thermal protection activation temperature		130	-	-	°C
$V_{ovp(VBAT)}$	overvoltage protection on pin VBAT		5.6	-	6.0	V
$V_{uvp(VBAT)}$	undervoltage protection on pin VBAT		2.3	-	2.7	V
$I_{O(ocp)}$	overcurrent protection output current		2.5	-	-	A
DC-to-DC converter						
V_{BST}	voltage on pin VBST	DCVOS = 111111; Boost mode (after trim)	[3] 9.8	10	10.2	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).

[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

[3] Boost switching frequency = 2 MHz in PWM mode.

11.2 AC characteristics

Table 7. AC characteristics

All parameters are guaranteed for $V_{BAT} = 3.6\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10.0\text{ V}$, adaptive boost mode; $L_{BST} = 1\text{ }\mu\text{H}^{[1]}$; $R_L = 8\text{ }\Omega^{[1]}$; $L_L = 44\text{ }\mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier output power						
$P_{O(AV)}$	average output power	Hands-free speaker, THD+N = 1 %; $V_{DDD} = 1.8\text{ V}$				
		$R_L = 8\text{ }\Omega$; $L_L = 44\text{ }\mu\text{H}$; $f_s = 48\text{ kHz}$, $V_{BST} = 10.0\text{ V}$, $V_{BAT} = 4.0\text{ V}$	5.3	5.6	-	W
		$R_L = 6\text{ }\Omega$; $L_L = 32\text{ }\mu\text{H}$; $f_s = 48\text{ kHz}$, $V_{BST} = 10.0\text{ V}$, $V_{BAT} = 4.0\text{ V}$	5.8	6.1	-	W
		$R_L = 4\text{ }\Omega$; $L_L = 30\text{ }\mu\text{H}$; $f_s = 48\text{ kHz}$, $V_{BST} = 9.0\text{ V}$, $V_{BAT} = 4.0\text{ V}$	6	6.2	-	W
		Receiver speaker; THD+N = 1 %; $V_{BST} = 10.0\text{ V}$				
		$R_L = 32\text{ }\Omega$; Voice mode	-	0.2	-	W
$R_L = 32\text{ }\Omega$; Audio mode	-	1.5	-	W		
Amplifier output pins (OUTP and OUTN)						
$ V_{O(offset)} $	output offset voltage	absolute value, after trimming; $V_{DDP} = 3.4\text{ V to }10.0\text{ V}$, $V_{BAT} = 3.4\text{ V to }5\text{ V}$	-	-	1.0	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Amplifier performances							
η_{po}	output power efficiency	On pin VBAT; Operating mode with load $R_L = 6 \Omega$; DC-to-DC in Adaptive Boost mode, $P_o = 380$ mW, (average music power), $V_{BAT} = 4.0$ V	[2]	-	82	-	%
		On pin VBAT; input: 100 Hz sine wave, $R_L = 8 \Omega$; DC-to-DC in Tracking Boost mode, $V_{BAT} = 4.0$ V, $P_o = 600$ mW	[2]	-	91	-	%
		On pin VBAT; Input: 100 Hz sine wave, $R_L = 8 \Omega$; DC-to-DC in Tracking Boost mode, $V_{BAT} = 4.0$ V, $P_o = 4$ W	[2]	-	84	-	%
THD+N	total harmonic distortion-plus-noise	$V_{DDP} > 9$ V, $P_o = 2.0$ W, $R_L = 8 \Omega$	[3]	-	-	0.05	%
		$V_{DDP} > 9$ V, $P_o = 2.0$ W, $R_L = 4 \Omega$	[3]	-	-	0.09	%
$V_{n(o)}$	output noise voltage	A-weighted; no input signal; Low Noise mode; $f_s = 48$ kHz	[2]	-	14	18	μ V
		A-weighted; no input signal; Low Noise mode; $f_s = 16$ kHz, 32 kHz	[2]	-	-	50	μ V
		A-weighted; no input signal; Low Noise mode; $f_s = 44.1$ kHz	[2]	-	15	18	
DR	dynamic range	A-weighted; $V_{BAT} = 3.4$ V to 5 V; S/N = maximum signal (at THD = 1 %); output noise voltage ($V_{n(o)}$); NO signal applied	[2]	110	114	-	dB
S/N	signal-to-noise ratio	A-weighted, $V_{BAT} = 3.4$ V to 5 V, maximum signal at THD = 1 %	[2]	100	-	-	dB
PSRR	power supply rejection ratio	from V_{BAT} ; booster in follower mode ($V_{DDP} = V_{BAT}$) $f_{ripple} = 217$ Hz square wave, $V_{ripple} = 50$ mV _(p-p) , $V_{BAT} = 4.0$ V		60	80	-	dB
		from V_{BAT} ; booster in follower mode ($V_{DDP} = V_{BAT}$) $f_{ripple} = 20$ Hz to 1 kHz sine wave, $V_{ripple} = 200$ mV (RMS), $V_{BAT} = 3.4$ V to 5.0 V Low Power AND Low Noise modes on		60	80	-	dB
		from V_{BAT} ; booster in follower mode ($V_{DDP} = V_{BAT}$) $f_{ripple} = 1$ kHz to 20 kHz sine wave, $V_{ripple} = 200$ mV (RMS), $V_{BAT} = 3.4$ V to 5.0 V		55	60	-	dB
$\Delta G/\Delta f$	gain variation with frequency	BW = 20 Hz to 15 kHz, $V_{BAT} = 3.4$ V to 5 V		-0.1	-	+0.7	dB
V_{POP}	pop noise voltage	At mode transition and gain change.		-	-	2	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_L	load resistance		3.2	8	38	Ω
C_L	load capacitance		-	-	200	pF
f_{sw}	switching frequency	directly coupled to the TDM input frequency	256	-	384	kHz
$G_{(TDM-VO)}$	TDM to V_O gain	INPLEV = 0 dB	6	-	21	dB
Amplifier power-up, power-down and propagation delays						
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK, $f_s = 48$ kHz	-	2	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time	$f_s = 48$ kHz	-	1	-	ms
$t_{d(off)}$	turn-off delay time		-	32	-	μ s
$t_{d(alarm)}$	alarm delay time		-	200	-	ms
t_{PD}	propagation delay	Delta Propagation delay between L & R in stereo application = 1.625 FS				
		$f_s = 16$ kHz	-	-	850	μ s
		$f_s = 16$ kHz HP	-	-	850	μ s
		$f_s = 32$ kHz	-	-	750	μ s
		$f_s = 44.1$ kHz	-	-	650	μ s
		$f_s = 48$ kHz	-	-	700	μ s
		$f_s = 96$ kHz	-	-	600	μ s
Booster Inductance						
L_{bst}	boost inductance		0.33	1.0	2.2	μ H
Voltage and Current-sensing performance						
S/N	signal-to-noise ratio	$I_O = 1.1$ A (peak); A-weighted	62	65	-	dB
$\Delta V_{sense}/I_{sense}$	V_{sense}/I_{sense} ratio mismatch	Pilot tone -40 dBFS	[4]	2	-	%
THD+N	total harmonic distortion-plus-noise	$f_i = 20$ Hz to 20 kHz, $V_i = -12$ dBFS	-	-	0.75	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
 [2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
 [3] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance (speaker).
 [4] Intended for Speaker protection. In combination with NXP Speaker protection a speaker temperature accuracy of ± 10 °C can be realized.

11.3 TDM timing characteristics

Table 8. TDM bus interface characteristics

All parameters are guaranteed for $V_{BAT} = 3.6\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10.0\text{ V}$, adaptive boost mode; $L_{BST} = 1\ \mu\text{H}^{[1]}$; $R_L = 8\ \Omega^{[1]}$; $L_L = 44\ \mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency	on pin WS, audio mode	[2] 16	-	48	kHz
		on pin WS, ultrasonic mode	-	-	96	kHz
f_{clk}	clock frequency	on pin BCK, audio mode	[2] $32f_s$	-	$384f_s$	kHz
		on pin BCK, ultrasonic mode	-	-	$96f_s$	MHz
t_{su}	set-up time	WS edge to BCK HIGH	[3] 10	-	-	ns
		DATA edge to BCK HIGH	10	-	-	ns
t_h	hold time	BCK HIGH to WS edge	[3] 10	-	-	ns
		BCK HIGH to DATA edge	10	-	-	ns
t_j	external clock jitter	PLL locked on BCK	[4] -	1	2	ns
		PLL locked on FS	[5] -	-	20	ns

- [1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
- [2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. Note that both the BCK and WS signals need to be present for the clock to operate correctly.
- [3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
- [4] When the PLL is locked on BCK, amplifier output noise can deteriorate when clock jitter >1 ns; performance is guaranteed up to jitter = 2 ns.
- [5] The system is less sensitive to jitter when the PLL is locked on FS.

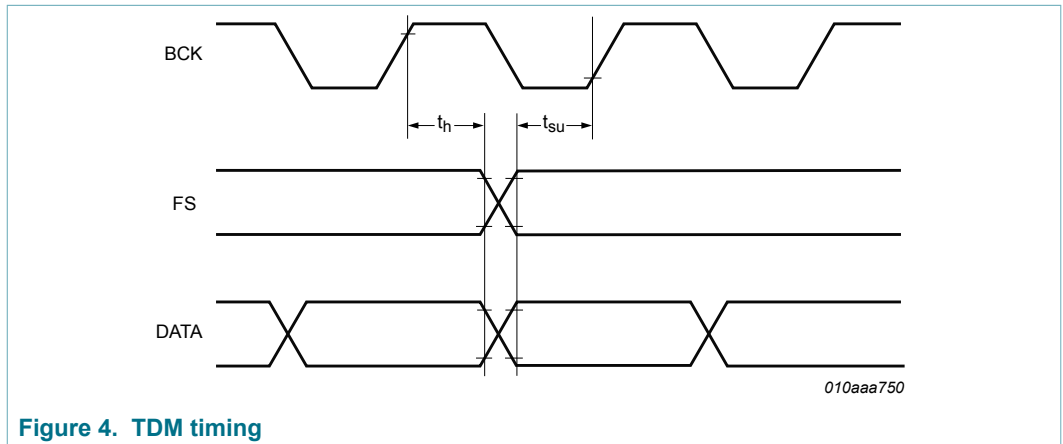


Figure 4. TDM timing

11.4 I²C timing characteristics

Table 9. I²C-bus interface characteristics; see Figure 15

All parameters are guaranteed for $V_{BAT} = 3.6\text{ V}$; $V_{DD} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 10.0\text{ V}$, adaptive boost mode; $L_{BST} = 1\text{ }\mu\text{H}^{[1]}$; $R_L = 8\text{ }\Omega^{[1]}$; $L_L = 44\text{ }\mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{LOW}	LOW period of the SCL clock		1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	μs
t_r	rise time	SDA and SCL signals	[2] $20 + 0.1 C_b$	-	-	ns
t_f	fall time	SDA and SCL signals	[2] $20 + 0.1 C_b$	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3] 0.6	-	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	μs
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	μs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	μs
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4] 0	-	50	ns
C_b	capacitive load for each bus line		-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
 [2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
 [3] After this period, the first clock pulse is generated.
 [4] To be suppressed by the input filter.

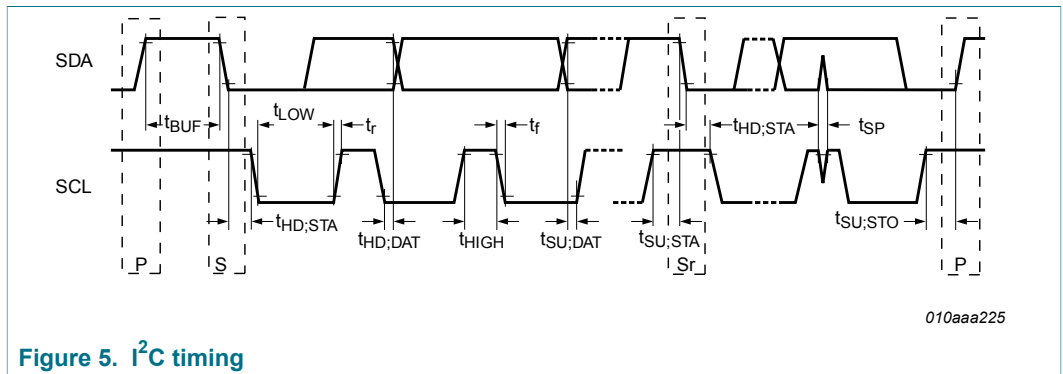


Figure 5. I²C timing

12 Application information

12.1 Application diagrams

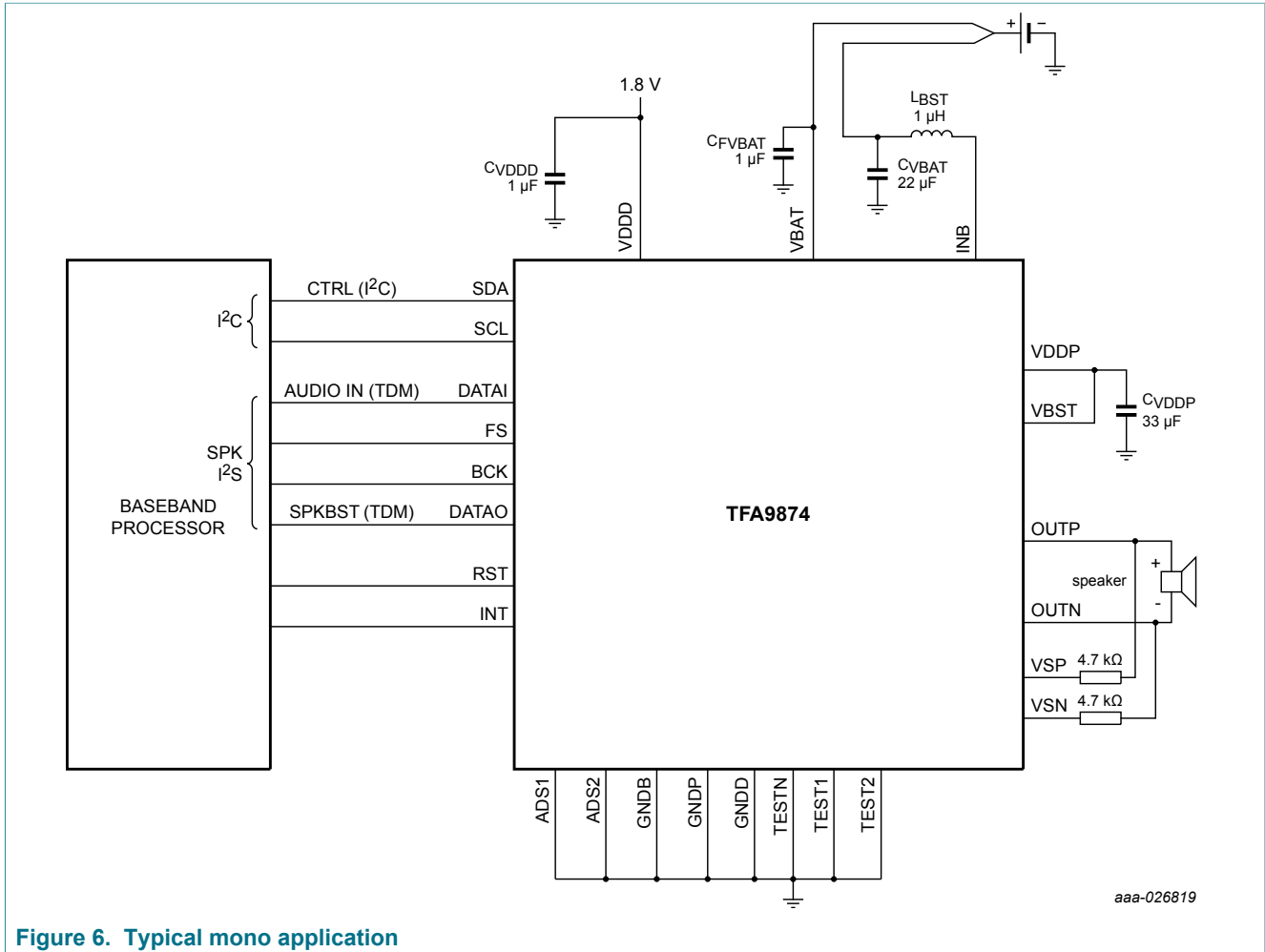


Figure 6. Typical mono application

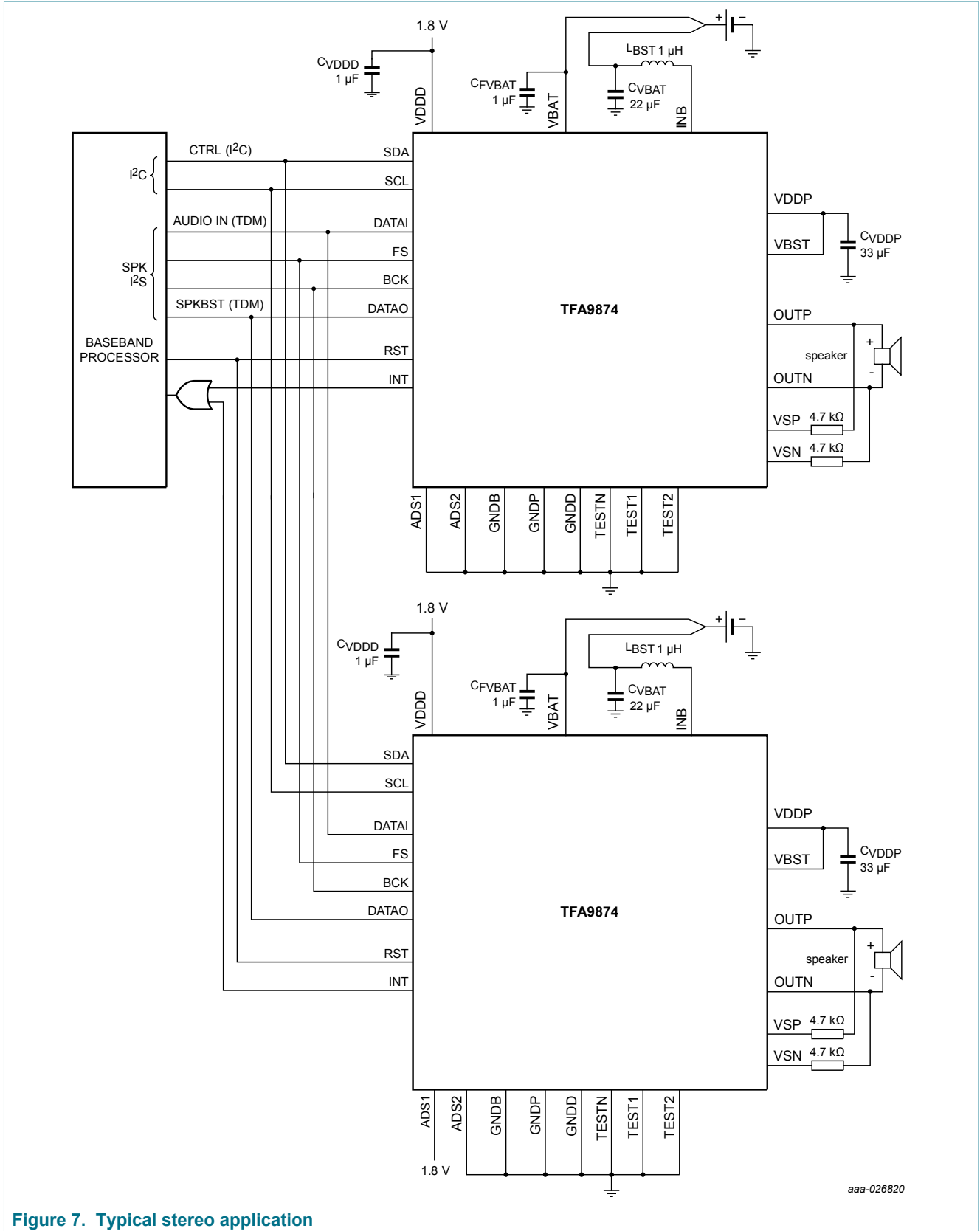


Figure 7. Typical stereo application

13 Package outline

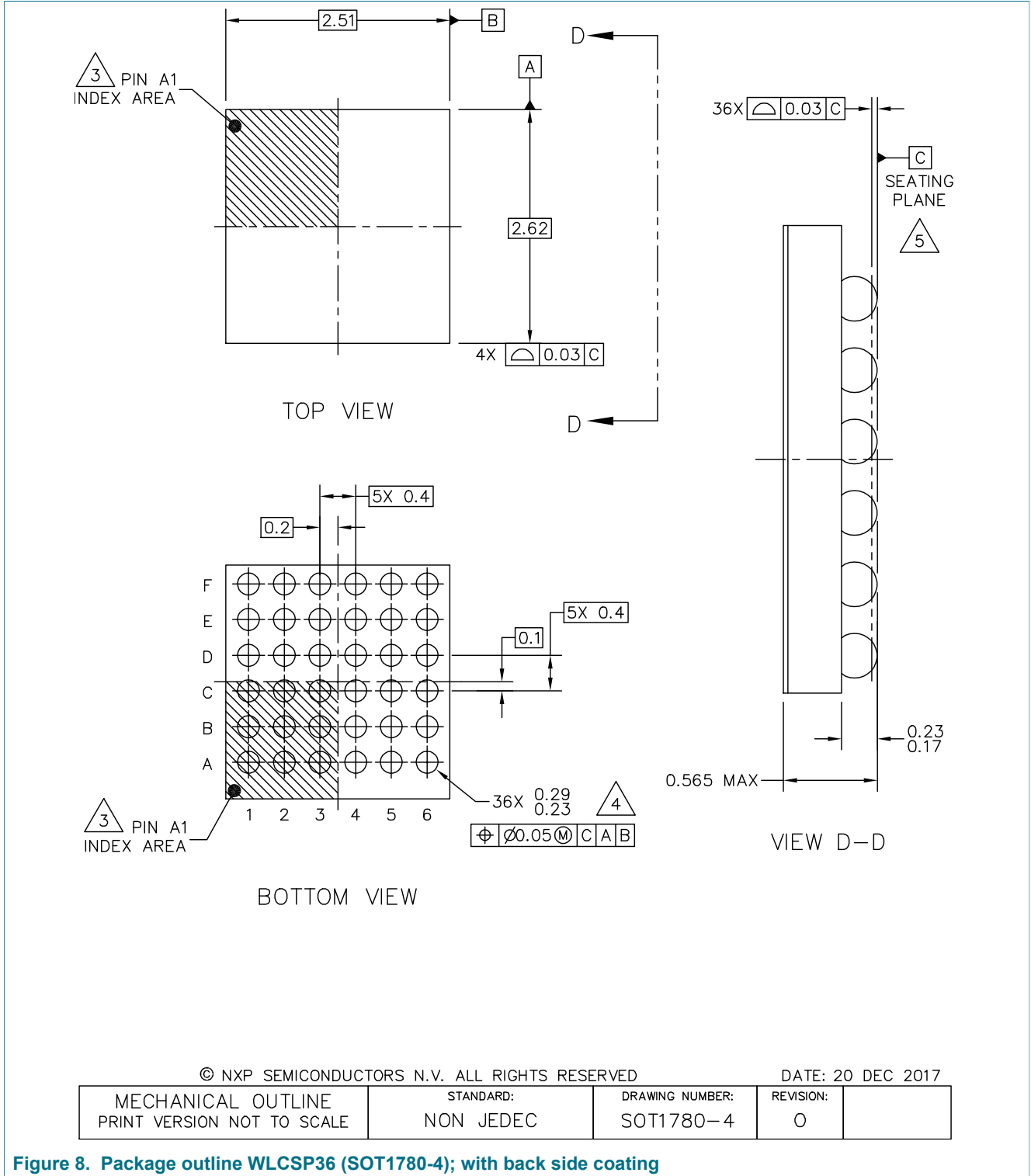


Figure 8. Package outline WLCSP36 (SOT1780-4); with back side coating

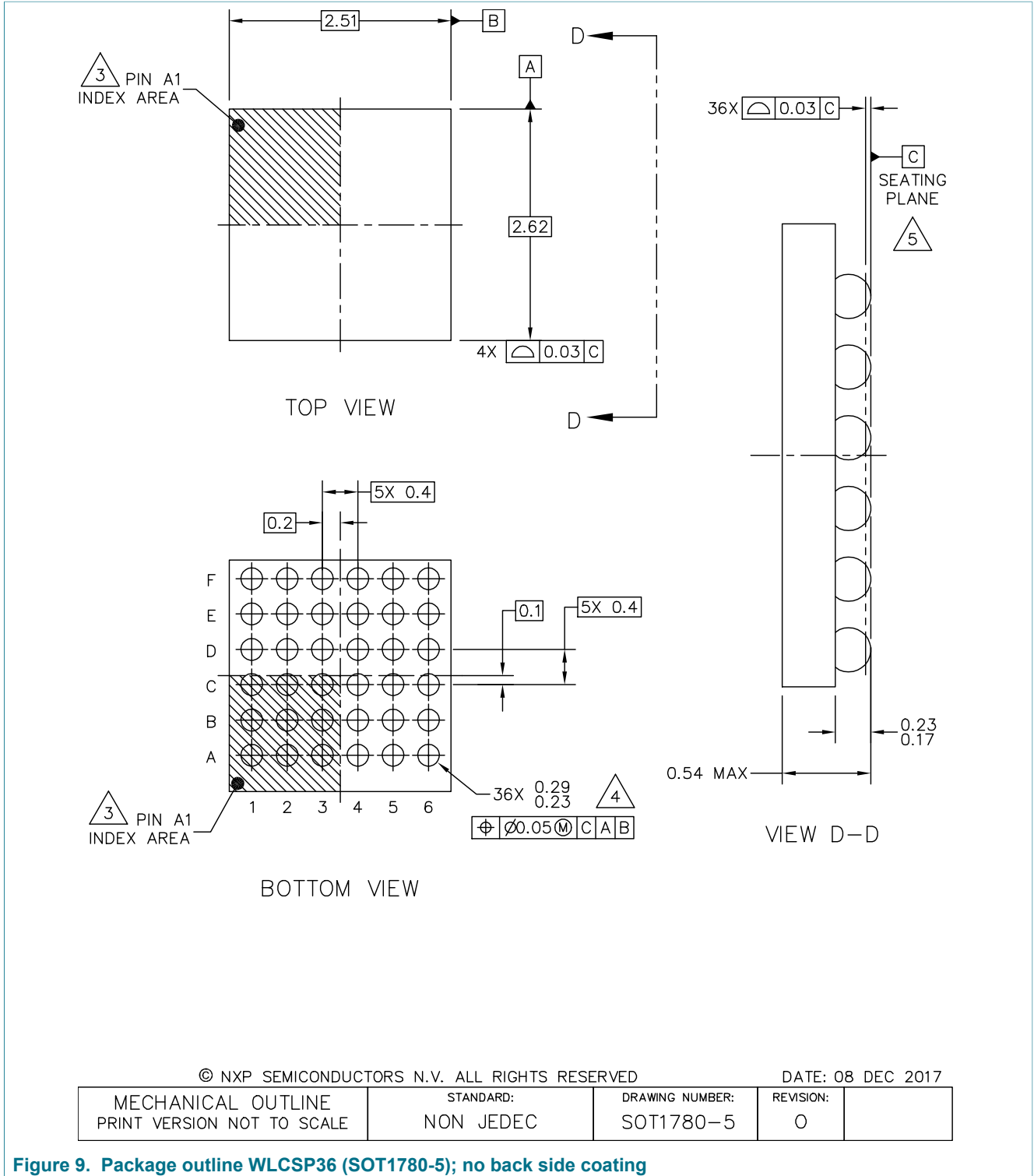


Figure 9. Package outline WLCSP36 (SOT1780-5); no back side coating

14 Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 "Wafer Level Chip Scale Package" and in application note AN10365 "Surface mount reflow soldering description".

Wave soldering is not suitable for this package.

All NXP Semiconductors WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

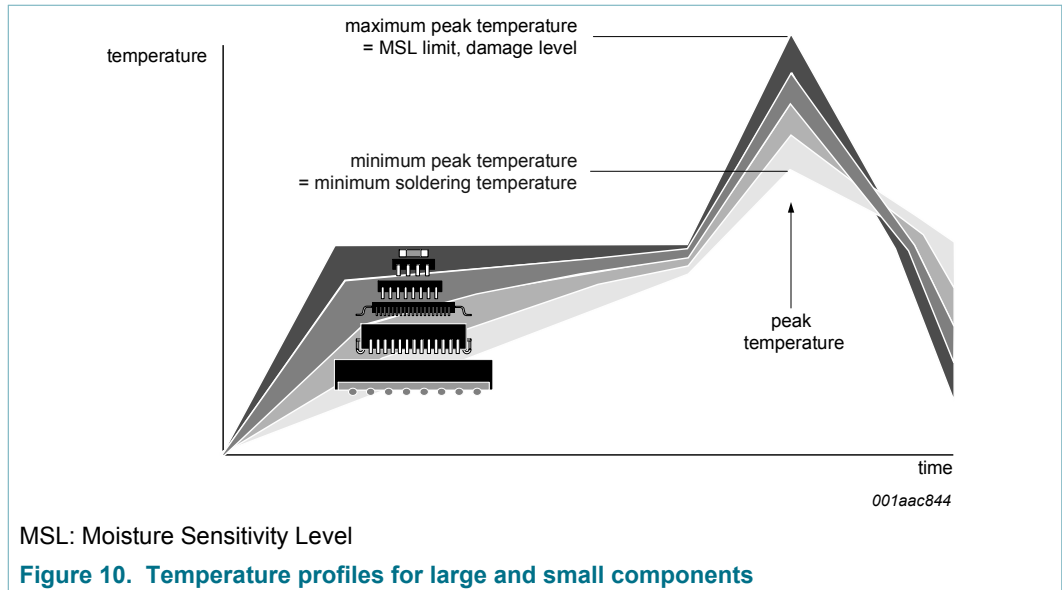
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 10](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#).

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 10](#).



For further information on temperature profiles, refer to application note AN10365 "Surface mount reflow soldering description".

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The

surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9874B_SDS v.1	20180814	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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