Full CMOS output levels help reduce power in many other system components.

The AT22LV10 and AT22LV10L logic architectures are identical to the familiar 22V10. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power-up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

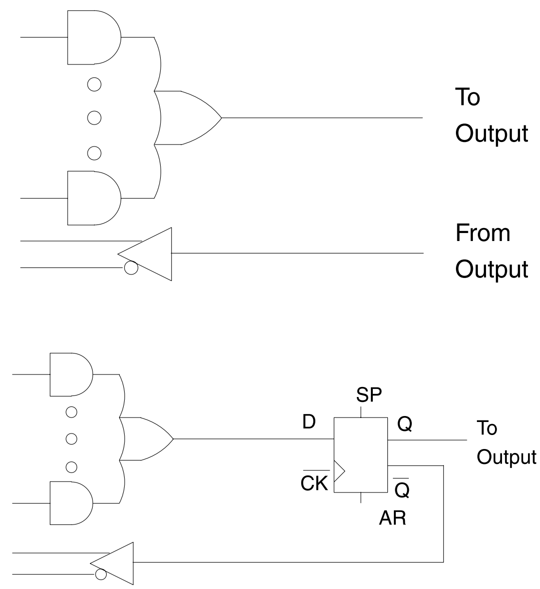
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V (1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V (1)
Integrated UV Erase Dose	7258 W•sec/cm^2

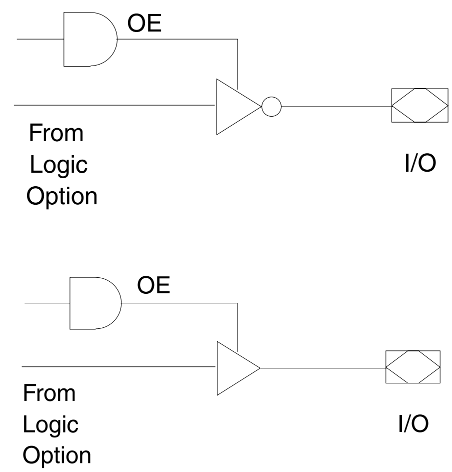
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum pin voltage is V_{CC} + 0.75V DC which may undershoot to V_{CC} + 2.0V for pulses of less than 20 ns.

Logic Options



Output Options



DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3.0V to 5.5V	3.0V to 5.5V

DC Characteristics

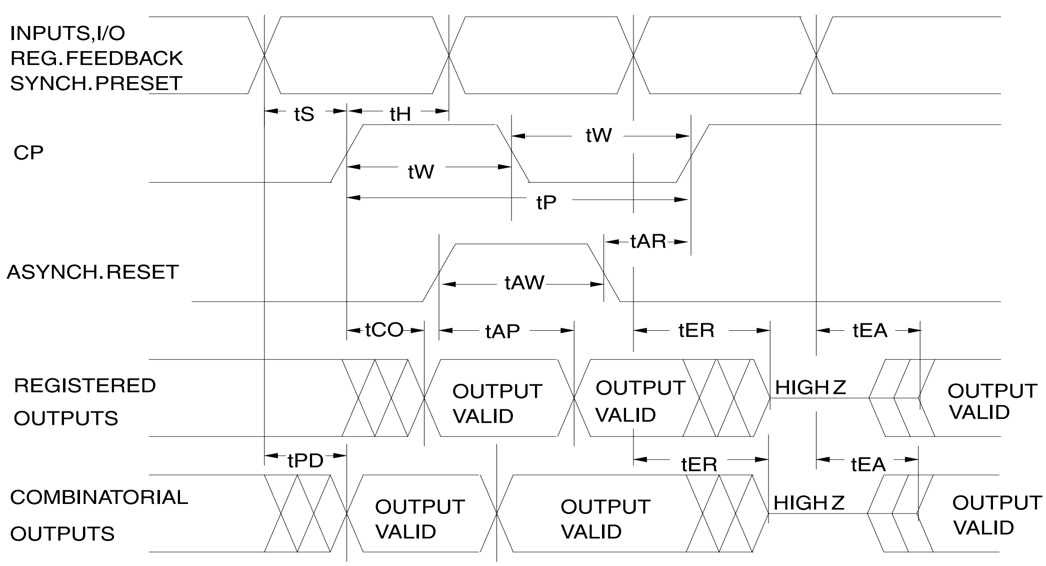
Symbol	Parameter	Condition[2]			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current	V_{CC} = 3.6V/5.5V, V_{IN} = GND, Outputs Open	AT22LV10	Com.		20/50	35/90	mA
				Ind.		20/50	45/100	mA
			AT22LV10L	Com.		1/2	4/12	mA
				Ind.		1/2	5/15	mA
I_{OS}[1]	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL1}	Input Low Voltage	4.5V ≤ $V_{CC} \leq$ 5.5V			-0.6		0.8	V
V_{IL2}	Input Low Voltage	3.0V ≤ $V_{CC} <$ 4.5V			-0.6		0.6	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage V_{IN} = V_{IH} or V_{IL}	V_{CC} = 3.0V	Com., Ind.	I_{OL} = 8 mA			0.5	V
		V_{CC} = 4.5V	Com., Ind.	I_{OL} = 16 mA			0.5	V
		V_{CC} = 3.0V	Com., Ind.	I_{OL} = 6 mA			0.35	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 3.0V/4.5V	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -0.4 mA/-4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. For DC characteristics, the test condition of V_{CC} = Max corresponds to 3.6V.

AC Characteristics for the AT22LV10

Symbol	Parameter	AT22LV10-20			AT22LV10-25			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		12	20		15	25	ns
t_{EA}	Input to Output Enable			20		15	25	ns
t_{ER}	Input to Output Disable			20		15	25	ns
t_{CF}	Clock to Feedback	0	4	9	0	5	9	ns
t_{CO}	Clock to Output	0	8	14	0	10	17	ns
t_S	Input or Feedback Setup Time	10	6		12	7		ns
t_H	Hold Time	0			0			ns
t_P	Clock Period	10			12			ns
t_W	Clock Width	5			6			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			41.6			34.5	MHz
	Internal Feedback $1/(t_S + t_{CF})$			52.6			47.6	MHz
	No Feedback $1/(t_P)$			100.0			83.3	MHz
t_{AW}	Asynchronous Reset Width	20	12		25	15		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	20	12		25	15		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		15	25		18	28	ns

AC Waveforms[1]

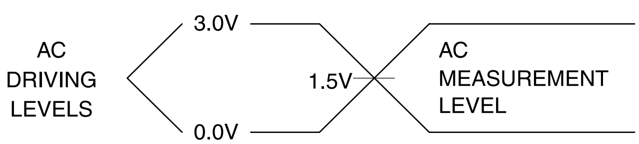


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics for the AT22LV10L

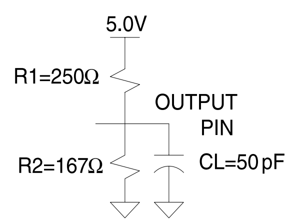
Symbol	Parameter	AT22LV10L-25			Units
		Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		15	25	ns
t_{EA}	Input to Output Enable		15	25	ns
t_{ER}	Input to Output Disable		15	25	ns
t_{CF}	Clock to Feedback	0	5	9	ns
t_{CO}	Clock to Output	0	10	14	ns
t_{SF}	Feedback Setup Time	12	7		ns
t_S	Input Setup Time	17	15		ns
t_H	Hold Time	0			ns
t_P	Clock Period	12			ns
t_W	Clock Width	6			ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$			32.2	MHz
	Internal Feedback $1/(t_{SF} + t_{CF})$			47.6	MHz
	No Feedback $1/(t_P)$			83.3	MHz
t_{AW}	Asynchronous Reset Width	25	15		ns
t_{AR}	Asynchronous Reset Recovery Time	25	15		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		18	28	ns

Input Test Waveforms and Measurement Levels

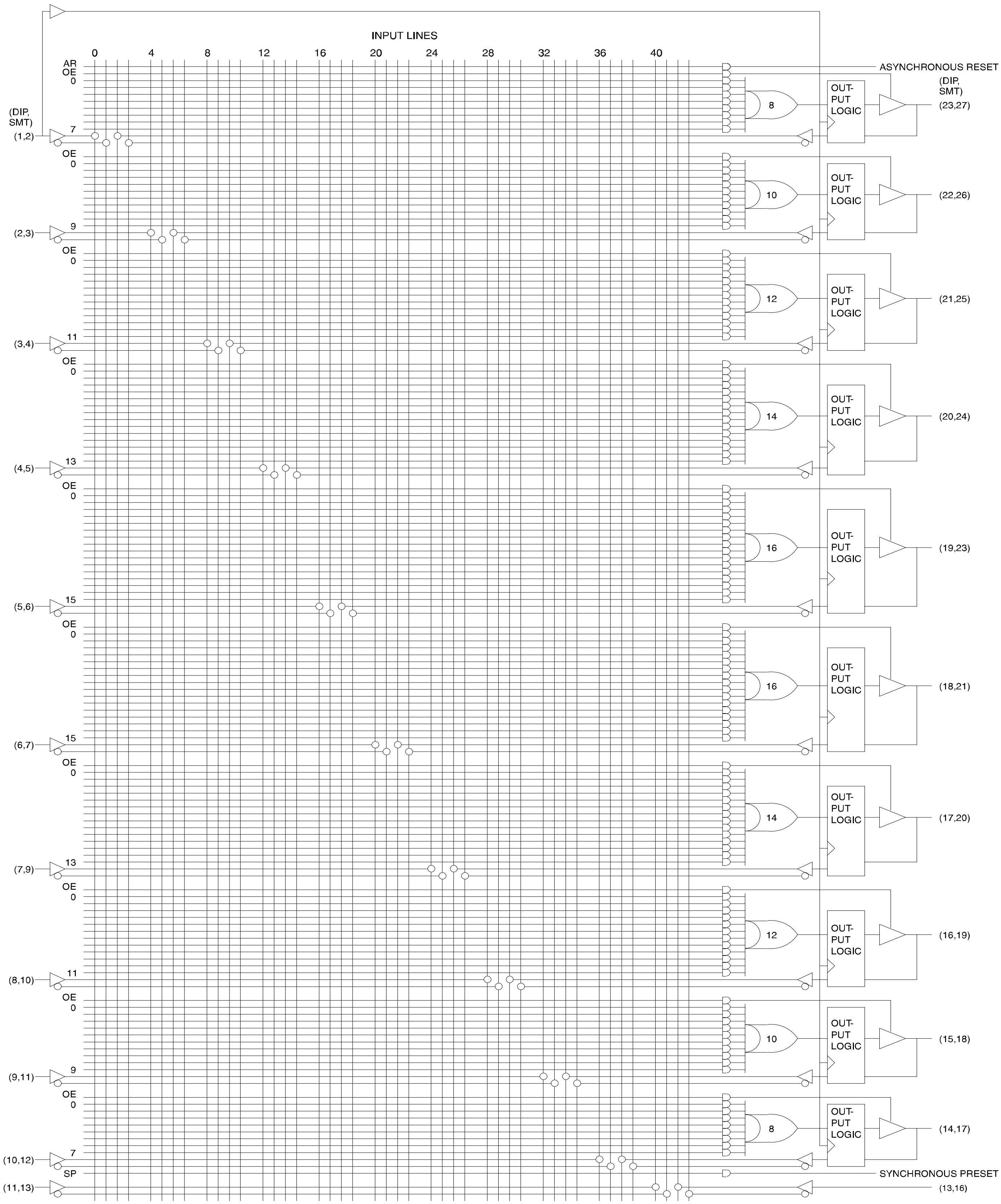


Output Test Loads

Commercial



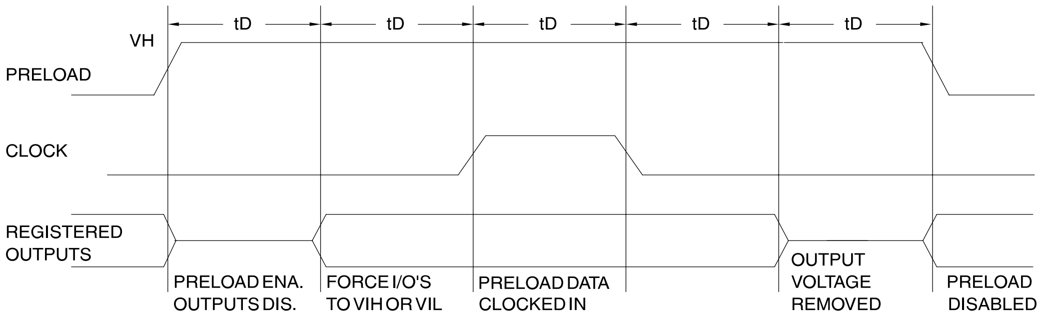
Functional Logic Diagram AT22LV10(L)



Preload of Registered Outputs

The registers in the AT22LV10 and AT22LV10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5V to 13V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level Forced on Registered Output Pin During Preload Cycle	Register State After Cycle
V_{IH}	High
V_{IL}	Low

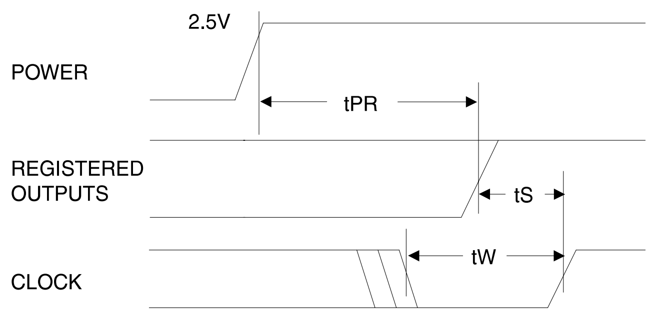


Power-up Reset

The registers in the AT22LV10 and AT22LV10L are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing 2.5V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonis;
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-up Reset Time		600	1000	ns

Pin Capacitance

(f = 1 MHz, T = 25°C)[1]

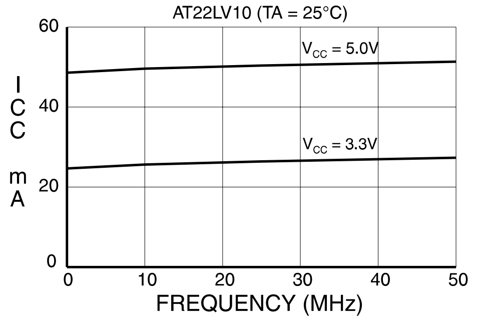
	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

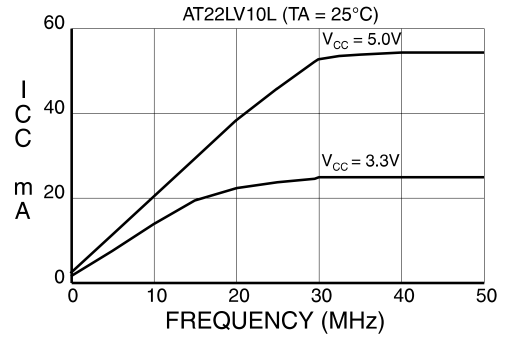
Erasure Characteristics

The entire fuse array of an AT22LV10 or AT22LV10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

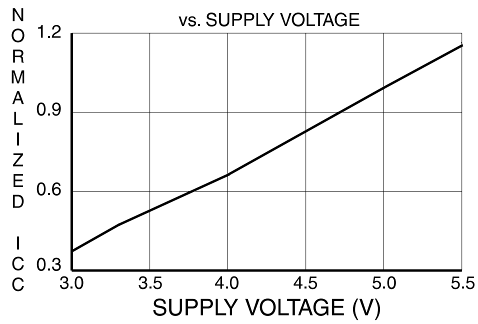
SUPPLY CURRENT vs. INPUT FREQUENCY



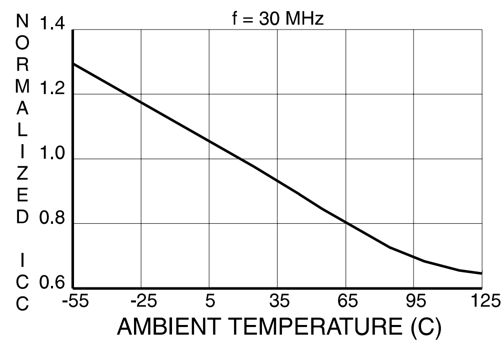
SUPPLY CURRENT vs. INPUT FREQUENCY



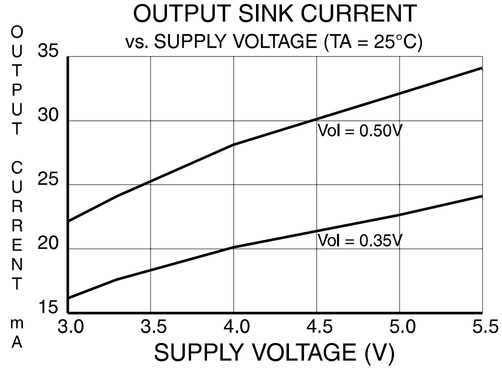
NORMALIZED SUPPLY CURRENT



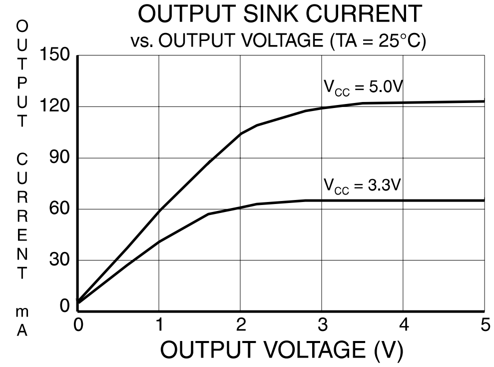
NORMALIZED ICC vs. AMBIENT TEMP.



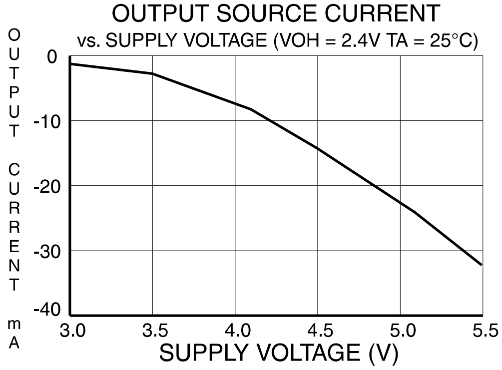
OUTPUT SINK CURRENT



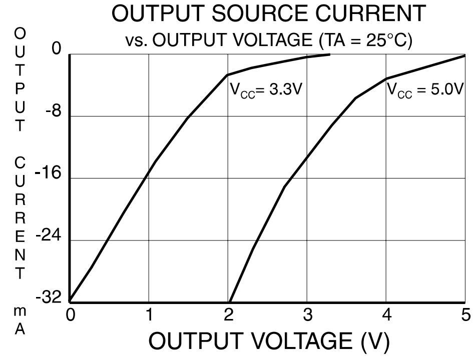
OUTPUT SINK CURRENT

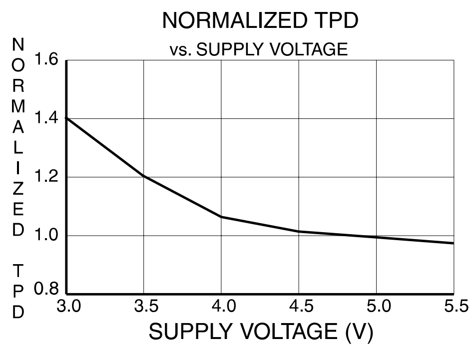


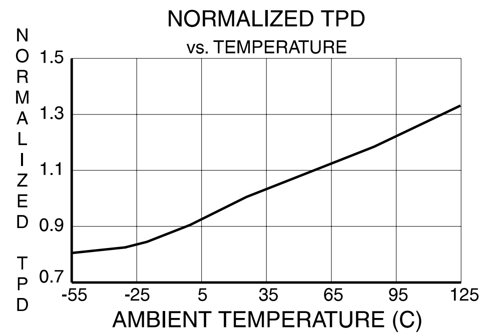
OUTPUT SOURCE CURRENT

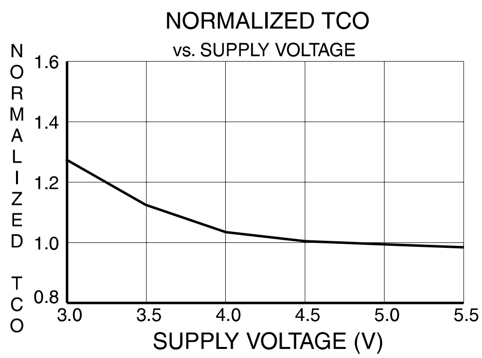


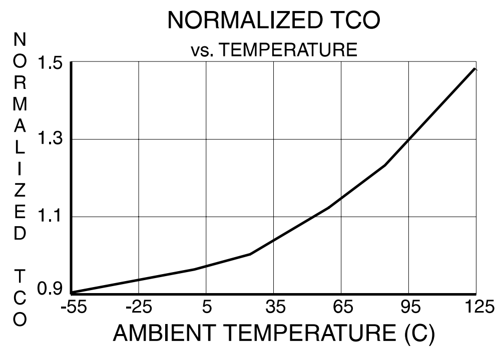
OUTPUT SOURCE CURRENT

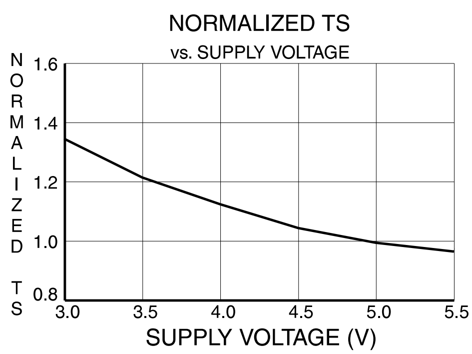


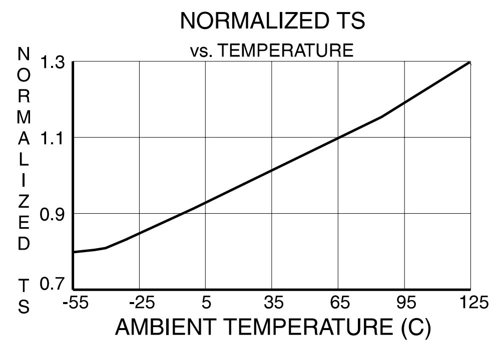

NORMALIZED TPD
vs. SUPPLY VOLTAGE
NORMALIZED TPD
1.6
1.4
1.2
1.0
0.8
3.0
3.5
4.0
4.5
5.0
5.5
SUPPLY VOLTAGE (V)

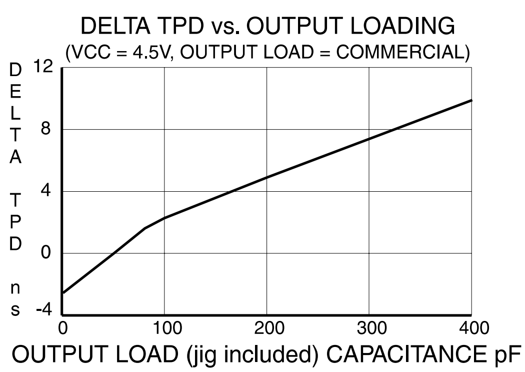

NORMALIZED TPD
vs. TEMPERATURE
NORMALIZED TPD
1.5
1.3
1.1
0.9
0.7
-55
-25
5
35
65
95
125
AMBIENT TEMPERATURE (C)

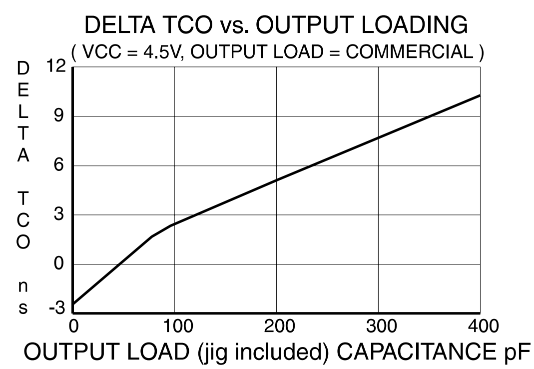

NORMALIZED TCO
vs. SUPPLY VOLTAGE
NORMALIZED TCO
1.6
1.4
1.2
1.0
0.8
3.0
3.5
4.0
4.5
5.0
5.5
SUPPLY VOLTAGE (V)


NORMALIZED TCO
vs. TEMPERATURE
NORMALIZED TCO
1.5
1.3
1.1
0.9
-55
-25
5
35
65
95
125
AMBIENT TEMPERATURE (C)


NORMALIZED TS
vs. SUPPLY VOLTAGE
NORMALIZED TS
1.6
1.4
1.2
1.0
0.8
3.0
3.5
4.0
4.5
5.0
5.5
SUPPLY VOLTAGE (V)


NORMALIZED TS
vs. TEMPERATURE
NORMALIZED TS
1.3
1.1
0.9
0.7
-55
-25
5
35
65
95
125
AMBIENT TEMPERATURE (C)


DELTA TPD vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)
DELTA TPD ns
12
8
4
0
-4
0
100
200
300
400
OUTPUT LOAD (jig included) CAPACITANCE pF


DELTA TCO vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)
DELTA TCO ns
12
9
6
3
0
-3
0
100
200
300
400
OUTPUT LOAD (jig included) CAPACITANCE pF

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	10	14	AT22LV10-20JC AT22LV10-20PC AT22LV10-20SC	28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-20JI AT22LV10-20PI AT22LV10-20SI	28J 24P3 24S	Industrial (-40°C to 85°C)
25	12	17	AT22LV10-25JC AT22LV10-25PC AT22LV10-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-25JI AT22LV10-25PI AT22LV10-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
25	17	14	AT22LV10L-25JC AT22LV10L-25PC AT22LV10L-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10L-25JI AT22LV10L-25PI AT22LV10L-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)

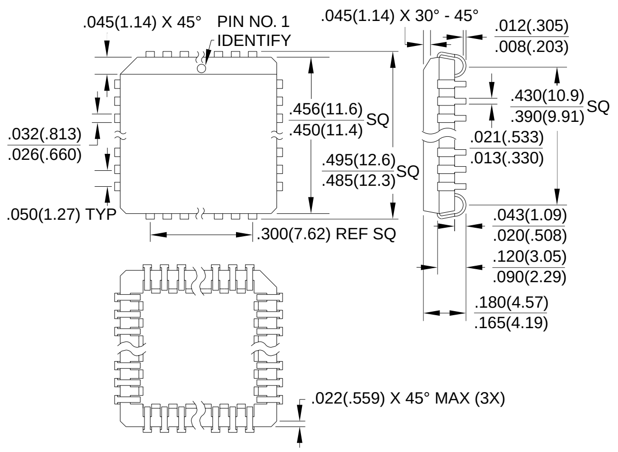
Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

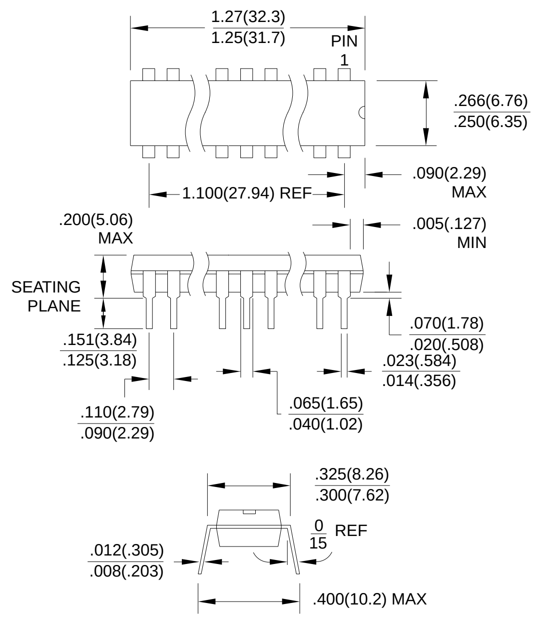
Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier OTP (PLCC)
24P3	24-lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24-lead, 0.300" Wide, Plastic Gull-Wing Small Outline OTP (SOIC)

Packaging Information

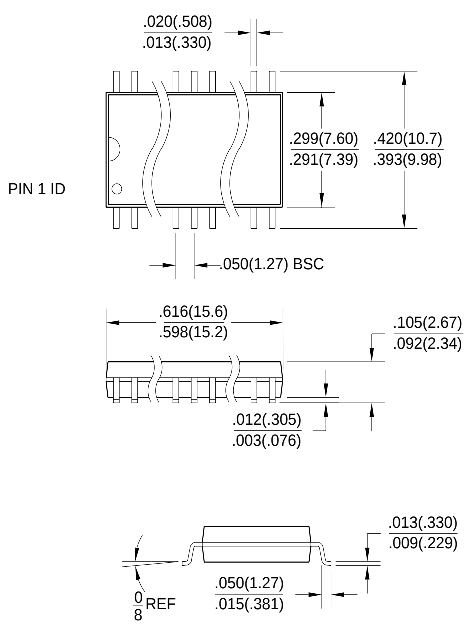
28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AB



24P3, 24-lead, 0.300" Wide. Plastic
Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AB



24S, 24-lead, 0.300" Wide, Plastic Gull-Wing Small
Outline (SOIC)
Dimensions in Inches and (Millimeters)



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