

**Truth Table**

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

**Division Ratio Table**

A	B	Number of Counter Stages	Count
		n	2 <sup>n</sup>
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

**Operating Characteristics**

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3 R_{TC} C_{TC}} \text{ if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

and  $R_S \approx 2 R_{TC}$  where  $R_S \geq 10 \text{ k}\Omega$

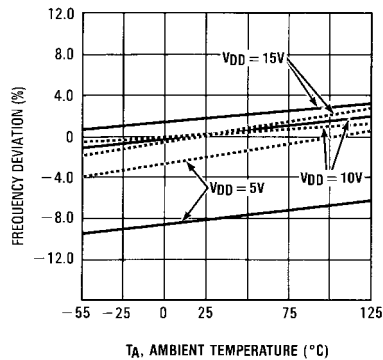
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages ( $2^8$ ,  $2^{10}$ ,  $2^{13}$ , and  $2^{16}$ ). The  $2^n$  counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is "1",  $2^{16}$  is selected for both states of B.

However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting  $2^8$ ).

The  $Q/\bar{Q}$  select output control pin provides for a choice of output level. When the counter is in a reset condition and  $Q/\bar{Q}$  select pin is set to a "0" the Q output is a "0". Correspondingly, when  $Q/\bar{Q}$  select pin is set to a "1" the Q output is a "1".

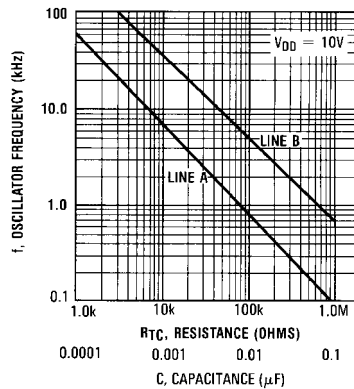
When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after  $2^{n-1}$  counts the RS flip-flop sets which causes the output to change state. Hence, after another  $2^{n-1}$  counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

**Typical RC Oscillator Characteristics**



Solid Line =  $R_{TC} = 56 \text{ k}\Omega$ ,  $R_S = 1 \text{ k}\Omega$  and  $C = 1000 \text{ pF}$   
 $f = 10.2 \text{ kHz}$  @  $V_{DD} = 10\text{V}$  and  $T_A = 25^\circ$   
 Dashed Line =  $R_{TC} = 56 \text{ k}\Omega$ ,  $R_S = 120 \text{ k}\Omega$  and  $C = 1000 \text{ pF}$   
 $f = 7.75 \text{ kHz}$  @  $V_{DD} = 10\text{V}$  and  $T_A = 25^\circ$

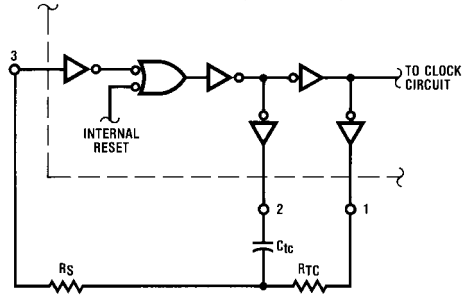
**RC Oscillator Frequency as a Function of  $R_{TC}$  and C**



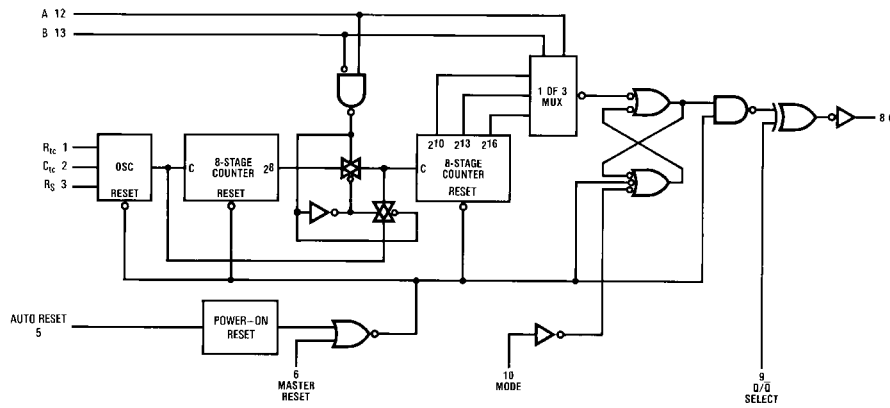
Line A:  $f$  as a function of  $C$  and ( $R_{TC} = 56 \text{ k}\Omega$ ;  $R_S = 120\text{k}$ )  
 Line B:  $f$  as a function of  $R_{TC}$  and ( $C = 100 \text{ pF}$ ;  $R_S = 2 R_{TC}$ )

**Operating Characteristics** (Continued)

**Oscillator Circuit Using RC Configuration**



**Logic Diagram**



V<sub>DD</sub> = Pin 14

V<sub>SS</sub> = Pin 7

**Absolute Maximum Ratings** (Note 1)

(Note 2)

Supply Voltage ( $V_{DD}$ )	-0.5V to +18V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD} + 0.5V$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{DD}$ )	3V to 15V
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$
Operating Temperature Range	-55°C to +125°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		5		0.005	5	150	$\mu A$	
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		10		0.010	10	300		
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.015	20	600		
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05	0.05	V	
		$V_{DD} = 10V$		0.05		0	0.05	0.05		
		$V_{DD} = 15V$		0.05		0	0.05	0.05		
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95	V	
		$V_{DD} = 10V$	9.95		9.95	10		9.95		
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2	1.5	1.5	V	
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4	3.0	3.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6	4.0	4.0		
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5	V	
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		
$I_{OL}$	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	2.85		2.27	3.6		1.6	mA	
		$V_{DD} = 10V, V_O = 0.5V$	4.16		4.0	9.0		2.8		
		$V_{DD} = 15V, V_O = 1.5V$	19.3		15.6	34.0		10.9		
$I_{OH}$	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 2.5V$	7.96		6.42	130		4.49	mA	
		$V_{DD} = 10V, V_O = 9.5V$	4.19		3.38	8.0		2.37		
		$V_{DD} = 15V, V_O = 13.5V$	16.3		13.2	30.0		9.24		
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		$-10^{-5}$	-0.1	-1.0	$\mu A$	
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1	1.0		

**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

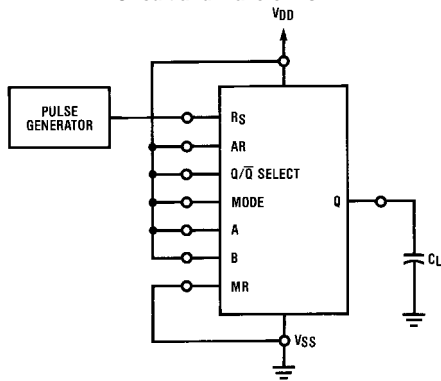
<b>AC Electrical Characteristics</b> (Note 4)						
T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF (refer to test circuits)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>TLH</sub>	Output Rise Time	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		50 30 25	200 100 80	ns
t <sub>THL</sub>	Output Fall Time	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		50 30 25	200 100 80	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Turn-Off, Turn-On Propagation Delay, Clock to Q (2 <sup>8</sup> Output)	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		1.8 0.6 0.4	4.0 1.5 1.0	μs
t <sub>PHL</sub> , t <sub>PLH</sub>	Turn-On, Turn-Off Propagation Delay, Clock to Q (2 <sup>16</sup> Output)	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		3.2 1.5 1.0	8.0 3.0 2.0	μs
t <sub>WH(CL)</sub>	Clock Pulse Width	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	400 200 150	200 100 70		ns
f <sub>CL</sub>	Clock Pulse Frequency	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		2.5 6.0 8.5	1.0 3.0 4.0	MHz
t <sub>WH(R)</sub>	MR Pulse Width	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	400 200 150	170 75 50		ns
C <sub>I</sub>	Average Input Capacitance	Any Input		5.0	7.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)			100		pF

**Note 4:** AC Parameters are guaranteed by DC correlated testing.

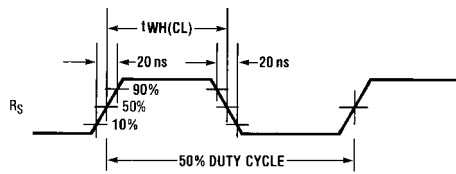
**Note 5:** C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note: AN-90.

### Test Circuits and Waveforms

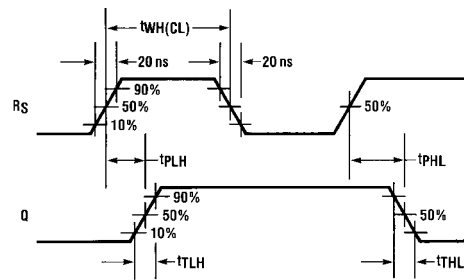
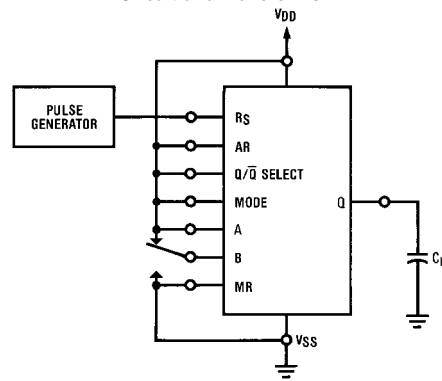
Power Dissipation Test Circuit and Waveforms



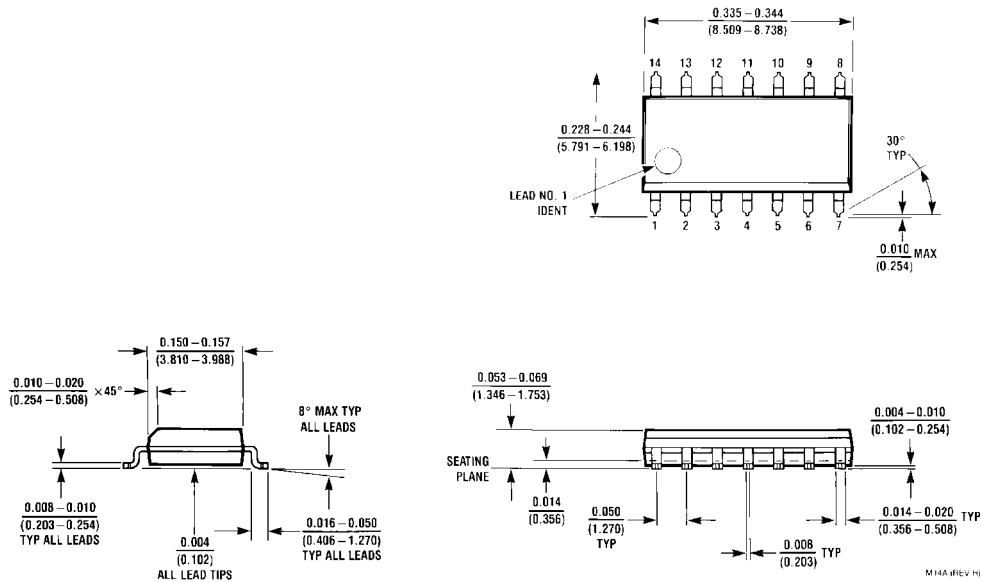
(R<sub>TC</sub> and C<sub>TC</sub> outputs are left open)



Switching Time Test Circuit and Waveforms

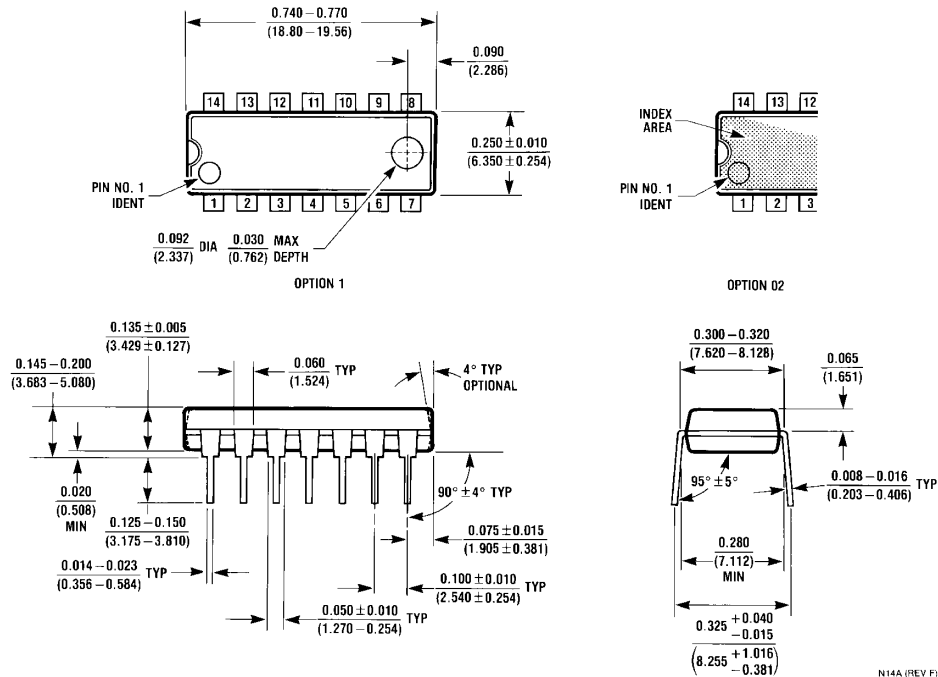


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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