1 Characteristics

Table 1. **Absolute ratings (limiting values)**

Symbol	Parameter	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. **Electrical characteristics (T_{amb} = 25 °C)**

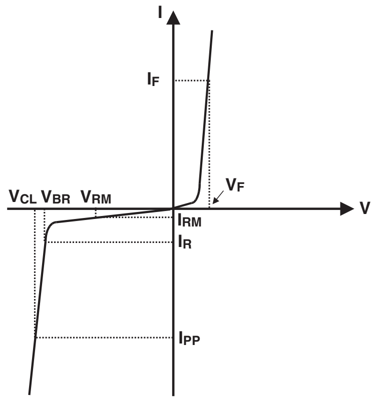
<table>
<tr><th>Symbol</th><th>Parameters</th><td colspan="4" rowspan="9">
</td></tr>
<tr><td>V_{BR}</td><td>Breakdown voltage</td></tr>
<tr><td>I_{RM}</td><td>Leakage current @ V_{RM}</td></tr>
<tr><td>V_{RM}</td><td>Stand-off voltage</td></tr>
<tr><td>V_{CL}</td><td>Clamping voltage</td></tr>
<tr><td>R_d</td><td>Dynamic impedance</td></tr>
<tr><td>I_{PP}</td><td>Peak pulse current</td></tr>
<tr><td>$R_{I/O}$</td><td>Series resistance between input and output</td></tr>
<tr><td>C_{line}</td><td>Input capacitance per line</td></tr>
<tr><th>Symbol</th><th>Test conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>V_{BR}</td><td>I_R = 1 mA</td><td>6</td><td></td><td></td><td>V</td></tr>
<tr><td>I_{RM}</td><td>V_{RM} = 3 V per line</td><td></td><td></td><td>1</td><td>µA</td></tr>
<tr><td>R_d</td><td></td><td></td><td>1.5</td><td></td><td>Ω</td></tr>
<tr><td>R_1</td><td></td><td>95</td><td>100</td><td>105</td><td>Ω</td></tr>
<tr><td>R_2</td><td></td><td>44.65</td><td>47</td><td>49.35</td><td>Ω</td></tr>
<tr><td>R_3</td><td></td><td>95</td><td>100</td><td>105</td><td>Ω</td></tr>
<tr><td>C_{line}</td><td>@ 0 V</td><td></td><td></td><td>35</td><td>pF</td></tr>
</table>

Figure 3. S21 (dB) attenuation measurement

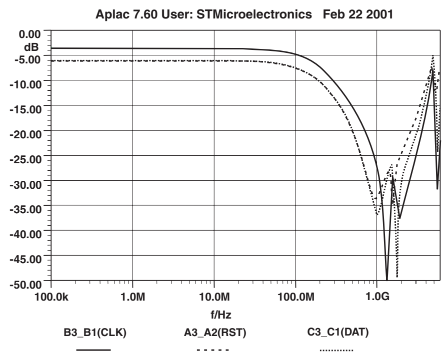


Figure 4. Analog crosstalk measurement

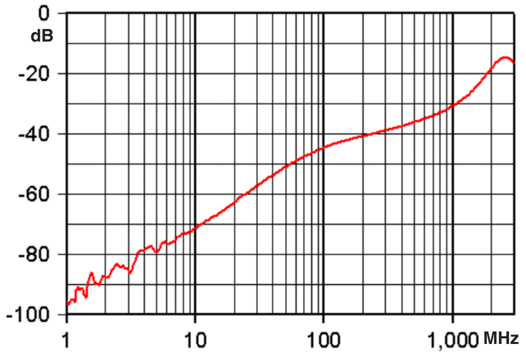


Figure 5. Digital crosstalk measurement

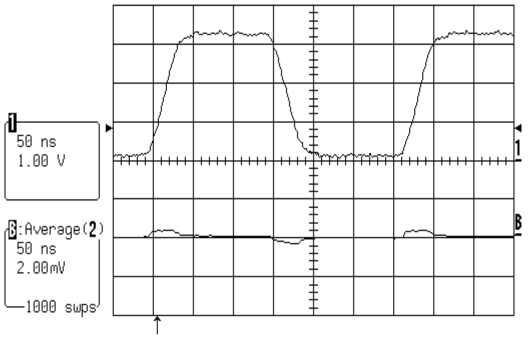


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (Vin) and on one output (Vout)

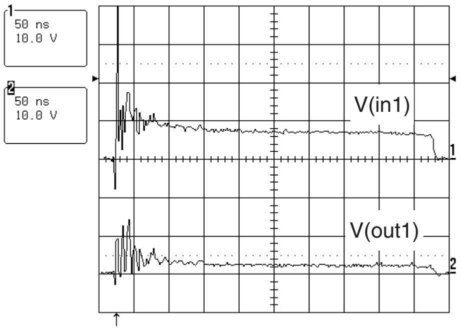


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (Vin) and on one output (Vout)

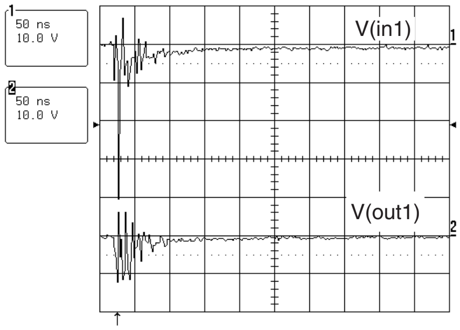
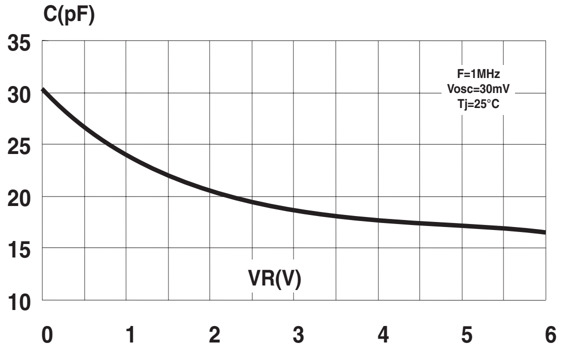
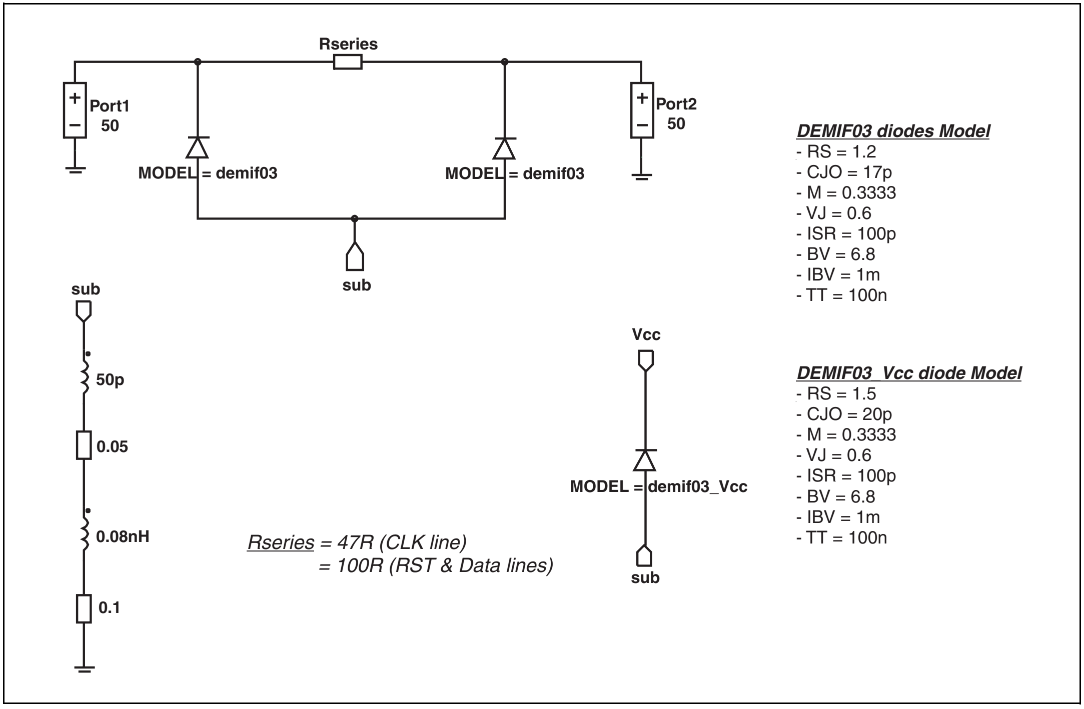


Figure 8. Line capacitance versus applied voltage (typical)



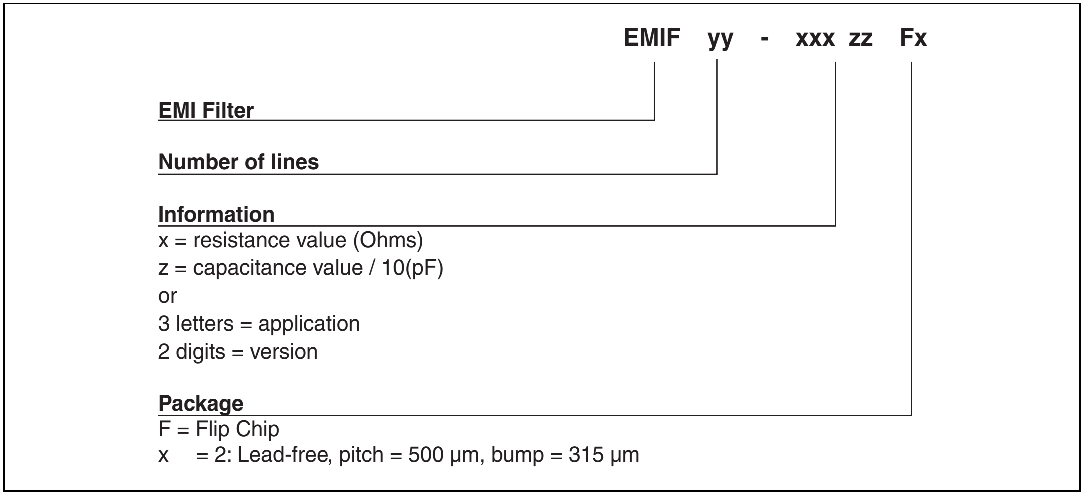
2 Application information

Figure 9. Aplac model



3 Ordering information scheme

Figure 10. Ordering information scheme



EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip Chip
x = 2: Lead-free, pitch = 500 µm, bump = 315 µm

4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 11. Package dimensions

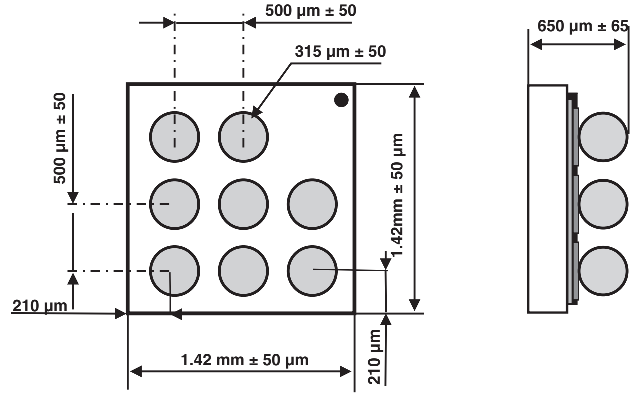


Figure 12. Footprint

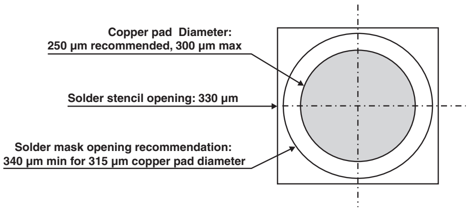


Figure 13. Marking

Dot, ST logo
xx = marking
z = manufacturing location
yww = datecode
(y = year
ww = week)

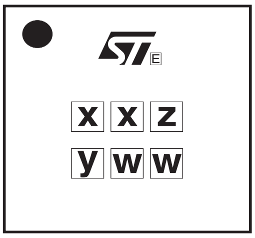
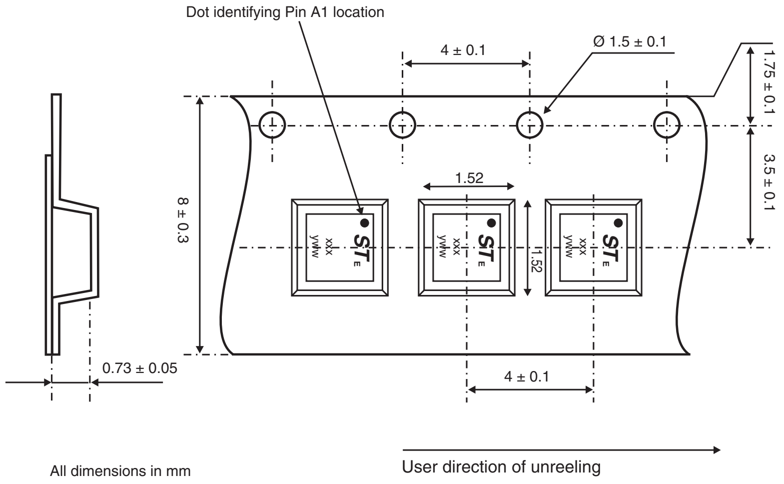


Figure 14. Flip Chip tape and reel specification



5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM01F2	FC	Flip Chip	2.9 mg	5000	Tape and reel 7”

Note: *More information is available in the application notes:*

AN1235:"Flip Chip: Package description and recommendations for use"

AN1751: “EMI filters: Recommendations and measurements”

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
08-Oct-2004	1	Initial release.
13-Dec-2004	2	*Table 3.* on page 6: Flip Chip weight corrected from 3.3 mg to 2.9 mg.
28-Apr-2008	3	Updated ECOPACK statement. Updated *Figure 10*, *Figure 11* and *Figure 14.* Reformatted to current standards.

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