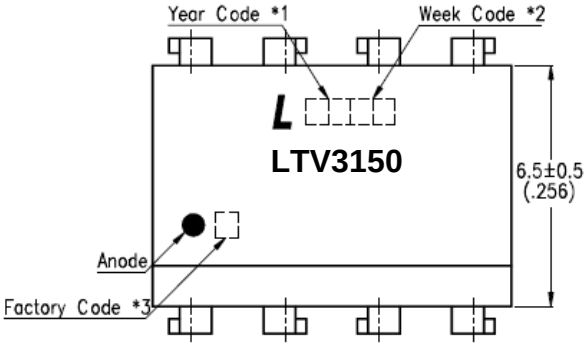
Ordering Information

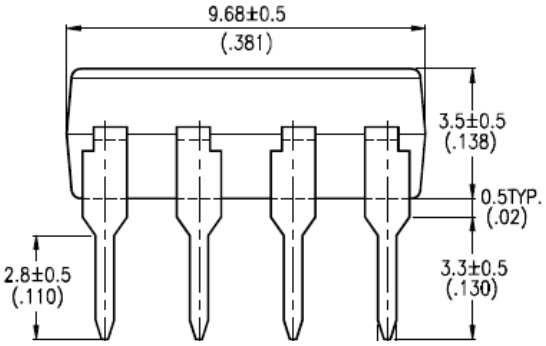
Part	Option	Remarks
LTV-3150		DIP-8
	M	Wide Lead Spacing, DIP-8
	S	Surface Mount, SMD-8
	S-TA	Surface Mount, SMD-8, Pin 1 location at lower right of the reel
	S-TA1	Surface Mount, SMD-8, Pin 1 location at upper left of the reel

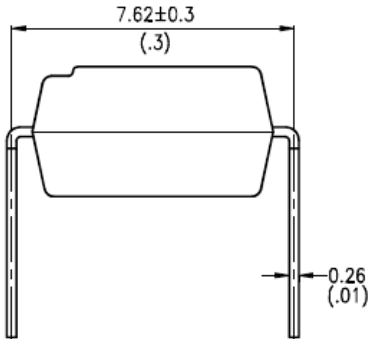
Package Dimensions

8-pin DIP Package (LTV-3150)



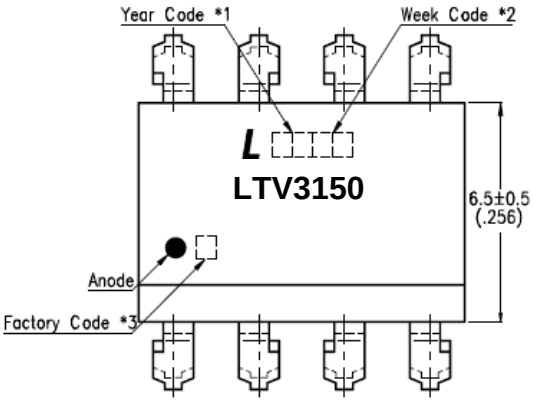
*1. Year date code.
*2. 2-digit work week.
*3. Factory identification mark
(Y : Thailand).
Dimensions are in Millimeters and (Inches).



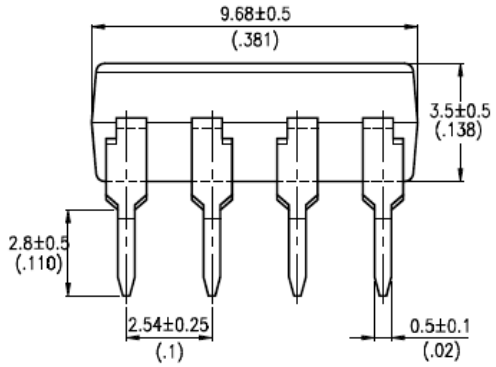


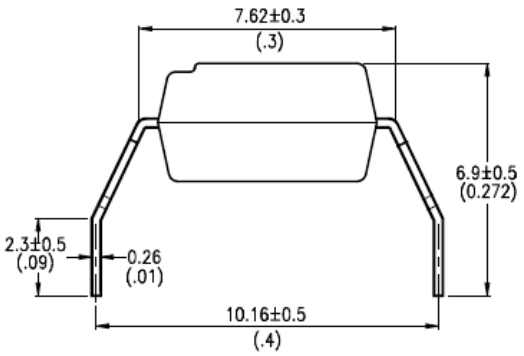
Package Dimensions

8-pin DIP Wide Lead Spacing Package (LTV-3150M)



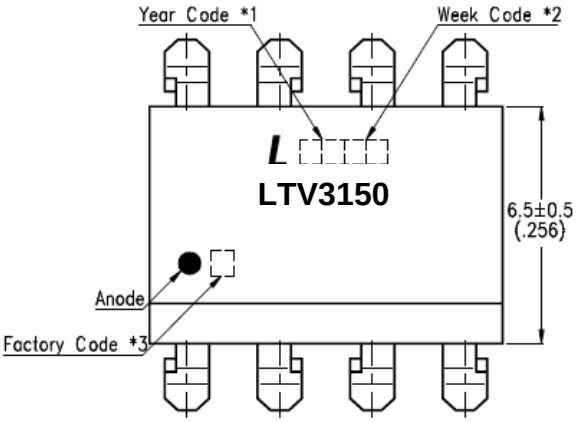
*1. Year date code.
*2. 2-digit work week.
*3. Factory identification mark
(Y : Thailand).
Dimensions are in Millimeters and (Inches).



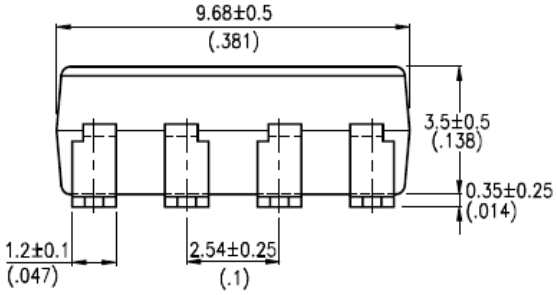


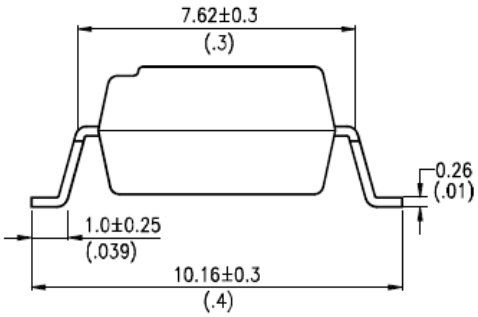
Package Dimensions

8-pin DIP Surface Mount Package (LTV-3150S)



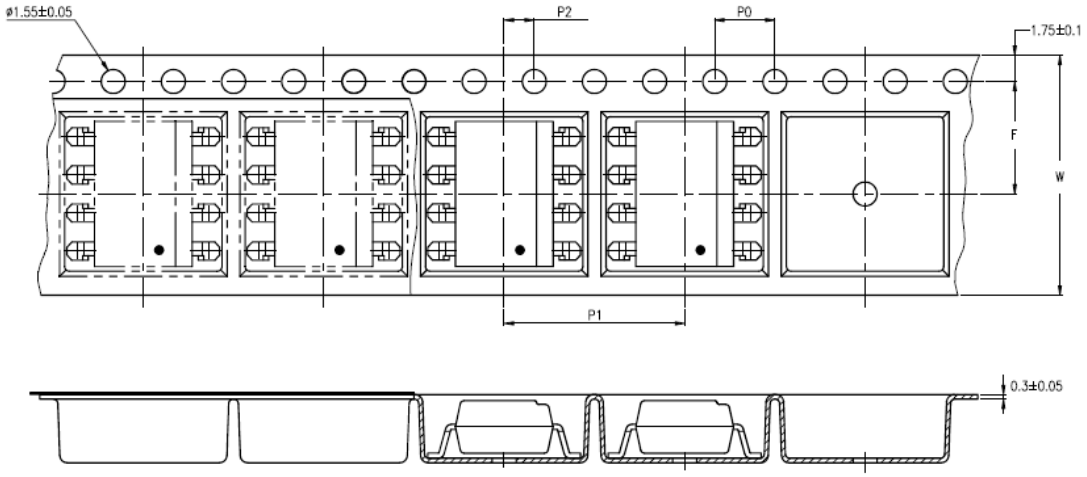
*1. Year date code.
*2. 2-digit work week.
*3. Factory identification mark
(Y : Thailand).
Dimensions are in Millimeters and (Inches).



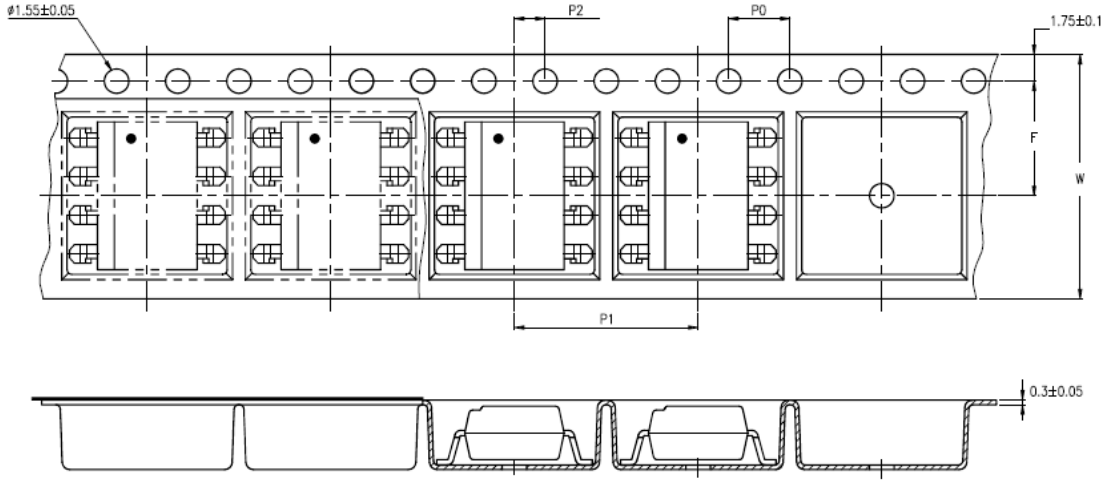


Taping Dimensions

LTV-3150S-TA

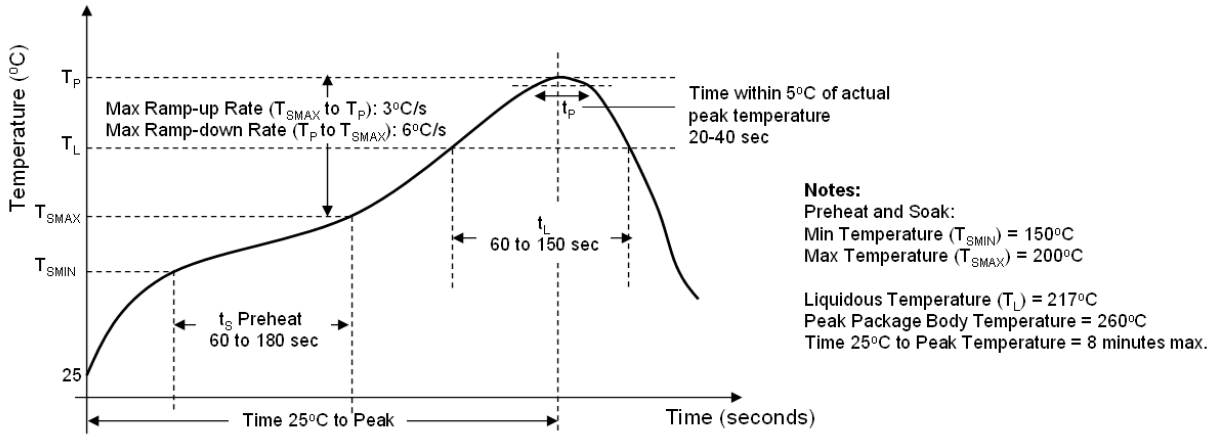


LTV-3150S-TA1



Description	Symbol	Dimensions in millimeters (inches)
Tape wide	W	16 ± 0.3 (.63)
Pitch of sprocket holes	P0	4 ± 0.1 (.15)
Distance of compartment	F P2	7.5 ± 0.1 (.295) 2 ± 0.1 (.079)
Distance of compartment to compartment	P1	12 ± 0.1 (.472)

Recommended Lead Free Reflow Profile



Notes:
Preheat and Soak:
Min Temperature (T_{SMIN}) = 150°C
Max Temperature (T_{SMAX}) = 200°C

Liquidous Temperature (T_L) = 217°C
Peak Package Body Temperature = 260°C
Time 25°C to Peak Temperature = 8 minutes max.

Absolute Maximum Ratings

Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_{ST}	-55	125	°C
Operating Temperature	T_A	-40	100	°C
Isolation Voltage	V_{ISO}	5000		V_{RMS}
Supply Voltage	V_{CC}	0	35	V
Lead Solder Temperature (9)	T_{SOL}		260	°C
Input				
Average Forward Input Current	$I_{F(AVG)}$		25	mA
Reverse Input Voltage	V_R		5	V
Peak Transient Input Current (<1 μs pulse width, 300 pps)	$I_{F(TRAN)}$		1	A
Input Current (Rise/Fall Time)	$t_{r(IN)}$ /$t_{f(IN)}$		500	ns
Input Power Dissipation (10)	P_I		45	mW
Output				
"High" Peak Output Current (1)	$I_{OH(PEAK)}$	0.6		A
"Low" Peak Output Current (1)	$I_{OL(PEAK)}$	-0.6		A
Output Voltage	V_O		V_{CC}	V
Output Power Dissipation (11)	P_O		250	mW
Total Power Dissipation	P_T		295	mW

8) At least a 0.1uF or bigger bypass capacitor must be connected across pin 8 and pin 5. Failure to provide the bypass may impair the switching property.

9) 260°C for 10 seconds. Refer to Lead Free Reflow Profile

10) Derating Linearly above 70°C free-air temperature at a rate of 0.47 mW/°C

11) Derating Linearly above 70°C free-air temperature at a rate of 4.8mW/°C

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	T_A	-40	100	^oC
Supply Voltage	V_{CC}	15	30	V
Input Current (ON)	$I_{FL(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V

Electrical Specifications

Parameters	Test Condition	Symbol	Min	Typ	Max	Units	Figure
Input							
Input Forward Voltage	I_F = 10mA	V_F	1.2	1.37	1.8	V	15
Input Forward Voltage Temperature Coefficient	I_F = 10mA	$\Delta V_F / \Delta T$		-1.237		mV/^{O}C	
Input Reverse Voltage	I_R = 10μA	BV_R	5			V	
Input Threshold Current (Low to High)	V_O > 5V, I_O = 0A	I_{FLH}			5	mA	9,16,21
Input Threshold Voltage (High to Low)	V_O < 5V, I_O = 0A	V_{FHL}	0.8			V	
Input Capacitance	f = 1 MHz, V_F = 0 V	C_{IN}		33		pF	
Output							
High Level Supply Current	Output Open, I_F = 10 to 16 mA	I_{CCH}		1	3.5	mA	7,8
Low Level Supply Current	Output Open, V_F = -3 to +0.8 V	I_{CCL}		1	3.5	mA	7,8
High level output current (1)	V_O = (V_{CC} - 6 V)	I_{OH}	-0.6			A	2,3,19
Low level output current (1)	V_O = (V_{EE} + 6 V)	I_{OL}	0.6			A	5,6,20
High level output voltage	I_F = 10mA, I_O = -100mA	V_{OH}	V_{CC} - 1			V	1,3,17
Low level output voltage	I_F = 0mA, I_O = 100mA	V_{OL}			V_{EE} + 1	V	4,6,18
UVLO Threshold	V_O > 5V, I_F = 10 mA	V_{UVLO+}	11	12.3	13.5	V	22
	V_O < 5V, I_F = 10 mA	V_{UVLO-}	9.5	10.7	12	V	
UVLO Hysteresis		$UVLO_{HYS}$		1.6		V	

Specified over recommended operating conditions.

All Typical values at TA = 25℃ and V_{CC} = 30 V, unless otherwise specified.

Switching Specifications

Parameter	Test Condition	Symbol	Min	Typ	Max	Units	Figure
Propagation Delay Time to High Output Level	I_F = 7 to 16 mA, Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%	T_{PLH}	0.1	0.3	0.5	µs	10,11, 12,13, 14,23
Propagation Delay Time to Low Output Level		T_{PHL}	0.1	0.3	0.5	µs	
Pulse Width Distortion (7)		PWD			0.3	µs	
Propagation delay difference between any two parts or channels (4)		PDD	-0.30		0.35	µs	
Output Rise Time (10 to 90%)		Tr		75		ns	23
Output Fall Time (90 to 10%)		Tf		50		ns	
UVLO turn on delay	I_F = 10 mA, V_O > 5 V	$T_{UVLO\ ON}$		2		µs	
UVLO turn off delay	I_F = 10 mA, V_O < 5 V	$T_{UVLO\ OFF}$		0.3		µs	
Common mode transient immunity at high level output (5)	I_F = 7 to 16 mA, V_{CM} = 1500 V, TA = 25℃, V_{CC} = 30 V	CMH	15	25		kV/µs	24
Common mode transient immunity at low level output (6)	V_F = 0 V, V_{CM} = 1500 V, TA = 25℃, V_{CC} = 30 V	CML	15	25		kV/µs	

Specified over recommended operating conditions.

All Typical values at TA = 25℃ and V_{CC} = 30 V, unless otherwise specified.

Isolation Characteristics

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
Withstand Insulation Test Voltage (2) (3)	RH ≤ 40-60%, t = 1min, T_A = 25°C	V_{ISO}	5000			V
Input-Output Resistance (2)	V_{I-O} = 500V DC	R_{I-O}		10^{12}		Ω
Input-Output Capacitance (2)	f = 1MHz, T_A = 25°C	C_{I-O}		0.92		pF

Notes:

1) Maximum pulse width = 10us, maximum duty cycle = 0.2%.
2) Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
3) According to UL1577, each optocoupler is tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 6 uA).
4) The difference between T_{PHL} and T_{PLH} between any two LTV-3150 parts under same test conditions.
5) Common mode transient immunity in high stage is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, Vcm, to assure that the output will remain high.
6) Common mode transient immunity in low stage is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain low.
7) Pulse Width Distortion is defined as $|T_{PHL} - T_{PLH}|$ for any given device.

Typical Performance Curves

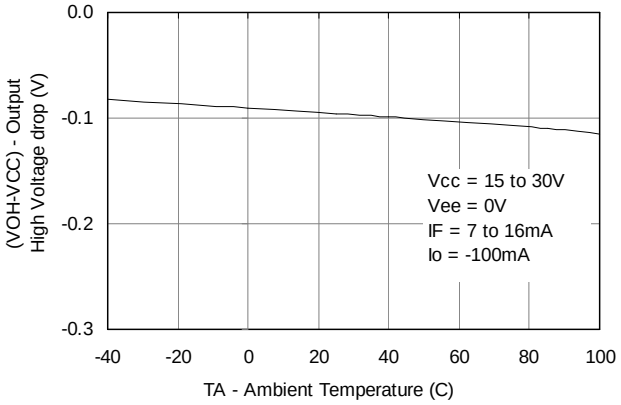


Figure 1: Output High Voltage drop vs Temperature

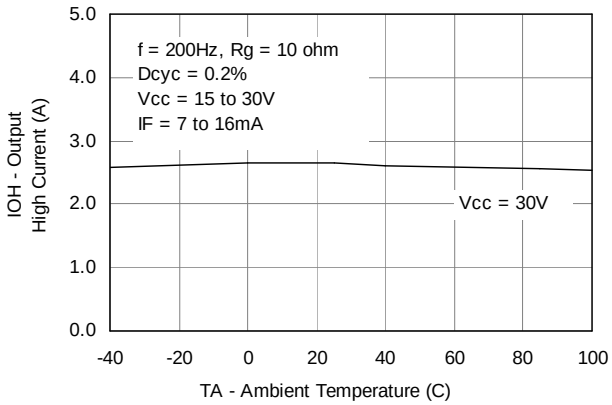


Figure 2: Output High Current vs Temperature

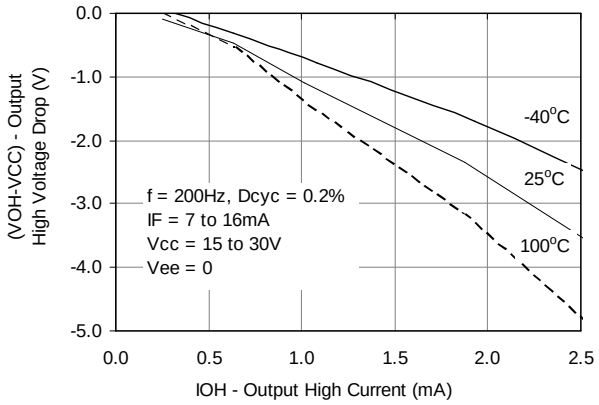


Figure 3: Output High Voltage drop vs High Current

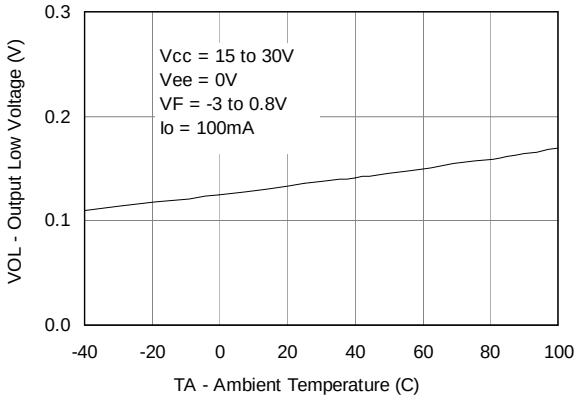


Figure 4: Output Low Voltage vs Temperature

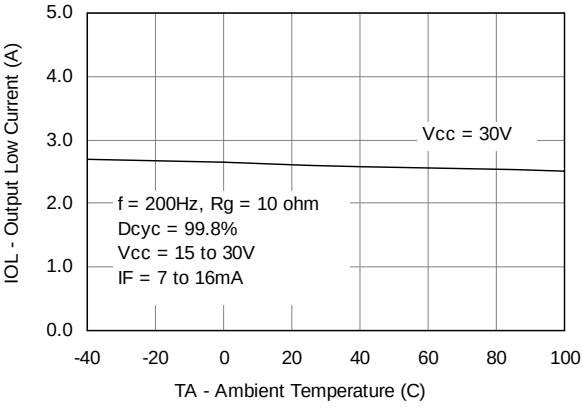


Figure 5: Output Low Current vs Temperature

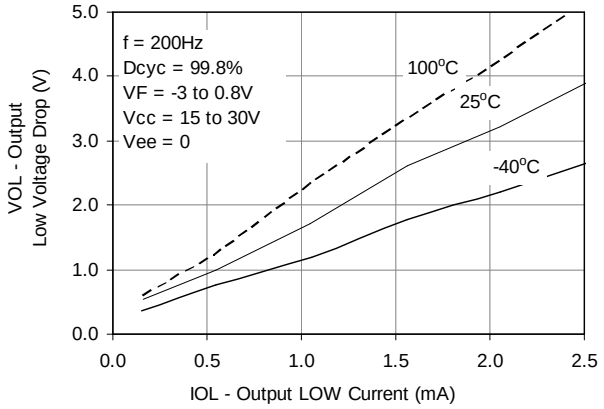


Figure 6: Output Low Voltage vs Low Current

Typical Performance Curves (Continued)

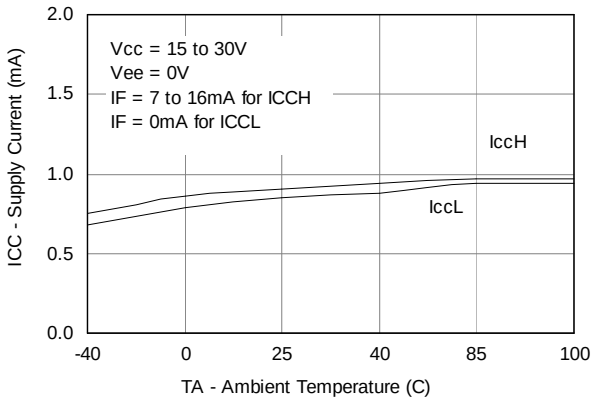


Figure 7: Supply Current vs Temperature

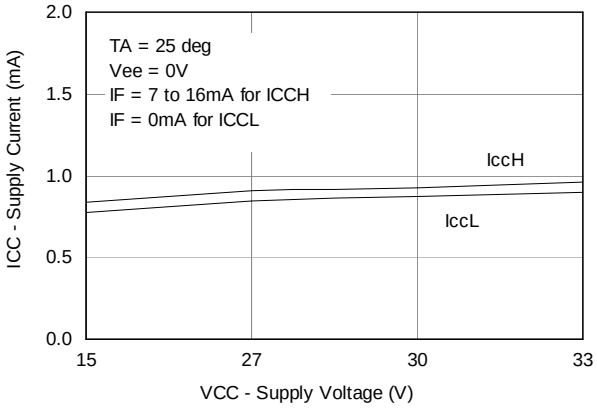


Figure 8: Supply Current vs Supply Voltage

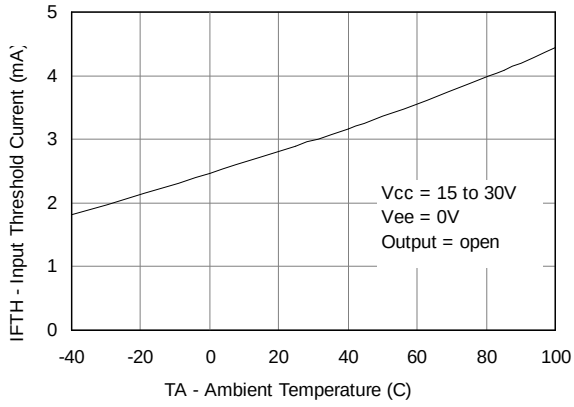


Figure 9: Low to High Threshold Current vs Temperature

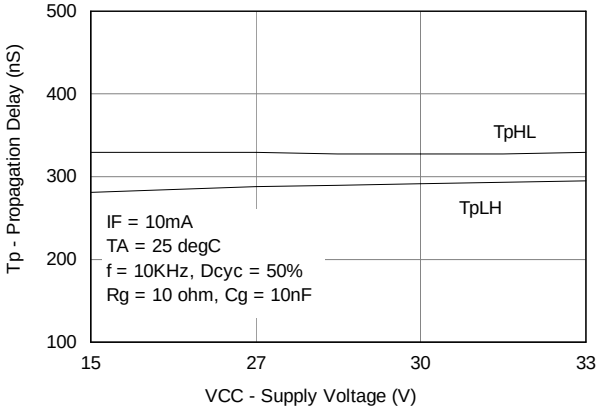


Figure 10: Propagation vs Vcc

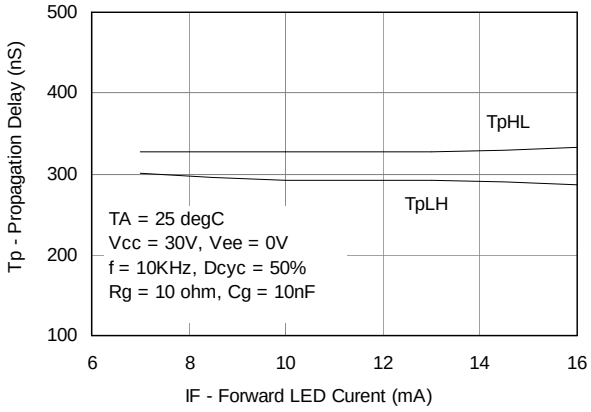


Figure 11: Propagation vs Input Current

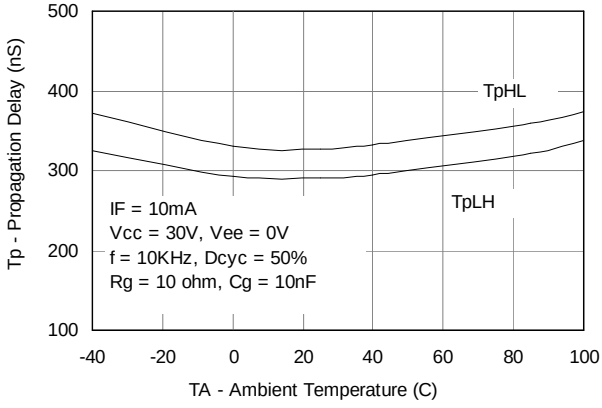


Figure 12: Propagation vs Temperature

Typical Performance Curves (Continued)

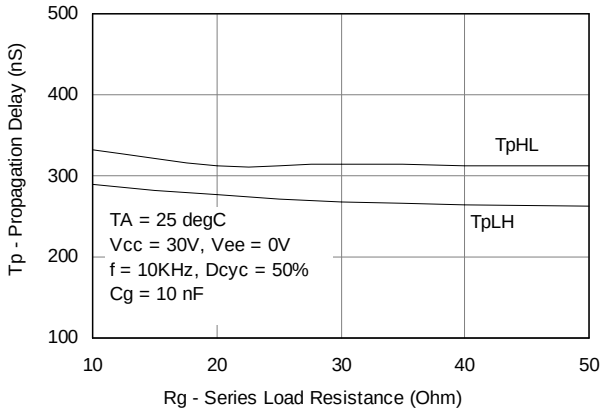


Figure 13: Propagation vs Series Load Resistance

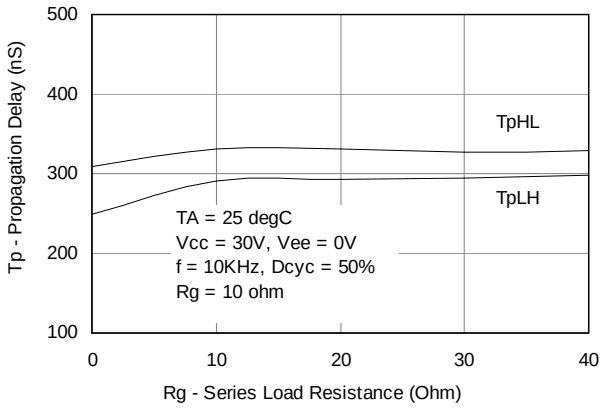


Figure 14: Propagation vs Load Capacitance (nF)

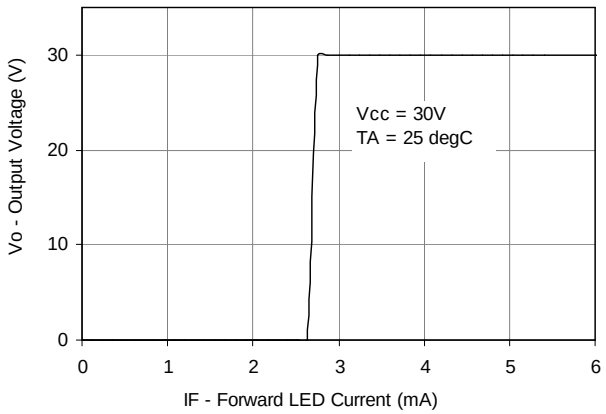


Figure 16: Transfer Characteristics

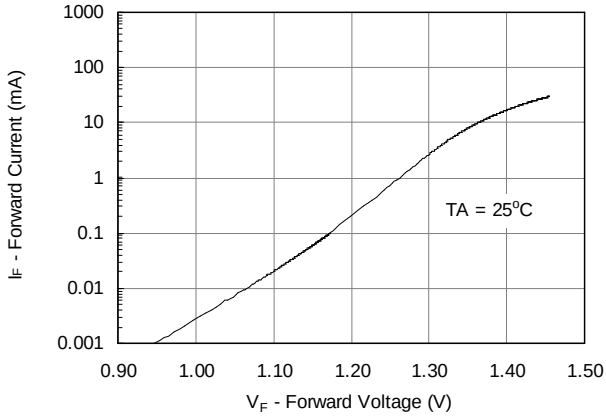


Figure 15: Input Current vs Forward Voltage

Test Circuit

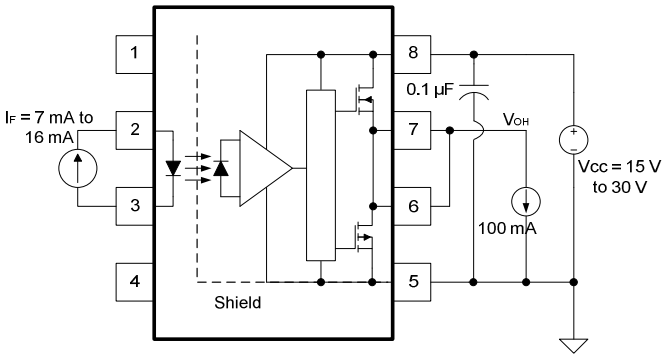


Figure 17 : V_{OH} Test Circuit

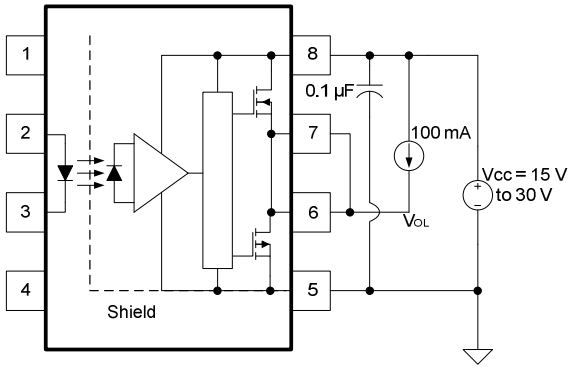


Figure 18 : V_{OL} Test Circuit

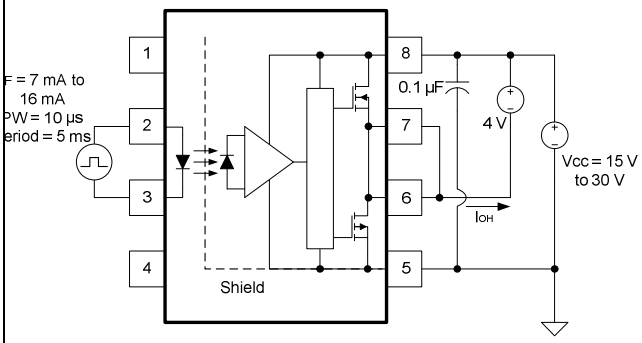


Figure 19 : I_{OH} Test Circuit

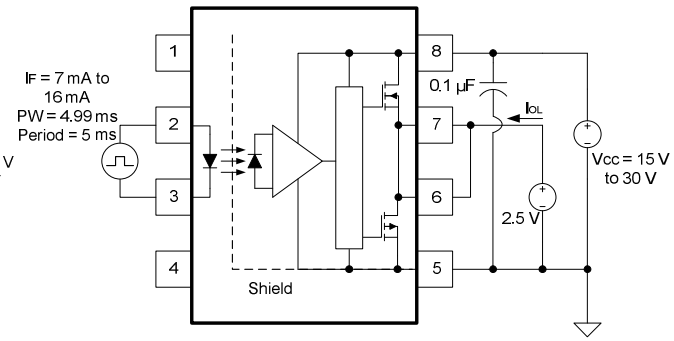


Figure 20 : I_{OL} Test Circuit

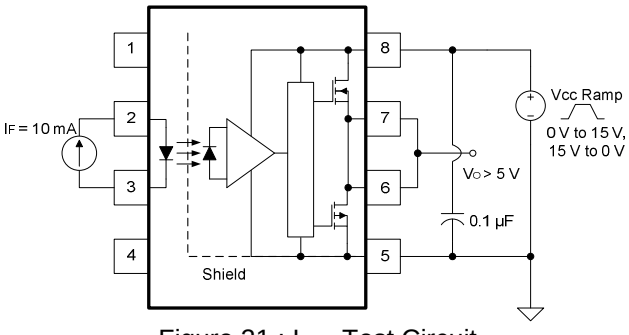


Figure 21 : I_{FLH} Test Circuit

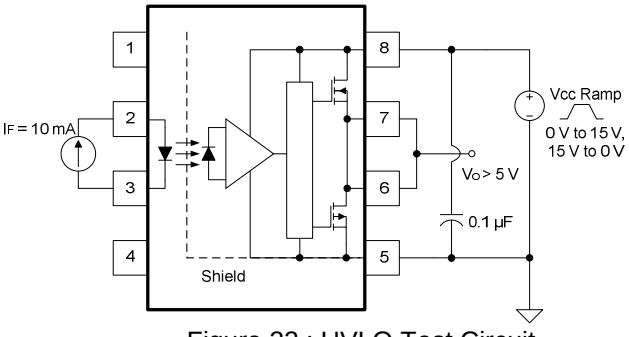


Figure 22 : UVLO Test Circuit

Test Circuit (Continued)

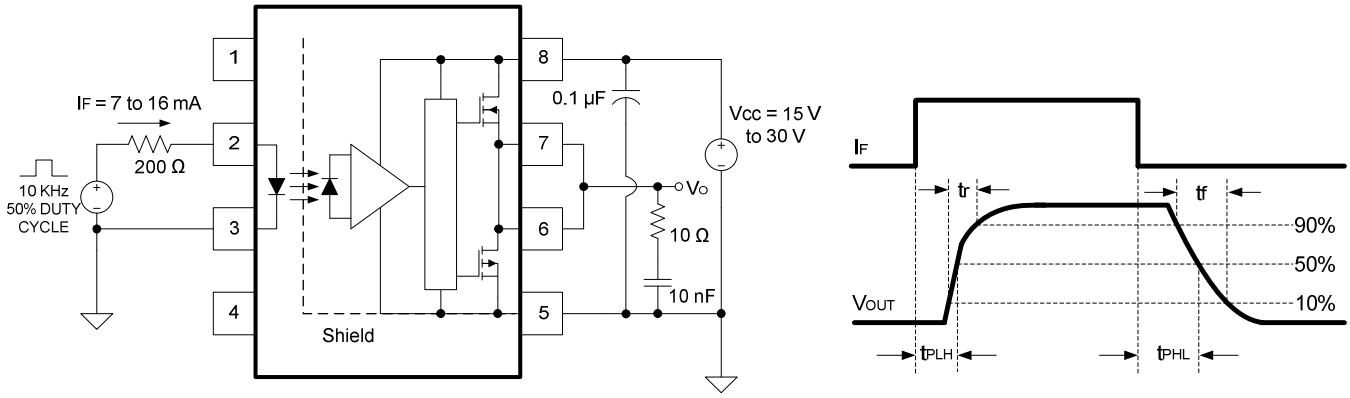


Figure 23 : tr, tf, t_{PLH} and t_{PHL} Test Circuit and Waveforms

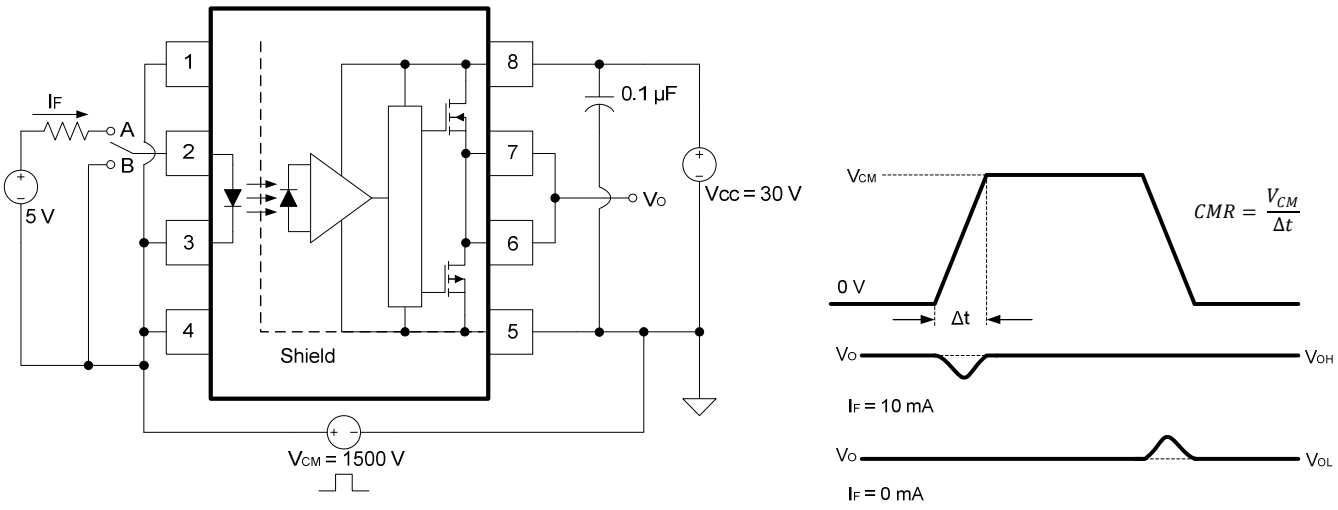


Figure 24 : CMR Test Circuit and Waveforms

Notice

Specifications of the products displayed herein are subject to change without notice.

The products shown in this publication are designed for the general use in electronic applications such as office automation equipment, communications devices, audio/visual equipment, electrical instrumentation and application. For equipment/devices where high reliability or safety is required, such as space applications, nuclear power control equipment, medical equipment, etc, please contact our sales representatives.

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