1.2MHz Low-Cost, High-Performance Chargers

ABSOLUTE MAXIMUM RATINGS

DCIN, CSSP, CSSN, BATT, CSIN, CSIP, $\overline{ACOK}$, LX to AGND .....-0.3V to +30V
BST to LDO.....-0.3V to +30V
CSIP to CSIN, CSSP to CSSN ..... -0.3V to +0.3V
IINP, FB, ACIN to AGND.....-0.3V to (V_{AA} + 0.3V)
V_{AA}, LDO, ISET, VCTL, CC to AGND .....-0.3V to +6V
DHI to LX .....-0.3V to (BST + 0.3V)
BST to LX.....-0.3V to +6V
DLO to PGND .....-0.3V to (LDO + 0.3V)
PGND to AGND ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 16.9mW/°C above +70°C)....1349.1mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, V_{VCTL} = V_{AA}, V_{ISET} = 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION						
Battery Regulation-Voltage Accuracy	2 cells, V_{VCTL} = GND (for MAX17006)		8.3664	8.40	8.4336	V
	3 cells, V_{VCTL} = V_{AA} (for MAX17005 and MAX17006)		12.549	12.60	12.651	
	4 cells, V_{VCTL} = GND (for MAX17005)		16.733	16.80	16.867	
	FB accuracy using FB divider (for MAX17015) (Note 1)		2.0916	2.1	2.1084	
FB Input Bias Curent			-1		+1	µA
VCTL Range	2 cells (for MAX17006), 4 cells (for MAX17005)		0.0		V_{AA}/2 -0.2	V
	3 cells (for MAX17005 and MAX17006)		V_{AA}/2 +0.2		V_{AA}	
VCTL Gain	V_{CELL}/V_{VCTL}		5.85	6	6.15	V/V
VCTL Input Bias Current	V_{VCTL} = GND and VCTL = V_{AA}		-1		+1	µA
CHARGE-CURRENT REGULATION						
ISET Range			0.0		V_{AA}/2	V
ISET Full-Scale Setting	ISET = 1.4V			80		mV
	ISET = 99.9% duty cycle			60		
Full-Charge Current Accuracy (CSIP to CSIN)	V_{BATT} = 1V to 16.8V	V_{ISET} = V_{AA}/4 or ISET = 99.9% duty cycle	58.2	60	61.8	mV
			-3		+3	%
		V_{ISET} = V_{AA}/6 or ISET = 66.7% duty cycle	38.2	40	41.8	mV
			-4.5		+4.5	%
Trickle Charge-Current Accuracy		V_{ISET} = V_{AA}/80 or ISET = 5% duty cycle	1.4	3	4.6	mV
			-52		+52	%
Charge-Current Gain Error	Based on V_{ISET} = V_{VAA}/4 and V_{ISET} = V_{VAA}/80		-2		+2	%
Charge-Current Offset Error	Based on V_{ISET} = V_{VAA}/4 and V_{ISET} = V_{VAA}/80		-1.4		+1.4	mV
BATT/CSIP/CSIN Input Voltage Range			0		24	V
ISET Power-Down Mode Threshold	ISET falling		21	26	31	mV
	ISET rising		33	40	47	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, V_{VCTL} = V_{AA}, V_{ISET} = 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ISET Input Bias Current	V_{ISET} = 3V		-0.2		+0.2	µA
	CSSN = BATT, V_{ISET} = 5V		-0.2		+0.2	
ISET PWM Threshold	Rising				2.4	V
	Falling		0.8			
ISET Frequency			0.128		500	kHz
ISET Effective Resolution	f_{PWM} = 3.2MHz			8		Bits
INPUT-CURRENT REGULATION						
Input Current-Limit Threshold	V_{CSSP} - V_{CSSN}		58.5	60	61.5	mV
			-2.5		+2.5	%
CSSN Input Bias Current	Adapter present		-0.1		+0.1	µA
CSSP/CSSN Input-Voltage Range			8.0		26.0	V
IINP Transconductance	V_{CSSP} - V_{CSSN} = 60mV		2.66	2.8	2.94	µA/mV
IINP Accuracy	V_{CSSP} - V_{CSSN} = 60mV, V_{IINP} = 0V to 4.5V		-2.5		+2.5	%
	V_{CSSP} - V_{CSSN} = 35mV		-2.5		+2.5	
SUPPLY AND LINEAR REGULATOR						
DCIN Input Voltage Range			8		26	V
DCIN Undervoltage-Lockout (UVLO) Trip-Point	DCIN falling		7.9	8.1		V
	DCIN rising			8.7	8.9	
DCIN + CSSP + CSSN Quiescent Current	Adapter present (Note 2)			3	6	mA
	Adapter absent (Note 2)			30	50	µA
BATT + CSIP + CSIN + LX Input Current	V_{BATT} = 16.8V	Adapter absent (Note 2)		10	20	µA
		Charger shutdown (Note 2)		10	20	
	V_{BATT} = 2V to 19V, adapter present (Note 2)			200	500	
LDO Output Voltage	8.0V < V_{DCIN} < 26V, no load		5.15	5.35	5.55	V
LDO Load Regulation	0 < I_{LDO} < 40mA			100	200	mV
LDO UVLO Threshold			3.2	4.1	5.0	V
REFERENCES						
V_{AA} Output Voltage	I_{VAA} = 50µA		4.18	4.20	4.22	V
V_{AA} UVLO Threshold	V_{AA} falling			3.1	3.9	V
ACIN						
ACIN Threshold			2.058	2.1	2.142	V
ACIN Threshold Hysteresis			10	20	30	mV
ACIN Input Bias Current			-1		+1	µA
$\overline{ACOK}$						
$\overline{ACOK}$ Sink Current	$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 1.5V		6			mA
$\overline{ACOK}$ Leakage Current	$V_{\overline{ACOK}}$ = 5.5V, V_{ACIN} = 2.5V				1	µA

1.2MHz Low-Cost, High-Performance Chargers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, V_{VCTL} = V_{AA}, V_{ISET} = 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING REGULATOR					
DHI Off-Time K Factor	V_{DCIN} = 19V, V_{BATT} = 10V	0.029	0.030	0.041	µs/V
Sense Voltage for Minimum Discontinuous Mode Ripple Current	V_{CSIP} - V_{CSIN}		10		mV
Zero-Crossing Comparator Threshold	V_{CSIP} - V_{CSIN}		10		mV
Cycle-by-Cycle Current-Limit Sense Voltage	V_{CSIP} - V_{CSIN}	105	110	115	mV
DHI Resistance High	I_{DLO} = 10mA		1.5	3	Ω
DHI Resistance Low	I_{DLO} = -10mA		0.8	1.75	Ω
DLO Resistance High	I_{DLO} = 10mA		3	6	Ω
DLO Resistance Low	I_{DLO} = -10mA		3	7	Ω
ADAPTER DETECTION					
Adapter Absence-Detect Threshold	V_{DCIN} - V_{BATT}, V_{DCIN} falling	+70	+120	+170	mV
Adapter Detect Threshold	V_{DCIN} - V_{BATT}, V_{DCIN} rising	+360	+420	+580	mV
Adapter Switch Charge-Pump Frequency	Charger Shutdown	180	200	220	Hz
Adapter Switch Charge-Pump Refresh Pulse	DLO	0.04	0.1	0.20	µs
	DHI	0.07	0.15	0.30	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, V_{VCTL} = V_{AA}, V_{ISET} = 1V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION					
Battery Regulation-Voltage Accuracy	2 cells, V_{VCTL} = GND (for MAX17006)	8.366		8.433	V
	3 cells, V_{VCTL} = V_{AA} (for MAX17005 and MAX17006)	12.549		12.651	
	4 cells, V_{VCTL} = GND (for MAX17005)	16.73		16.86	
	FB accuracy using FB divider (for MAX17015) (Note 1)	2.091		2.108	
VCTL Range	2 cells (for MAX17006), 4 cells (for MAX17005)	0.0		V_{AA}/2 - 0.2	V
	3 cells (for MAX17005 and MAX17006)	V_{AA}/2 + 0.2		V_{AA}	
VCTL Gain	V_{CELL}/V_{VCTL}	5.85		6.15	V/V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, V_{VCTL} = V_{AA}, V_{ISET} = 1V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-CURRENT REGULATION						
ISET Range			0.0		V_{AA}/2	V
Full Charge-Current Accuracy (CSIP to CSIN)	V_{BATT} = 1V to 16.8V	V_{ISET} = V_{AA}/4 or ISET = 99.9% duty cycle	57.5		62.5	mV
			-4.2		+4.2	%
		V_{ISET} = V_{AA}/6 or ISET = 66.7% duty cycle	38		42	mV
			-5		+5	%
Trickle Charge-Current Accuracy		V_{ISET} = V_{AA}/80 or ISET = 5% duty cycle	1.4		4.6	mV
			-52		+52	%
Charge-Current Gain Error	Based on V_{ISET} = V_{VAA}/4 and V_{ISET} = V_{VAA}/80		-2		+2	%
Charge-Current Offset Error	Based on V_{ISET} = V_{VAA}/4 and V_{ISET} = V_{VAA}/80		-1.4		+1.4	mV
BATT/CSIP/CSIN Input Voltage Range			0		24	V
ISET Power-Down Mode Threshold	ISET falling		21		31	mV
	ISET rising		33		47	
ISET PWM Threshold	Rising				2.4	V
	Falling		0.8			
ISET Frequency			0.128		500	kHz
INPUT-CURRENT REGULATION						
Input Current-Limit Threshold	V_{CSSP} - V_{CSSN}		58.2		61.8	mV
			-3		+3	%
CSSN Input Bias Current	Adapter present		-2		+2	µA
CSSP/CSSN Input-Voltage Range			8.0		26.0	V
IINP Transconductance	V_{CSSP} - V_{CSSN} = 60mV		2.66		2.94	µA/mV
IINP Accuracy	V_{CSSP} - V_{CSSN} = 60mV, V_{IINP} = 0V to 4.5V		-2.5		+2.5	%
	V_{CSSP} - V_{CSSN} = 35mV		-2.5		+2.5	
SUPPLY AND LINEAR REGULATOR						
DCIN Input-Voltage Range			8		26	V
DCIN UVLO Trip-Point	DCIN falling		7.9			V
	DCIN rising				8.9	
DCIN + CSSP + CSSN Quiescent Current	Adapter present (Note 2)				6	mA
	Adapter absent (Note 2)				50	µA
BATT + CSIP + CSIN + LX Input Current	V_{BATT} = 16.8V	Adapter absent (Note 2)			20	µA
		Charger shutdown (Note 2)			20	
	V_{BATT} = 2V to 19V, adapter present (Note 2)				500	
LDO Output Voltage	8.0V < V_{DCIN} < 26V, no load		5.15		5.55	V
LDO Load Regulation	0 < I_{LDO} < 40mA				200	mV
LDO UVLO Threshold			3.2		5.0	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, V_{VCTL} = V_{AA}, V_{ISET} = 1V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCES					
VAA Output Voltage	I_{VAA} = 50µA	4.18		4.22	V
VAA UVLO Threshold	V_{AA} falling			3.9	V
ACIN					
ACIN Threshold		2.058		2.142	V
ACIN Threshold Hysteresis		10		30	mV
$\overline{ACOK}$					
$\overline{ACOK}$ Sink Current	$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 1.5V	6			mA
SWITCHING REGULATOR					
DHI Off-Time K Factor	V_{DCIN} = 19V, V_{BATT} = 10V	0.029		0.041	µs/V
Cycle-by-Cycle Current-Limit Sense Voltage	V_{CSIP} - V_{CSIN}	105		115	mV
DHI Resistance High	I_{DLO} = 10mA			3	Ω
DHI Resistance Low	I_{DLO} = -10mA			1.75	Ω
DLO Resistance High	I_{DLO} = 10mA			6	Ω
DLO Resistance Low	I_{DLO} = -10mA			7	Ω
ADAPTER DETECTION					
Adapter Absence-Detect Threshold	V_{DCIN} - V_{BATT}, V_{DCIN} falling	+70		+170	mV
Adapter Detect Threshold	V_{DCIN} - V_{BATT}, V_{DCIN} rising	+320		+620	mV
Adapter Switch Charge-Pump Frequency		180		220	Hz
Adapter Switch Charge-Pump Refresh Pulse	DLO	0.04		0.2	µs
	DHI	0.07		0.3	

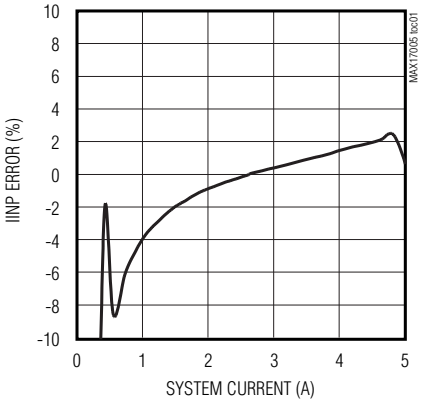
Note 1: Accuracy does not include errors due to external resistance tolerances.

Note 2: Adapter present conditions are tested at V_{DCIN} = 19V and V_{BATT} = 16.8V. Adapter absent conditions are tested at V_{DCIN} = 16V, V_{BATT} = 16.8V.

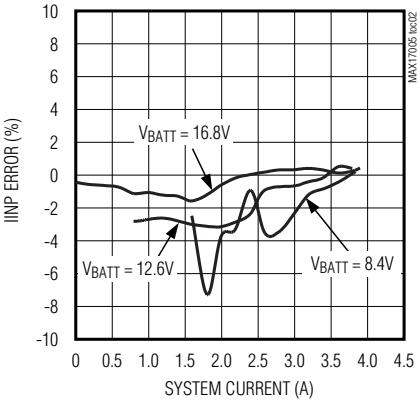
Typical Operating Characteristics

(Circuit of Figure 1, adapter = 19V, battery = 10V, ISET = 1.05V, V_{CTL} = GND, T_A = +25°C, unless otherwise noted.)

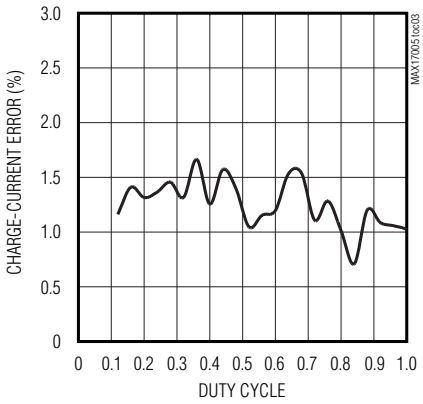
IINP DC ERROR vs. SYSTEM CURRENT



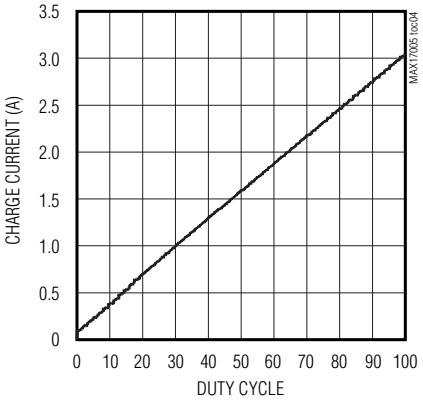
IINP ERROR vs. SYSTEM CURRENT



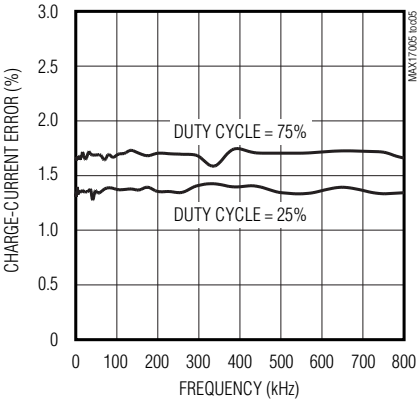
ISET PWM DUTY-CYCLE CHANGE



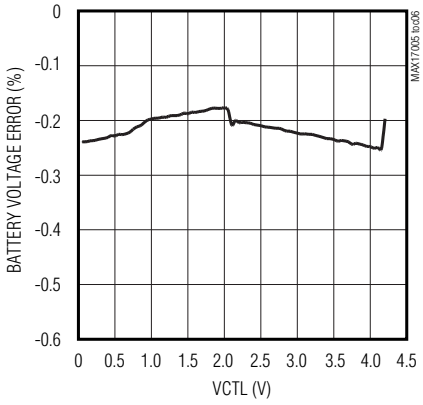
ISET PWM DUTY-CYCLE CHANGE



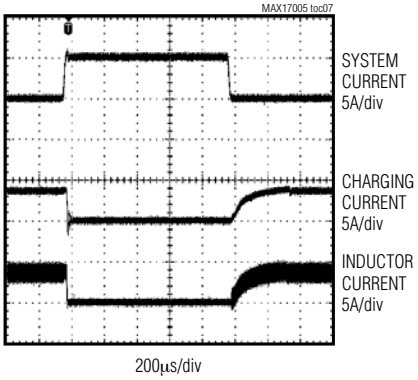
ISET PWM FREQUENCY SWEEP



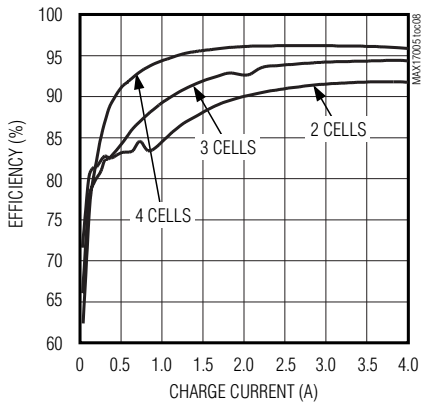
BATTERY VOLTAGE-SETTING ERROR



SYSTEM LOAD TRANSIENT



EFFICIENCY vs. CHARGE CURRENT

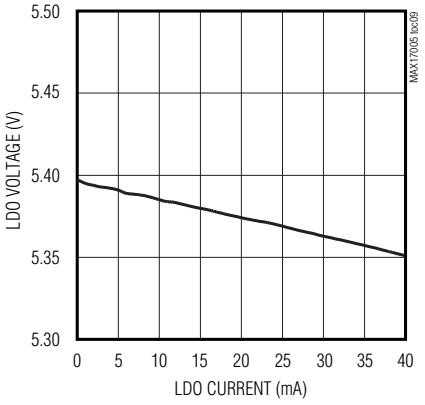


1.2MHz Low-Cost, High-Performance Chargers

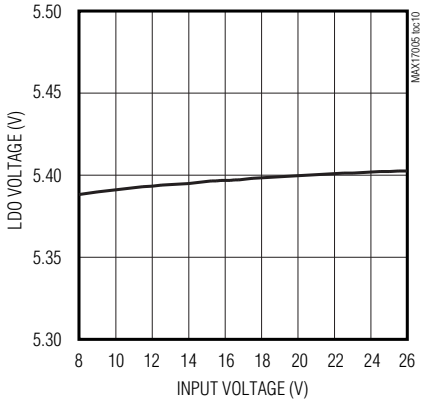
Typical Operating Characteristics (continued)

(Circuit of Figure 1, adapter = 19V, battery = 10V, ISET = 1.05V, V_{CTL} = GND, T_A = +25°C, unless otherwise noted.)

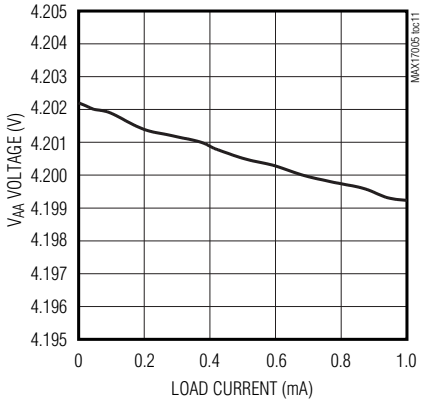
LDO LOAD REGULATION



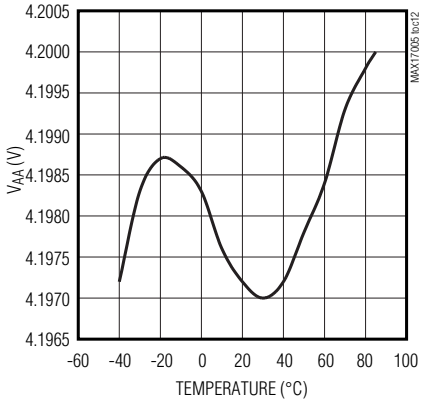
LDO LINE REGULATION



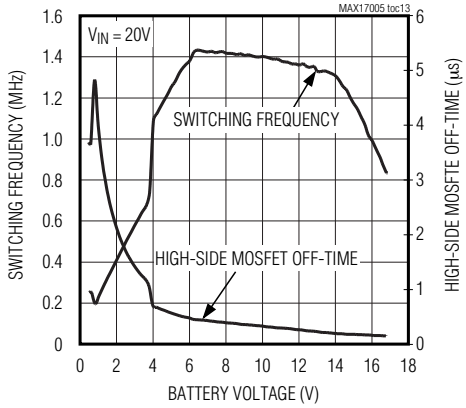
V_{AA} LOAD REGULATION



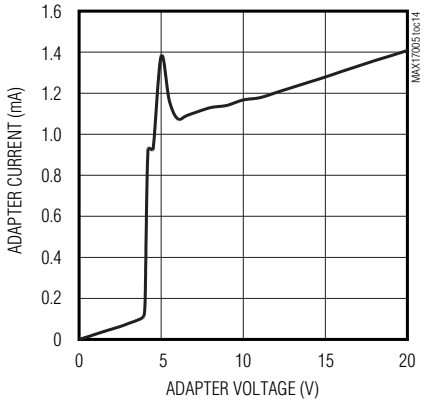
V_{AA} vs. TEMPERATURE



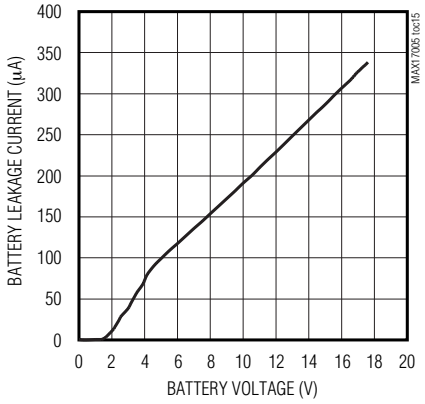
HIGH-SIDE MOSFET OFF-TIME AND SWITCHING FREQUENCY vs. BATTERY VOLTAGE



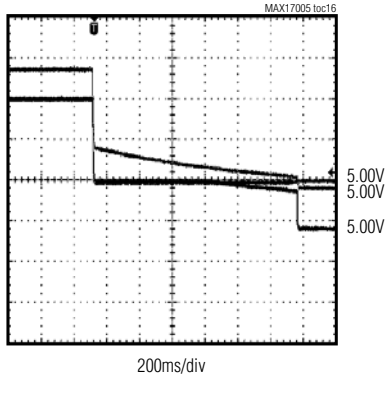
ADAPTER CURRENT vs. ADAPTER VOLTAGE



BATTERY LEAKAGE



ADAPTER REMOVAL



Pin Description

PIN	NAME	FUNCTION
1	DCIN	Charger Bias Supply Input. Bypass DCIN with a 1µF capacitor to PGND.
2	AGND	Analog Ground
3	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
4	CSIN	Output Current-Sense Negative Input
5	IINP	Input Current-Monitor Output. IINP sources the current proportional to the current sensed across CSSP and CSSN. The transconductance from (CSSP - CSSN) to IINP is 2.8µA/mV. See the *Analog Input Current-Monitor Output* section to configure the current monitor for a particular gain setting.
6	BATT	Battery Voltage Feedback Input
7	$\overline{ACOK}$	AC Detect Output. This open-drain output is high impedance when ACIN is lower than $V_{AA}/2$. Connect a 10kΩ pullup resistor from LDO to $\overline{ACOK}$.
8	CSSP	Input Current Sense for Positive Input. Connect a current-sense resistor from CSSP to CSSN.
9	CSSN	Input Current-Sense Negative Input
10	ISET	Dual Mode™ Input for Setting Maximum Charge Current. ISET can be configured either with a resistor voltage-divider or with a PWM signal from 128Hz to 500kHz. If there is no clock edge within 20ms, ISET defaults to analog input mode. Pull ISET to GND to shut down the charger. In the MAX17015, when the adapter is absent, drive ISET above 1V to enable IINP during battery discharge. When the adapter is reinserted, ISET must be released to the correct control level within 300ms.
11	PGND	Power Ground Connection for MOSFET Drivers
12	DLO	Low-Side Power-MOSFET Driver Output. Connect to low-side n-channel MOSFET gate.
13	LDO	Linear Regulator Output. LDO provides the power to the MOSFET drivers. LDO is the output of the 5.4V linear regulator supplied from DCIN. Bypass LDO with a 4.7µF ceramic capacitor from LDO to PGND.
14	BST	High-Side Driver Supply. Connect a 0.68µF capacitor from BST to LX.
15	DHI	High-Side Power-MOSFET Driver Output. Connect to high-side n-channel MOSFET gate.
16	LX	High-Side Driver Source Connection. Connect a 0.68µF capacitor from BST to LX.
17	ACIN	AC Adapter Detect Input. ACIN is the input to an uncommitted comparator.
18	V_{AA}	4.2V Voltage Reference and Device Power-Supply Input. Bypass V_{AA} with a 1µF capacitor to GND.
19	CC	Voltage Regulation Loop-Compensation Point. Connect 3kΩ and 0.01µF capacitor in series from CC to GND.
20	VCTL	Battery Voltage Adjust Input. VCTL sets the number of cells and adjusts the voltage per cell. The adjustment range is 4.2V to 4.4V per cell. See the *Setting Charge Voltage* section.
—	BP	Backside Paddle. Connect the backside paddle to analog ground.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

1.2MHz Low-Cost, High-Performance Chargers

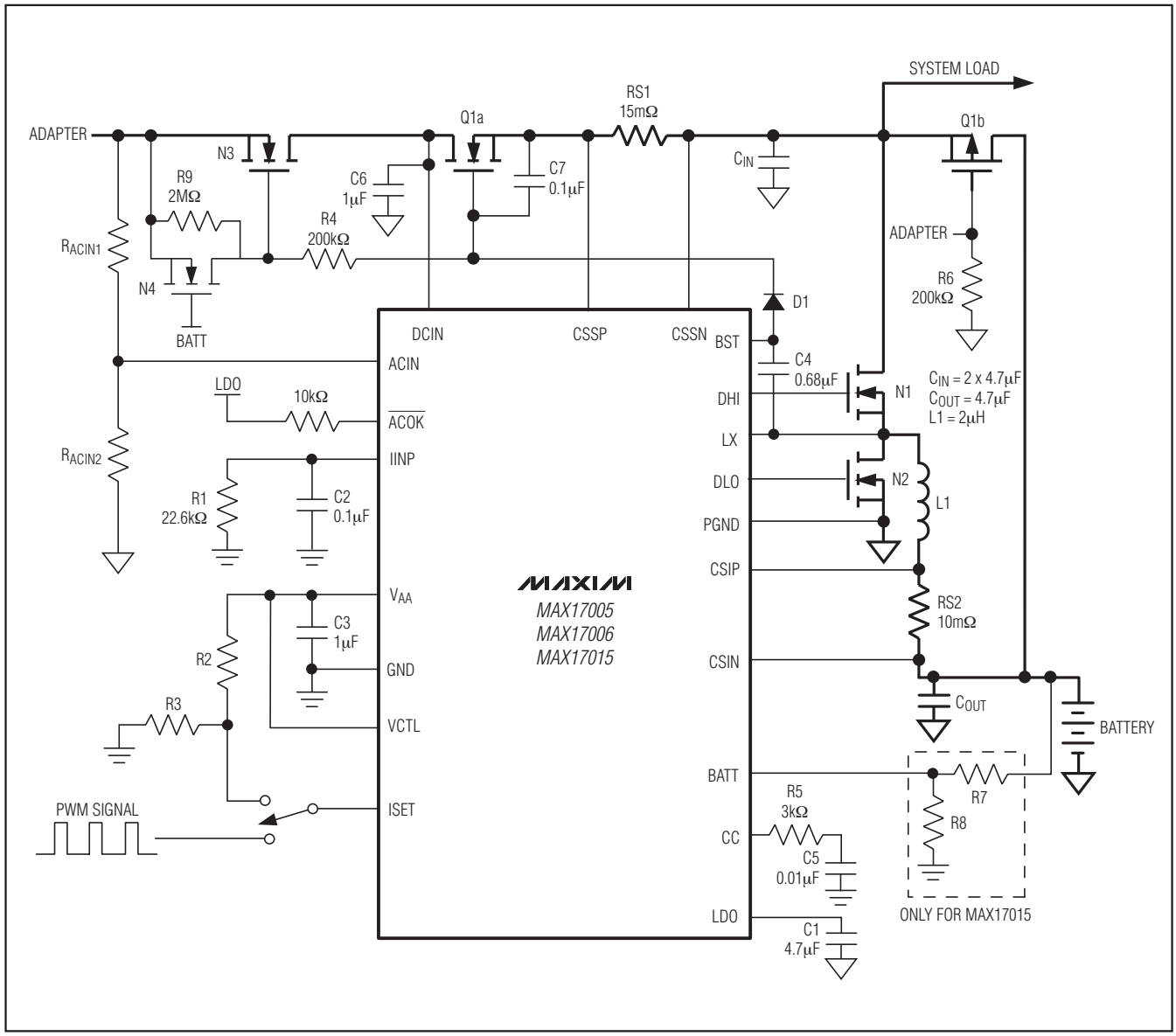


Figure 1. Typical Operating Circuit

Detailed Description

The MAX17005/MAX17006/MAX17015 include all the functions necessary to charge Li+, NiMH, and NiCd batteries. An all n-channel synchronous-rectified step-down DC-DC converter is used to implement a precision constant-current, constant-voltage charger. The charge current and input current-limit sense amplifiers have low-input offset errors (250µV typ), allowing the use of small-valued sense resistors.

The MAX17005/MAX17006/MAX17015 use a new thermally optimized high-frequency architecture. With this new architecture, the switching frequency is adjusted to control the power dissipation in the high-side MOSFET. Benefits of the new architecture include: reduced output capacitance and inductance, resulting in smaller printed-circuit board (PCB) area and lower cost.

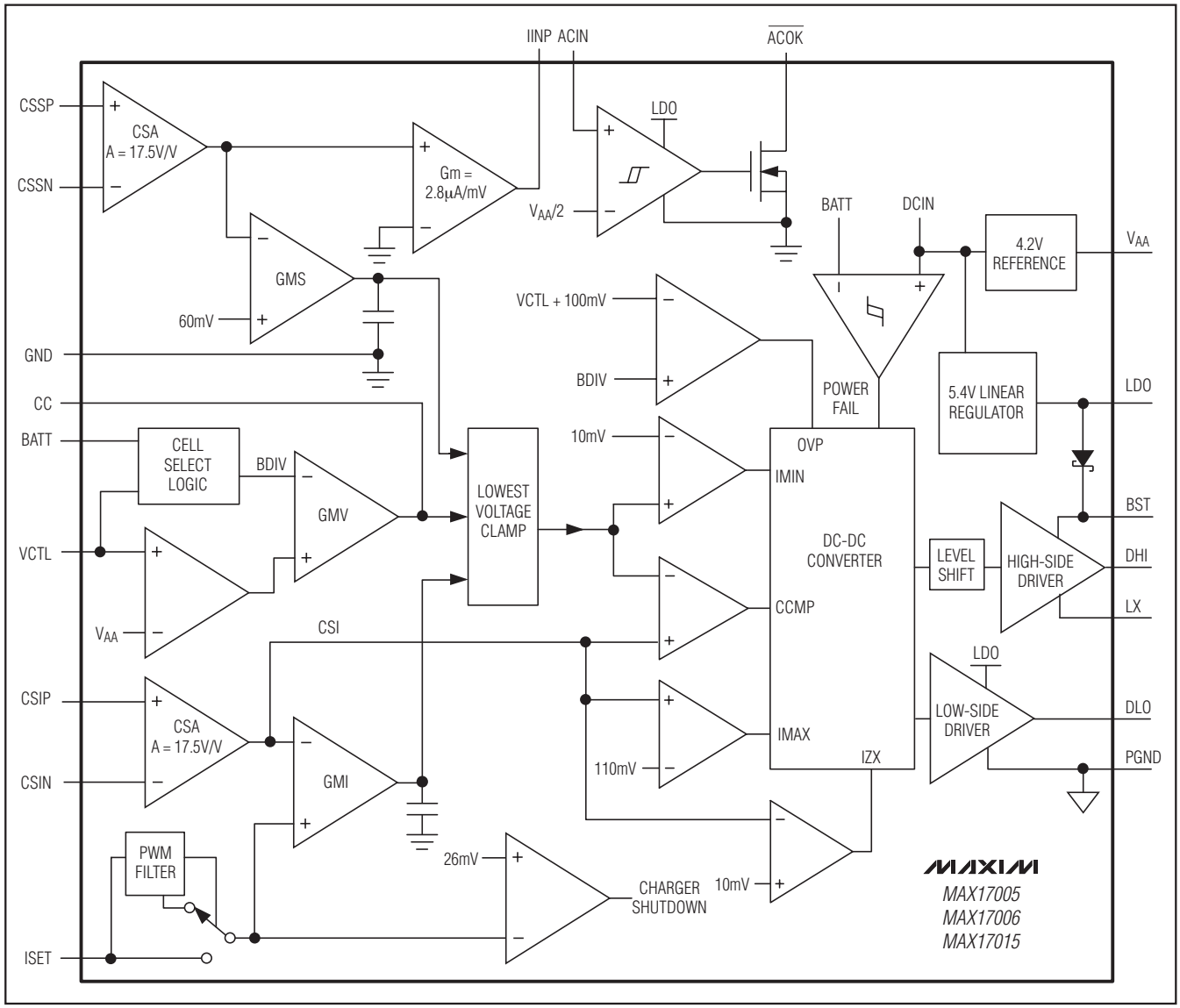


Figure 2. Functional Diagram

The MAX17005/MAX17006/MAX17015 feature a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The loops operate independently of each other. The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by VCTL. The CCI battery charge current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by ISET. The charge current-regulation loop is in control as long as the battery voltage is below the set point. When the battery voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. A third loop (CCS) takes control and reduces the charge current when the adapter current exceeds the input current limit.

The MAX17005/MAX17006/MAX17015 have single-point compensation. The two current loops are internally compensated while the voltage loop is compensated with a series RC network at CC pin. See the *CC Loop Compensation* section for the resistor and capacitor selection. A functional diagram is shown in Figure 2.

1.2MHz Low-Cost, High-Performance Chargers

Setting Charge Voltage

The VCTL input adjusts the battery-output voltage, V_{BATT}, and determines the number of cells. For 3- and 4-cell applications, use the MAX17005; for 2- and 3-cell applications, use the MAX17006. Use the MAX17015 to adjust the cell number and set the cell voltage with a resistive voltage-divider from the output. Based on the version of the part, the number of cells and the level of VCTL should be set as in Table 1:

Table 1. Cell Configuration

VERSION	NO. OF CELLS	LEVEL
MAX17005	3	2.4V < VCTL < 4.2V
MAX17005	4	0V < VCTL < 1.8V
MAX17006	2	0V < VCTL < 1.8V
MAX17006	3	2.4V < VCTL < 4.2V
MAX17015	Sets FB	VCTL = GND or VCTL = V_{AA}

The MAX17005 and MAX17006 support from 4.2V/cell to 4.4V/cell, whereas the MAX17015 supports minimum 2.1V. The maximum voltage is determined with the dropout performance of IC. When the required voltage falls outside the range available with the MAX17005 or MAX17006, the MAX17015 should be used.

The charge-voltage regulation for the MAX17005 and MAX17006 is calculated with the following equations:

$$V_{CELL} = 4.2V + \frac{4.2V - V_{VCTL}}{6}$$

for 3-cell selection of MAX17005 and MAX17006, 4.2V > VCTL > 2.4V:

$$V_{CELL} = 4.2V + \frac{V_{VCTL}}{6}$$

for 2- or 4-cell selection of MAX17006 or MAX17005, respectively, 0V < VCTL < 1.8V. Connect VCTL to GND or to V_{AA} for default 4.2V/cell battery-voltage setting.

For the MAX17015, connect VCTL to GND to set the FB regulation point to 2.1V. The charge-voltage regulation is calculated with the following equation:

$$V_{CHG\_REG} = V_{FB\_SETPOINT} \times \frac{R8 + R7}{R8}$$

There are two constraints in choosing R7 and R8. The resistors cannot be too small since they discharge the battery, and they cannot be too large because FB pin consumes less than 1µA of input bias current. Pick R8 to be approximately 10kΩ and then calculate R7.

FB regulation error (±0.5% max) and the tolerance of R7 and R8 both contribute to the error on the battery voltage. Use 0.1% feedback resistors for best accuracy.

Setting Charge Current

The voltage at ISET determines the voltage across current-sense resistor RS2. ISET can accept either analog or digital inputs. The full-scale differential voltage between CSIP and CSIN is 80mV (8A for RS2 = 10mΩ) for the analog input, and 60mV (6A for RS2 = 10mΩ) for the digital PWM input.

When the MAX17005/MAX17006/MAX17015 power up and the charger is ready, if there is no clock edge within 20ms, the circuit assumes ISET is an analog input, and disables the PWM filter block. To configure the charge current, force the voltage on ISET according to the following equation:

$$I_{CHG} = \frac{240mV}{RS2} \times \frac{V_{ISET}}{V_{AA}}$$

The input range for ISET is from 0 to $V_{AA}/2$. To shut down the charger, pull ISET below 26mV.

If there is a clock edge on ISET within 20ms, the PWM filter is enabled and ISET accepts digital PWM input. The PWM filter has a DAC with 8-bit resolution that corresponds to equivalent $V_{CSIP-CSIN}$ steps.

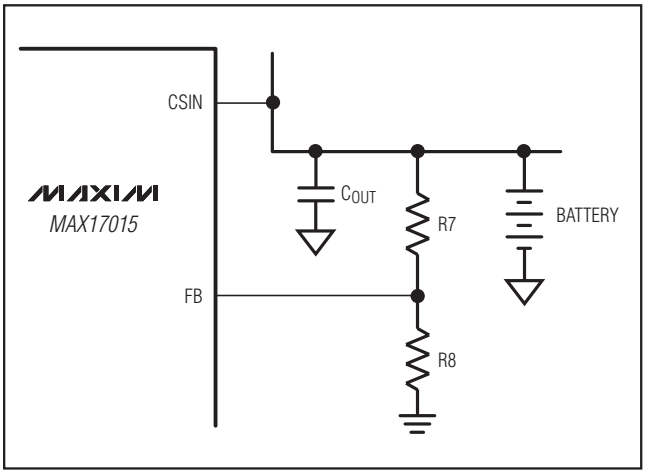


Figure 3. MAX17015 Charge-Voltage Regulation Feedback Network

The PWM filter accepts the digital signal with a frequency from 128Hz to 500kHz. Zero duty cycle shuts down the MAX17005/MAX17006/MAX17015, and 99.5% duty cycle corresponds to full scale (60mV) across CSIP and CSIN.

Choose a current-sense resistor (RS2) to have a sufficient power-dissipation rating to handle the full-charge current. The current-sense voltage can be reduced to minimize the power-dissipation period. However, this can degrade accuracy due to the current-sense amplifier's input offset (0.25mV typ). See *Typical Operating Characteristics* to estimate the charge-current accuracy at various set points.

Setting Input-Current Limit

The total input current, from a wall adapter or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input-current limit, the controller decreases the charge current to provide priority to system load current. System current normally fluctuates as portions of the system are powered up or down. The input-current-limit circuit reduces the power requirement of the AC wall adapter, which reduces adapter cost. As the system supply rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase without limit.

The total input current is the sum of the device supply current, the charger input current, and the system load current. The total input current can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \frac{I_{CHARGE} \times V_{BATTERY}}{V_{IN} \times \eta}$$

where η is the efficiency of the DC-to-DC converter (typically 85% to 95%).

In the MAX17005/MAX17006/MAX17015, the voltage across CSSP and CSSN is constant at 60mV. Choose the current-sense resistor, RS1, to set the input current limit. For example, for 4A input current limit, choose RS1 = 15mΩ. For the input current-limit settings, which cannot be achievable with standard sense resistor values, use a resistive voltage-divider between CSSP and CSSN to tune the setting (Figure 4).

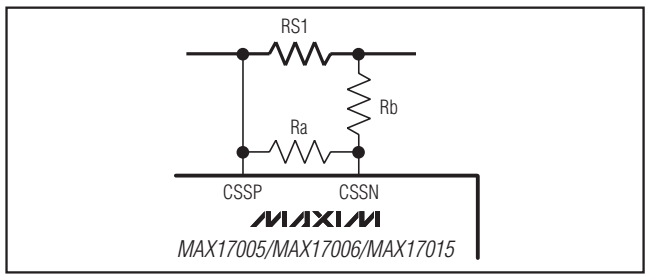


Figure 4. Input Current-Limit Fine Tuning

$$I_{INPUT\_LIMIT} = \frac{60mV}{RS1} \times (1 + \frac{Rb}{Ra})$$

To minimize power dissipation, first choose RS1 according to the closest available value. For convenience, choose Ra = 6kΩ and calculate Rb from the above equation.

Choose a current-sense resistor (RS1) to have a sufficient power rating to handle the full system current. The current-sense resistor can be reduced to improve efficiency, but this degrades accuracy due to the current-sense amplifier's input offset (0.15mV typ). See *Typical Operating Characteristics* to estimate the input current-limit accuracy at various set points.

Automatic Power-Source Selection

The MAX17005/MAX17006/MAX17015 use an external charge pump to drive the gate of an n-channel adapter selection switch (N3 and Q1a). In Figure 1, when the adapter is present, BST is biased 5V above $V_{ADAPTER}$ so that N3 and Q1a are on, and Q1b is off. As long as the adapter is present, even though the charger is off, the power stage forces a refresh pulse to the BST charge pump every 5ms.

When the adapter voltage is removed, the charger stops generating BST refresh pulses and N4 forces N2 off, Q1b turns on and supplies power to the system from the battery.

In Figure 1, D1 must have low forward-voltage drop and low reverse-leakage current to ensure sufficient gate drive at N3 and Q1a. A 100mA, low reverse-leakage Schottky diode is the right choice.

Analog Input Current-Monitor Output

Use IINP to monitor the system-input current, which is sensed across CSSP and CSSN. The voltage at IINP is proportional to the input current:

$$I_{INPUT} = \frac{V_{IINP}}{RS1 \times G_{IINP} \times R_{IINP}}$$

where I_{INPUT} is the DC current supplied by the AC adapter, G_{IINP} is the transconductance of the sense amplifier (2.8 mA/V typ), and R_{IINP} is the resistor connected between IINP and ground. Typically, IINP has a 0V to 3.5V output voltage range. Leave IINP unconnected when not used.

1.2MHz Low-Cost, High-Performance Chargers

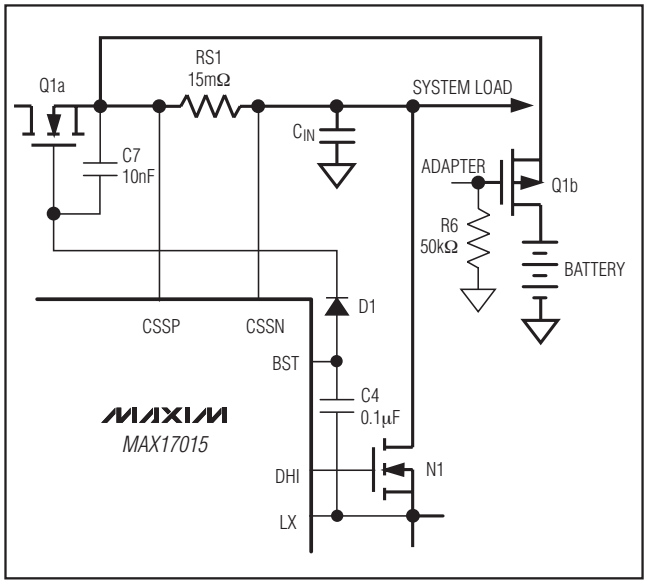


Figure 5. Current-Monitoring Design Battery Discharge

IINP can also be used to monitor battery discharge current (see Figure 5). In the MAX17015, when the adapter is absent, drive ISET above 1V to enable IINP during battery discharge. When the adapter is reinserted, ISET must be released to the correct control level within 300ms.

AC Adapter Detection

The MAX17005/MAX17006/MAX17015 include a hysteretic comparator that detects the presence of an AC power adapter. When ACIN is lower than 2.1V, the open-drain ACOK output becomes high impedance. Connect a 10kΩ pullup resistance between LDO and ACOK. Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. Select the resistive voltage-divider so that the voltage on ACIN does not to exceed its absolute maximum rating (6V).

LDO Regulator and V_{AA}

An integrated low-dropout (LDO) linear regulator provides a 5.4V supply derived from DCIN, and delivers over 40mA of load current. Do not use the LDO to external loads greater than 10mA. The LDO powers the gate drivers of the n-channel MOSFETs. See the *MOSFET Drivers* section. Bypass LDO to PGND with a 4.7µF ceramic capacitor. V_{AA} is 4.2V reference supplied by DCIN. V_{AA} biases most of the control circuitry, and should be bypassed to GND with a 1µF or greater ceramic capacitor.

Operating Conditions

The MAX17005/MAX17006/MAX17015 have the following operating states:

- **Adapter Present:** When DCIN is greater than 8.7V, the controller detects the adapter. In this condition, both the LDO and V_{AA} turn on and battery charging is allowed:
  a) **Charging:** The total MAX17005/MAX17006/MAX17015 quiescent current when charging is 3mA (max) plus the current required to drive the MOSFETs.
  b) **Not Charging:** To disable charging drive ISET below 26mV. When the adapter is present and charging is disabled, the total adapter quiescent current is less than 1.5mA and the total battery quiescent current is less than 60µA. The charge pump still operates.
- **Adapter Absent (Power Fail):** When V_{DCIN} is less than V_{CSIN} + 120mV, the DC-DC converter is in dropout. The charger detects the dropout condition and shuts down.

The MAX17005/MAX17006/MAX17015 allow charging under the following conditions:

- DCIN > 7.5V, LDO > 4V, V_{AA} > 3.1V
- V_{DCIN} > V_{CSIN} + 420mV (300mV falling hysteresis)
- V_{ISET} > 45mV or PWM detected

DC-DC Converter

The MAX17005/MAX17006/MAX17015 employ a synchronous step-down DC-DC converter with an n-channel high-side MOSFET switch and an n-channel low-side synchronous rectifier. The charger features a controlled inductor current-ripple architecture, current-mode control scheme with cycle-by-cycle current limit. The controller's off-time (t_{OFF}) is adjusted to keep the high-side MOSFET junction temperature constant. In this way, the controller switches faster when the high-side MOSFET has available thermal capacity. This allows the inductor current ripple and the output-voltage ripple to decrease so that smaller and cheaper components can be used. The controller can also operate in discontinuous conduction mode for improved light-load efficiency.

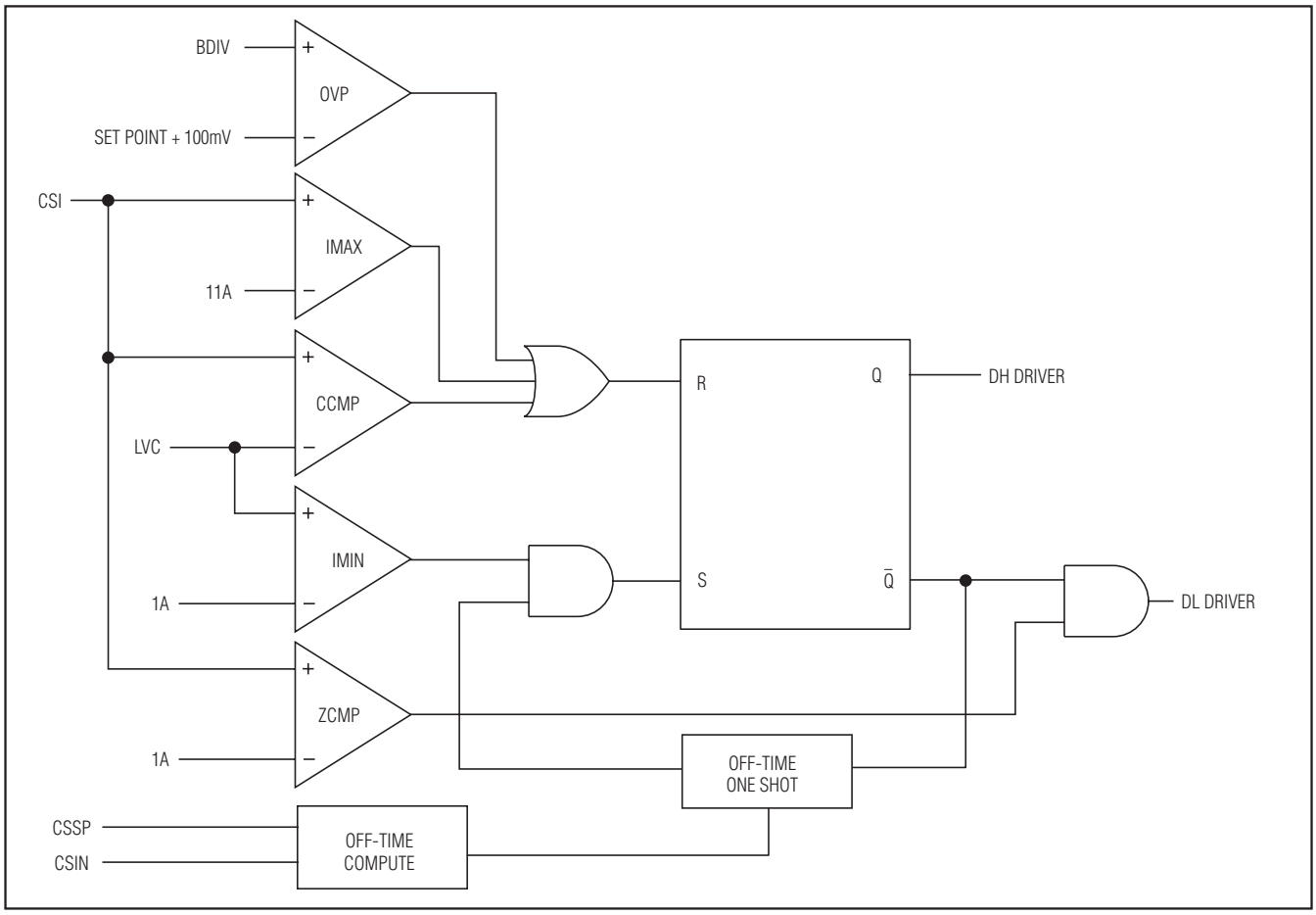


Figure 6. DC-DC Converter Functional Diagram

The operation of the DC-to-DC controller is determined by the following five comparators as shown in the functional diagram in Figures 2 and 6:

- The IMIN comparator triggers a pulse in discontinuous mode when the accumulated error is too high. IMIN compares the control signal (LVC) against 10mV (referred at V_{CSIP} - V_{CSIN}). When LVC is less than this threshold, DHI and DLO are both forced low. Indirectly, IMIN sets the peak inductor current in discontinuous mode.
- The CCMP comparator is used for current-mode regulation in continuous-conduction mode. CCMP compares LVC against the inductor current. The high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- The IMAX comparator provides a secondary cycle-by-cycle current limit. IMAX compares CSI to 110mV (corresponding to 11A when RS2 = 10mΩ). The high-side MOSFET on-time is terminated when the current-sense signal exceeds 11A. A new cycle cannot start until the IMAX comparator's output goes low.
- The ZCMP comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 1A (RS2 = 10mΩ). When the inductor current is lower than the 1A threshold, the comparator output is high, and DLO is turned off.
- The OVP comparator is used to prevent overvoltage at the output due to battery removal. OVP compares BATT against the VCTL. When BATT is 100mV/cell above the set value, the OVP comparator output goes high, and the high-side MOSFET on-time is terminated. DHI and DLO remain off until the OVP condition is removed.

1.2MHz Low-Cost, High-Performance Chargers

CC, CCI, CCS, and LVC Control Blocks

The MAX17005/MAX17006/MAX17015 control input current (CCS control loop), charge current (CCI control loop), or charge voltage (CC control loop), depending on the operating condition. The three control loops, CC, CCI, and CCS are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CC, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section). The CCS and CCI loops are compensated internally, and the CC loop is compensated externally.

Continuous-Conduction Mode

With sufficiently large charge current, the MAX17005/MAX17006/MAX17015s' inductor current never crosses zero, which is defined as continuous-conduction mode. The controller starts a new cycle by turning on the high-side MOSFET and turning off the low-side MOSFET. When the charge-current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side MOSFET and turning on the low-side MOSFET. The operating frequency is governed by the off-time and is dependent upon V_{CSIN} and V_{DCIN}.

The on-time can be determined using the following equation:

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{DCIN} - V_{BATT}}$$

where:

$$I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}$$

The switching frequency can then be calculated:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}}$$

At the end of the computed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 10mV (V_{CSIP} - V_{CSIN} referred), and the charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high, IMAX must be low, and OVP must be low for the controller to initiate a new cycle. If the peak inductor current exceeds IMAX comparator threshold or the output voltage exceeds the OVP threshold, then the on-time is terminated. The cycle-by-cycle current limit effectively protects against overcurrent and short-circuit faults.

If during the off-time the inductor current goes to zero, the ZCMP comparator output pulls high, turning off the low-side MOSFET. Both the high- and low-side MOSFETs are turned off until another cycle is ready to begin. ZCOMP causes the MAX17005/MAX17006/MAX17015 to enter into the discontinuous conduction mode (see the *Discontinuous Conduction* section).

Discontinuous Conduction

The MAX17005/MAX17006/MAX17015 can also operate in discontinuous conduction mode to ensure that the inductor current is always positive. The MAX17005/MAX17006/MAX17015 enter discontinuous conduction mode when the output of the LVC control point falls below 10mV (referred at V_{CSIP} - V_{CSIN}). For RS2 = 10mΩ, this corresponds to a peak inductor current of 1A.

In discontinuous mode, a new cycle is not started until the LVC voltage rises above IMIN. Discontinuous mode operation can occur during conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the charger is in constant-voltage mode with a nearly full battery pack.

Compensation

The charge voltage, charge current, and input current-limit regulation loops are compensated separately. The charge current and input current-limit loops, CCI and CCS, are compensated internally, whereas the charge voltage loop is compensated externally at CC.

CC Loop Compensation

The simplified schematic in Figure 7 is sufficient to describe the operation of the controller's voltage loop, CC. The required compensation network is a pole-zero pair formed with C_{CC} and R_{CC}. The zero is necessary to compensate the pole formed by the output capacitor and the load. R_{ESR} is the equivalent series resistance (ESR) of the charger output capacitor (C_{OUT}). R_L is the equivalent charger output load, where $R_L = \Delta V_{BATT}/\Delta I_{CHG}$. The equivalent output impedance of the GMV amplifier, R_{OGMV}, is greater than 10MΩ. The voltage-amplifier transconductance, GMV = 0.125µA/mV. The DC-DC converter transconductance is dependent upon charge current-sense resistor RS2:

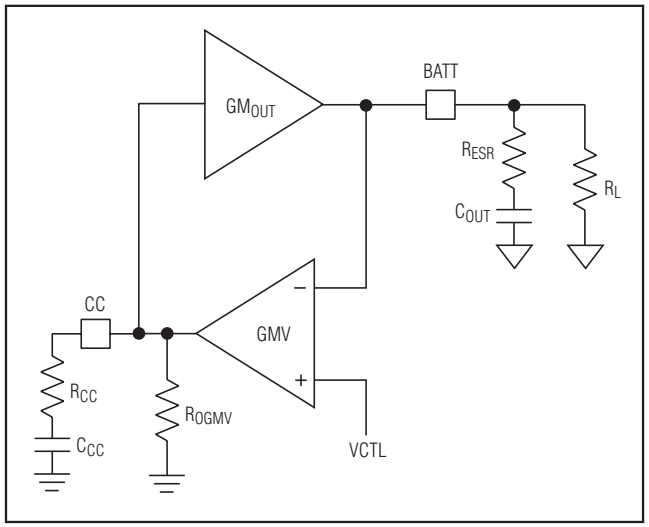


Figure 7. CC Loop Diagram

$$GM_{OUT} = \frac{1}{ACSI \times RS2}$$

where A_{CSI} = 20, and RS2 = 10mΩ in the typical application circuits, so GM_{OUT} = 5A/V.

The loop transfer function is given by:

$$LTF = GM_{OUT} \times R_L \times GMV \times R_{OGMV} \times \frac{(1 + sC_{OUT} \times R_{ESR})(1 + sC_{CC} \times R_{CC})}{(1 + sC_{CC} \times R_{OGMV})(1 + sC_{OUT} \times R_L)}$$

The poles and zeros of the voltage-loop transfer function are listed from lowest frequency to highest frequency in Table 2.

Near crossover, C_{CC} is much lower impedance than R_{OGMV}. Since C_{CC} is in parallel with R_{OGMV}, C_{CC} dominates the parallel impedance near crossover. Additionally, R_{CC} is much higher impedance than C_{CC} and dominates the series combination of R_{CC} and C_{CC}, so:

$$\frac{R_{OGMV} \times (1 + sC_{CC} \times R_{CC})}{(1 + sC_{CC} \times R_{OGMV})} \cong R_{CC}$$

C_{OUT} is also much lower impedance than R_L near crossover so the parallel impedance is mostly capacitive and:

$$\frac{R_L}{(1 + sC_{OUT} \times R_L)} \cong \frac{1}{sC_{OUT}}$$

Table 2. CC Loop Poles and Zeros

NAME	EQUATION	DESCRIPTION
CCV Pole	$f_{P\_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CC}}$	Lowest frequency pole created by C_{CV} and GMV's finite output resistance.
CCV Zero	$f_{Z\_CV} = \frac{1}{2\pi R_{CC} \times C_{CC}}$	Voltage-loop compensation zero. If this zero is at the same frequency or lower than output pole f_{P_OUT}, the loop-transfer function approximates a single-pole response near the crossover frequency. Choose C_{CV} to place this zero at least one decade below crossover to ensure adequate phase margin.
Output Pole	$f_{P\_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$	Output pole formed with the effective load resistance R_L and the output capacitance C_{OUT}. R_L influences the DC gain but does not affect the stability of the system or the crossover frequency.
Output Zero	$f_{Z\_OUT} = \frac{1}{2\pi R_{ESR} \times C_{OUT}}$	Output ESR Zero. This zero can keep the loop from crossing unity gain if f_{Z_OUT} is less than the desired crossover frequency; therefore, choose a capacitor with an ESR zero greater than the crossover frequency.

1.2MHz Low-Cost, High-Performance Chargers

If R_{ESR} is small enough, its associated output zero has a negligible effect near crossover and the loop-transfer-function can be simplified as follows:

$$LTF = GM_{OUT} \times \frac{R_{CC}}{sC_{OUT}} G_{MV}$$

Setting LTF = 1 to solve for the unity-gain frequency yields:

$$f_{CO\_CV} = GM_{OUT} \times G_{MV} \times \frac{R_{CC}}{2\pi \times C_{OUT}}$$

For stability, choose a crossover frequency lower than 1/10 the switching frequency (f_{OSC}). For example, choose a crossover frequency of 50kHz and solve for R_{CC} using the component values listed in Figure 1 to yield R_{CC} = 3kΩ:

$$R_{CC} = \frac{2\pi \times C_{OUT} \times f_{CO\_CV}}{GMV \times GM_{OUT}} \cong 3k\Omega$$

GMV = 0.125µA/mV

GM_{OUT} = 5A/V

C_{OUT} = 4.7µF

f_{OSC_CV} = 600kHz

R_L = 0.2Ω

f_{CO_CV} = 50kHz

To ensure that the compensation zero adequately cancels the output pole, select $f_{Z\_CV} \le f_{P\_OUT}$:

$$C_{CC} \ge (R_L/R_{CC}) \times C_{OUT}$$

$C_{CC} \ge$ 300pF (assuming 2 cells and 2A maximum charge current).

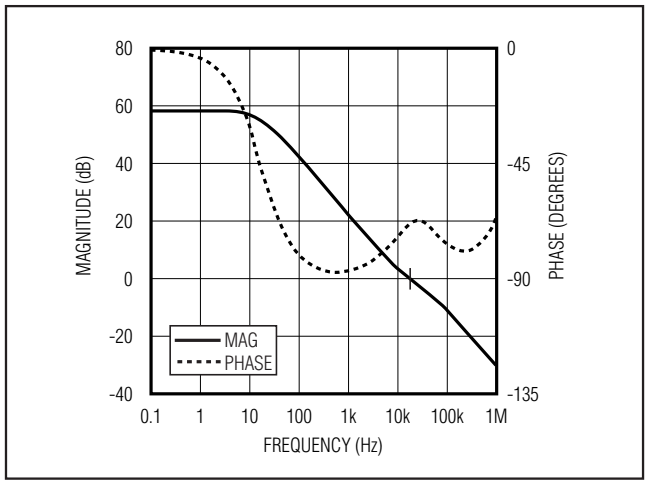


Figure 8. CC Loop Response

Figure 8 shows the Bode plot of the voltage-loop-frequency response using the values calculated above.

MOSFET Drivers

The DHI and DLO outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is the same for both the low-side and high-sides switches. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. There must be a low-resistance, low-inductance path from the DLO driver to the MOSFET gate to prevent shoot-through. Otherwise, the sense circuitry in the MAX17005/MAX17006 interpret the MOSFET gate as "off" while there is still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares or fewer (1.25mm to 2.5mm wide if the MOSFET is 25mm from the device). Unlike the DLO output, the DHI output uses a 50ns (typ) delay time to prevent the low-side MOSFET from turning on until DHI is fully off. The same considerations should be used for routing the DHI signal to the high-side MOSFET.

The high-side driver (DHI) swings from LX to 5V above LX (BST) and has a typical impedance of 1.5Ω sourcing and 0.8Ω sinking. The strong high-side MOSFET driver eliminates most of the power dissipation due to switching losses. The low-side driver (DLO) swings from LDO to ground and has a typical impedance of 3Ω sinking and 3Ω sourcing. This helps prevent DLO from being pulled up when the high-side switch turns on due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the MOSFETs that can be used. Using a low-side MOSFET with smaller gate-to-drain capacitance can prevent these problems.

Design Procedure

MOSFET Selection

Choose the n-channel MOSFETs according to the maximum required charge current. The MOSFETs must be able to dissipate the resistive losses plus the switching losses at both $V_{DCIN(MIN)}$ and $V_{DCIN(MAX)}$.

For the high-side MOSFET, the worst-case resistive power losses occur at the maximum battery voltage and minimum supply voltage:

$$PD_{COND}(High\,Side) = \frac{V_{BATT(MAX)}}{V_{DCIN(MIN)}} \times I_{CHG}{}^2 \times R_{DS(ON)}$$

Generally, a low gate charge high-side MOSFET is preferred to minimize switching losses. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V. Calculating the power dissipation in N1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on N1:

$$PD_{SW}(HS) = \frac{1}{2} \times t_{TRANS} \times V_{CSSP} \times I_{CHG} \times f_{SW}$$

where t_{TRANS} is the drivers transition time and can be calculated as follows:

$$t_{TRANS} = \left(\frac{1}{I_{GSRC}} + \frac{1}{I_{GSNK}} \right) \times \left(Q_{GD} + Q_{GS} \right)$$

I_{GSRC} and I_{GSNK} are the peak gate-drive source/sink current (3Ω sourcing and 0.8Ω sinking, typically). The MAX17005/MAX17006/MAX17015 control the switching frequency as shown in the *Typical Operating Characteristics*.

The following is the power dissipated due to high-side n-channel MOSFET's output capacitance (C_{RSS}):

$$PD_{CRSS}(HS) \approx \frac{V^2_{CSSP} \times C_{RSS} \times f_{SW}}{2}$$

The following high-side MOSFET's loss is due to the reverse-recovery charge of the low-side MOSFET's body diode:

$$PD_{QRR}(HS) = \frac{Q_{RR2} \times V_{CSSP} \times f_{SW}}{2}$$

Ignore PD_{QRR}(HighSide) if a Schottky diode is used parallel to a low-side MOSFET.

The total high-side MOSFET power dissipation is:

$$PD_{TOTAL}(HS) \approx PD_{COND}(HS) + PD_{SW}(HS) + PD_{CRSS}(HS) + PD_{QRR}(HS)$$

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes hot when biased from $V_{DCIN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N2), the worst-case power dissipation always occurs at maximum input voltage:

$$PD_{COND}(LS) = \left(1 - \frac{V_{BATT(MIN)}}{V_{CSSP(MAX)}} \right) \times I_{CHG}^2 \times R_{DS(ON)}$$

The following additional loss occurs in the low-side MOSFET due to the body diode conduction losses:

$$PD_{BDY}(LS) = 0.05 \times I_{PEAK} \times 0.4V$$

The total power low-side MOSFET dissipation is:

$$PD_{TOTAL}(LS) \approx PD_{COND}(LS) + PD_{BDY}(LS)$$

These calculations provide an estimate and are not a substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on the MOSFET.

Inductor Selection

The selection of the inductor has multiple trade-offs between efficiency, transient response, size, and cost. Small inductance is cheap and small, and has a better transient response due to higher slew rate; however, the efficiency is lower because of higher RMS current. High inductance results in lower ripple so that the need of the output capacitors for output voltage ripple goes low.

The MAX17005/MAX17006/MAX17015 combine all the inductor trade-offs in an optimum way by controlling switching frequency. High-frequency operation permits the use of a smaller and cheaper inductor, and consequently results in smaller output ripple and better transient response.

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. For optimum efficiency, choose the inductance according to the following equation:

$$L = \frac{k \times V_{IN}^2}{4 \times I_{CHG} \times LIR_{MAX}}$$

where k = 35ns/V.

1.2MHz Low-Cost, High-Performance Chargers

For optimum size and inductor current ripple, choose LIR_{MAX} = 0.4, which sets the ripple current to 40% the charge current and results in a good balance between inductor size and efficiency. Higher inductor values decrease the ripple current. Smaller inductor values save cost but require higher saturation current capabilities and degrade efficiency.

Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 the ripple current (ΔIL):

$$I_{SAT} = I_{CHG} + (1/2)\,\Delta IL$$

The ripple current is determined by:

$$\Delta IL = \frac{k \times V_{IN}^2}{4L}$$

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up and surge currents:

$$IRMS = ICHG \times \left(\frac{\sqrt{V_{BATT} \times (V_{DCIN} - V_{BATT})}}{V_{DCIN}} \right)$$

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately 10°C. The maximum ripple current occurs at 50% duty factor or V_{DCIN} = 2 x V_{BATT}, which equates to 0.5 x I_{CHG}. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions.

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to ensure the stability of the DC-to-DC converter (see the *Compensation* section.) Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents. Choose the output capacitor based on:

$$C_{OUT} = \frac{I_{RIPPLE}}{f_{SW} \times 8 \times \Delta V_{BATT}} \times k_{CAP-BIAS}$$

Choose $k_{CAP-BIAS}$ is a derating factor of 2 for typical 25V-rated ceramic capacitors.

For f_{SW} = 800kHz, I_{RIPPLE} = 1A, and to get ΔV_{BATT} = 70mV, choose C_{OUT} as 4.7µF.

If the internal resistance of battery is close to the ESR of the output capacitor, the voltage ripple is shared with the battery and is less than calculated.

Applications Information

Setting Input Current Limit

The input current limit should be set based on the current capability of the AC adapter and the tolerance of the input current limit. The upper limit of the input current threshold should never exceed the adapter's minimum available output current. For example, if the adapter's output current rating is 5A ±10%, the input current limit should be selected so that its upper limit is less than 5A × 0.9 = 4.5A. Since the input current-limit accuracy of the MAX17005/MAX17006/MAX17015 is ±3%, the typical value of the input current limit should be set at 4.5A/1.03 ≈ 4.36A. The lower limit for input current must also be considered. For chargers at the low end of the spec, the input current limit for this example could be 4.36A × 0.95 or approximately 4.14A.

Layout and Bypassing

Bypass DCIN with a 0.1µF ceramic to ground (Figure 1). N1 and N2 protect the MAX17005/MAX17006/MAX17015 when the DC power source input is reversed. Bypass V_{AA}, CSSP, and LDO as shown in Figure 1.

Good PCB layout is required to achieve specified noise immunity, efficiency, and stable performance. The PCB layout designer must be given explicit instructions—preferably, a sketch showing the placement of the power switching components and high current routing. Refer to the PCB layout in the MAX17005/MAX17006/MAX17015 evaluation kit for examples. A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections, and the inner layers for an uninterrupted ground plane.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:
   a) Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
   b) Minimize ground trace lengths in the high-current paths.

c) Minimize other trace lengths in the high-current paths.

d) Use > 5mm wide traces in the high-current paths.

e) Connect C_{IN} to high-side MOSFET (10mm max length).

f) Minimize the LX node (MOSFETs, rectifier cathode, inductor (15mm max length)). Keep LX on one side of the PCB to reduce EMI radiation.

Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the paddle. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PCB layout problems.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and V_{AA} capacitor). **Important:** the IC must be no further than 10mm from the current-sense resistors. Quiet connections to V_{AA} and CC should be returned to a separate ground (GND) island. There is very little current flowing in these traces, so the ground island need not be very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low-current connections can be made through vias. The ground pad on the backside of the package should also be connected to this quiet ground island.

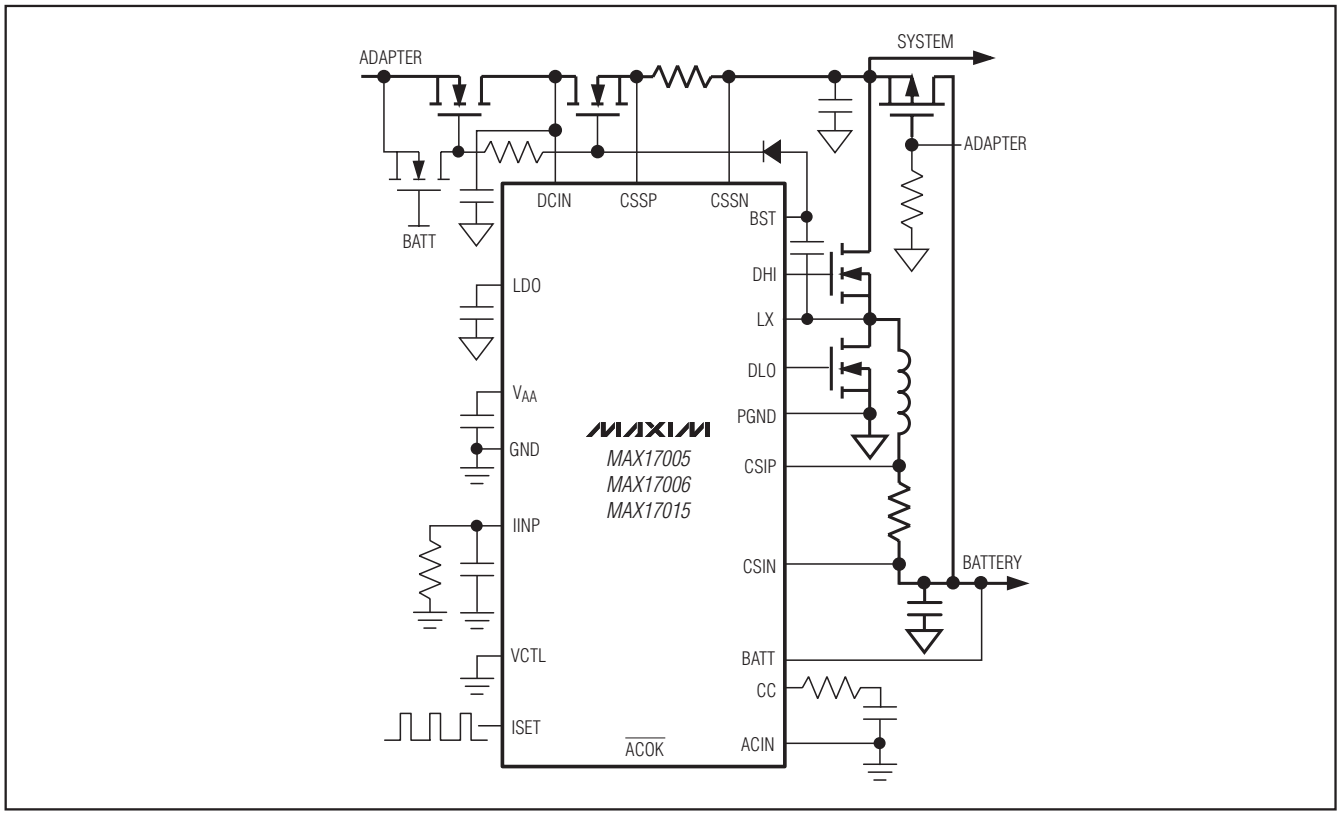
3) Keep the gate drive traces (DHI and DLO) as short as possible (L < 20mm), and route them away from the current-sense lines and V_{AA}. These traces should also be relatively wide (W > 1.25mm).

4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.

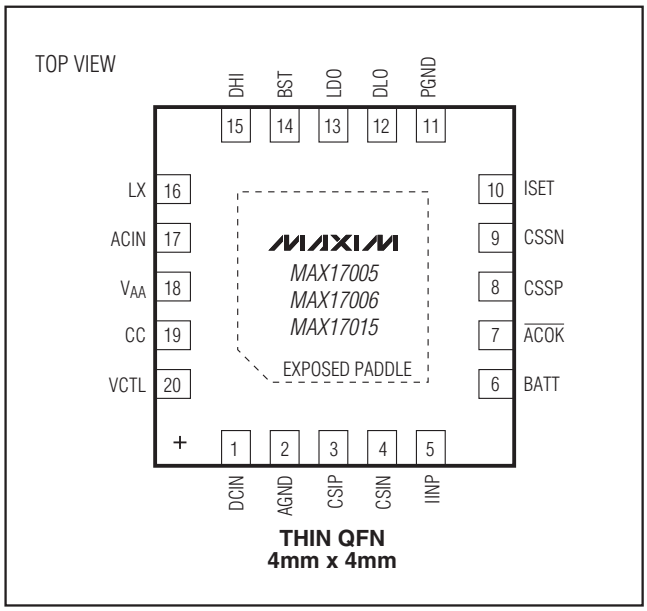
5) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location.

1.2MHz Low-Cost, High-Performance Chargers

Minimal Operating Circuit



Pin Configuration



THIN QFN
4mm x 4mm

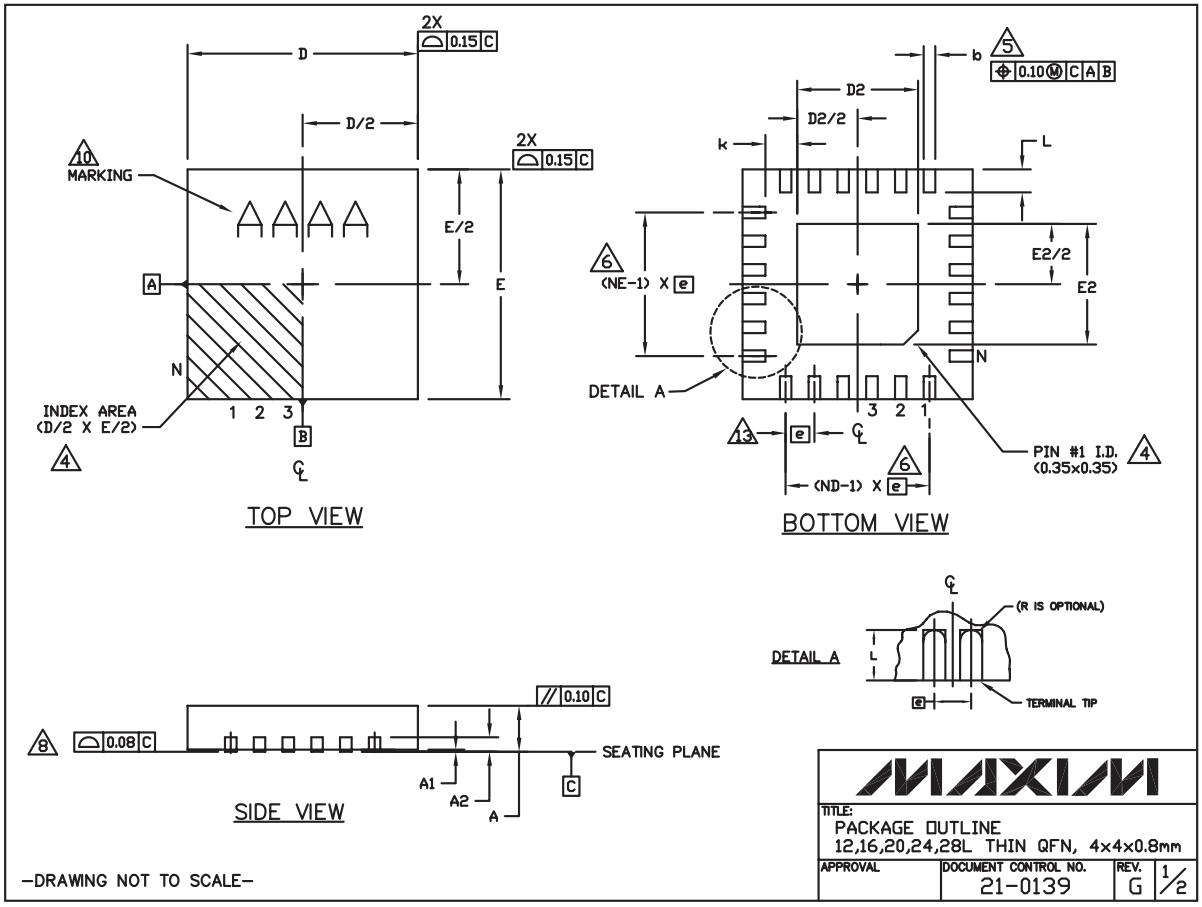
Chip Information

TRANSISTOR COUNT: 12,990

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



1.2MHz Low-Cost, High-Performance Chargers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	G	2/2

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX17005ETP+ MAX17005ETP+T MAX17006ETP+ MAX17006ETP+T MAX17015ETP+ MAX17015ETP+T